LH64400

PRELIMINARY

CMOS 4M (1M × 4) Dynamic RAM

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FEATURES

- 1,048,576 × 4 bit organization
- Access times: 80/100 ns (MAX.)
- Cycle times: 140/160 ns (MIN.)
- Cycle time in high speed page mode: 50/55 ns (MIN.)
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
  Operating: 523/468 mW (MAX.)
  Standby: 5.5 mW (MAX.)
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- 8-bit parallel test mode
  (contact SHARP for details)
- 1,024 refresh cycle
  (refresh period (MAX.) = 16 ms)
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP
  26-pin, 300-mil TSOP
  (normal/reverse bend pins)

DESCRIPTION

The LH64400 is a 1,048,576 × 4 bit dynamic RAM which provides a high speed page mode operation.

The LH64400 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ/TSOP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH64400 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

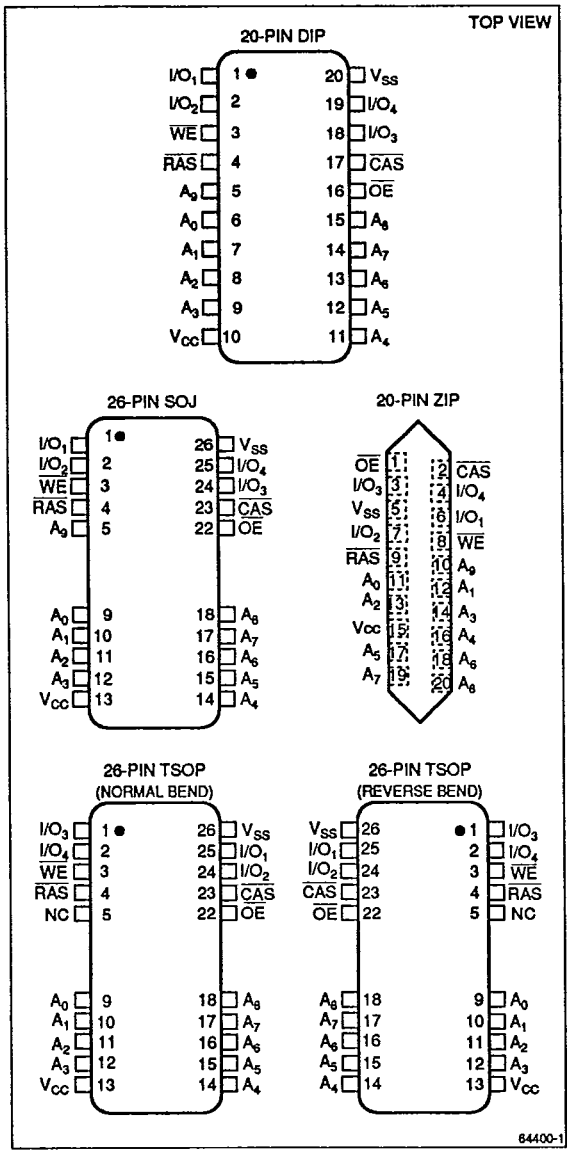

Figure 1. Pin Connections for DIP, SOJ, ZIP, and TSOP Packages

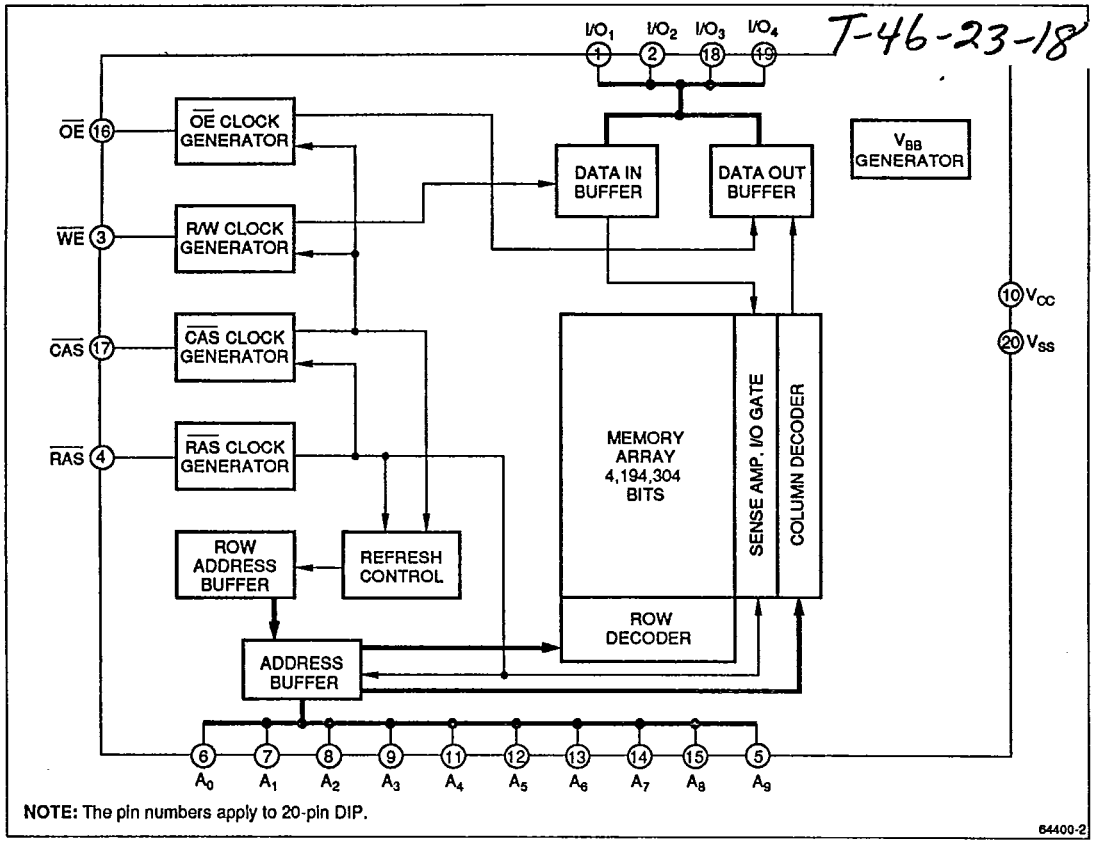

Figure 2. LH64400 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_9	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_{OS}	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

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RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8	V	1

NOTE:
1. Referenced to Vss

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH64400-80	I_{CC1}	—	95	mA	1, 2, 3
	LH64400-10		—	85		
Supply current in standby mode		I_{CC2}	—	1.0	mA	1
Average supply current in high speed page mode	LH64400-80	I_{CC3}	—	70	mA	1, 2
	LH64400-10		—	60		
Average supply current in $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	LH64400-80	I_{CC6}	—	95	mA	1, 2, 3
	LH64400-10		—	85		
Average supply current in $\overline{RAS}$ only refresh cycle	LH64400-80	I_{CC7}	—	95	mA	1, 2, 3
	LH64400-10		—	85		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	I_{LI}	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	I_{LO}	-10	10	µA	
Output "High" voltage	I_{OUT} = -5 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7} depend on the cycle time.
3. Address transition occurs when $\overline{RAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_9	C_{IN1}	—	5	pF
	$\overline{RAS}$, $\overline{CAS}$	C_{IN2}	—	5	pF
	$\overline{WE}$, $\overline{OE}$	C_{IN3}	—	5	pF
Input/output capacitance	I/O_1 - I/O_4	C_{OUT1}	—	7	pF

AC CHARACTERISTICS [1,2,3,4] (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%) T-46-23-18

PARAMETER	SYMBOL	LH64400-80		LH64400-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(1) READ CYCLE							
Random read/write cycle time	t_{RC}	140		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	7
Access time from $\overline{CAS}$	t_{CAC}		25		30	ns	7
Access time from column address	t_{AA}		40		50	ns	7
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	7
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address delay time ($\overline{RAS}$)	t_{RAD}	15	40	20	50	ns	5
Column address lead time ($\overline{RAS}$)	t_{RAL}	40		50		ns	
Column address hold time ($\overline{RAS}$)	t_{CAH}	15		20		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		ns	
$\overline{CAS}$ precharge time ($\overline{RAS}$ fall)	t_{CRP}	0		0		ns	
$\overline{CAS}$ delay time ($\overline{RAS}$)	t_{RCD}	20	55	25	70	ns	6
$\overline{CAS}$ lead time ($\overline{RAS}$)	t_{RSL}	25		30		ns	
$\overline{OE}$ command $\overline{RAS}$ lead time	t_{ROL}	0		0		ns	
Output data disable time ($\overline{CAS}$)	t_{OFF}		20		25	ns	
Output data disable time ($\overline{OE}$)	t_{OEZ}		20		25	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
Output data hold time ($\overline{CAS}$)	t_{SOH}	0		0		ns	
Output data hold time ($\overline{OE}$)	t_{OOH}	0		0		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time ($\overline{CAS}$)	t_{RCH}	10		10		ns	8
Read command hold time ($\overline{RAS}$ rise)	t_{RRH}	10		10		ns	8
Transition time (rise and fall)	t_T	3	50	3	50	ns	
Refresh time interval	t_{REF}		16		16	ms	
(2) HIGH SPEED PAGE MODE READ CYCLE							
High speed page mode cycle time	t_{PC}	50		55		ns	
$\overline{CAS}$ precharge time	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge access time ($\overline{CAS}$ rise)	t_{CACP}	45		50		ns	7, 10
$\overline{RAS}$ pulse width	t_{RASP}	80	10,000	100	10,000	ns	
High speed page mode read write cycle time	t_{PRWC}	105		115		ns	11
(3) WRITE CYCLE EARLY WRITE)							
Data input setup time	t_{DS}	0		0		ns	
Data input hold time	t_{DH}	15		15		ns	
Write command set-up time	t_{WCS}	0		0		ns	9
Write command hold time	t_{WCH}	10		15		ns	
($\overline{OE}$ CONTROL)							
$\overline{CAS}$ set-up time ($\overline{WE}$)	t_{CWS}	0		0		ns	9
Write command lead time ($\overline{RAS}$)	t_{RWL}	20		25		ns	
Write command lead time ($\overline{CAS}$)	t_{CWL}	20		25		ns	
Write pulse width ($\overline{WE}$)	t_{WP}	15		15		ns	
OE hold time ($\overline{WE}$)	t_{OEH}	20		20		ns	
(4) READ-WRITE CYCLE							
Read-write cycle time	t_{RWC}	195		225		ns	11
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	110		135		ns	11
Column address delay time ($\overline{WE}$)	t_{AWD}	70		85		ns	11
$\overline{WE}$ delay time ($\overline{CAS}$)	t_{CWD}	55		65		ns	11
$\overline{OE}$ delay time	t_{OED}	20		25		ns	
($\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE/HIDDEN REFRESH CYCLE							
$\overline{CAS}$ set-up time ($\overline{RAS}$)	t_{CSR}	0		0		ns	
$\overline{CAS}$ hold time ($\overline{RAS}$)	t_{CHR}	20		20		ns	
$\overline{RAS}$/$\overline{CAS}$ precharge time ($\overline{RAS}$ rise)	t_{RPC}	10		10		ns	
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0		0		ns	
$\overline{WE}$/$\overline{RAS}$ hold time	t_{WRH}	10		10		ns	
$\overline{CAS}$ precharge time ($\overline{RAS}$ fall)	t_{CPN}	10		10		ns	

* See next page for notes.

NOTES:

1. For proper operation, at least 200 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristic assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. I_{CC} when power on depends on $\overline{RAS}$ input level.
   If $\overline{RAS}$ = V_{IL} when power on, LSI goes into an active cycle and may have a large current I_{CC}. It is recommended to rise $\overline{RAS}$ with V_{CC} or fix at V_{IH} when power on.
5. t_{RCD} (MAX.), is the maximum point for t_{RAD} where t_{AA} (Max.) is ensured, and does not represent a limit of operation.
   If $t_{RAD} \geq t_{RAD}$ (MAX.), the access time comes under the control of t_{AA}.
6. t_{RCD} (MAX.), is the maximum point for t_{RAD} where t_{CAC} (MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time will come under the control of t_{CAC}.
7. 2TTL + 100 pF load.
8. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
9. t_{WCS} is not a restrictive operating parameter. It comes into early write cycle with the WE = "Low" at the falling edge of $\overline{CAS}$. Then, I/O pins remain inactive until the $\overline{CAS}$ = "High" irrespective of $\overline{WE}$.
10. If $t_{CACP} \geq t_{CP} + t_{CAC} + t_T$, the access time depends upon t_{CACP}.
11. t_{RWC}, t_{RWD}, t_{AWD}, t_{CWD} and t_{PRWC} are not restrictive operating parameters.

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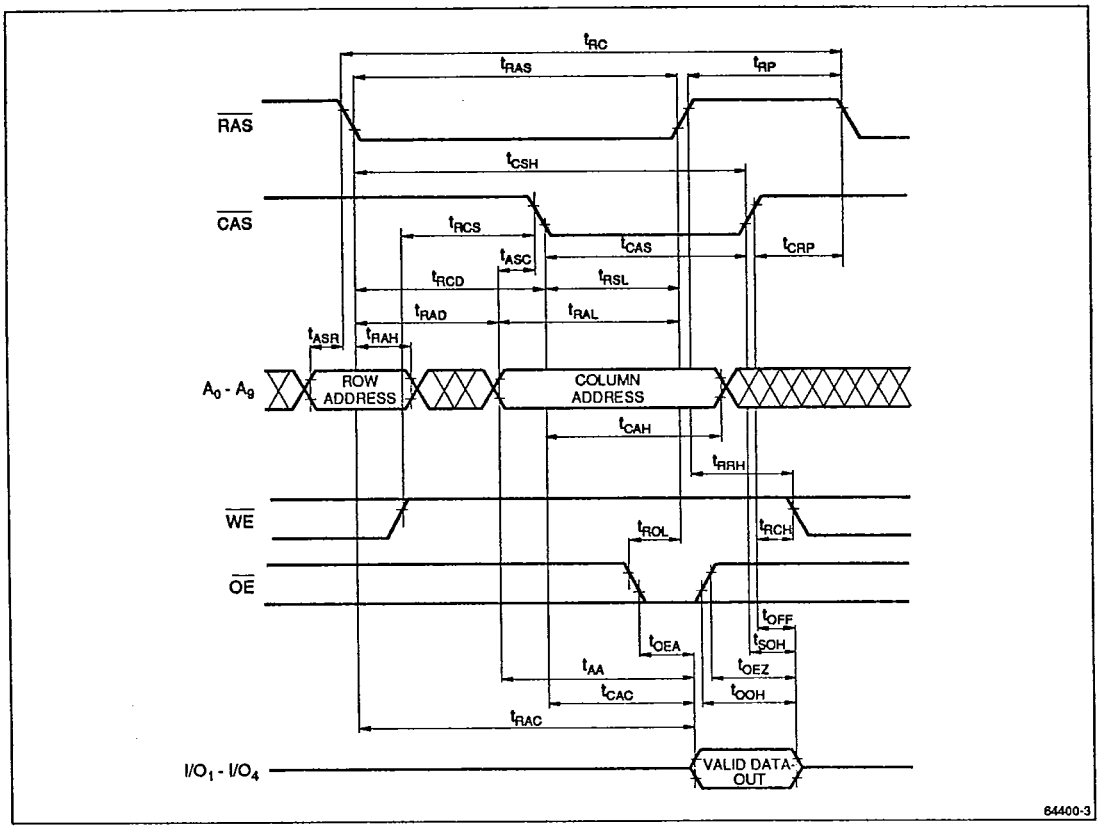

Figure 3. Read Cycle

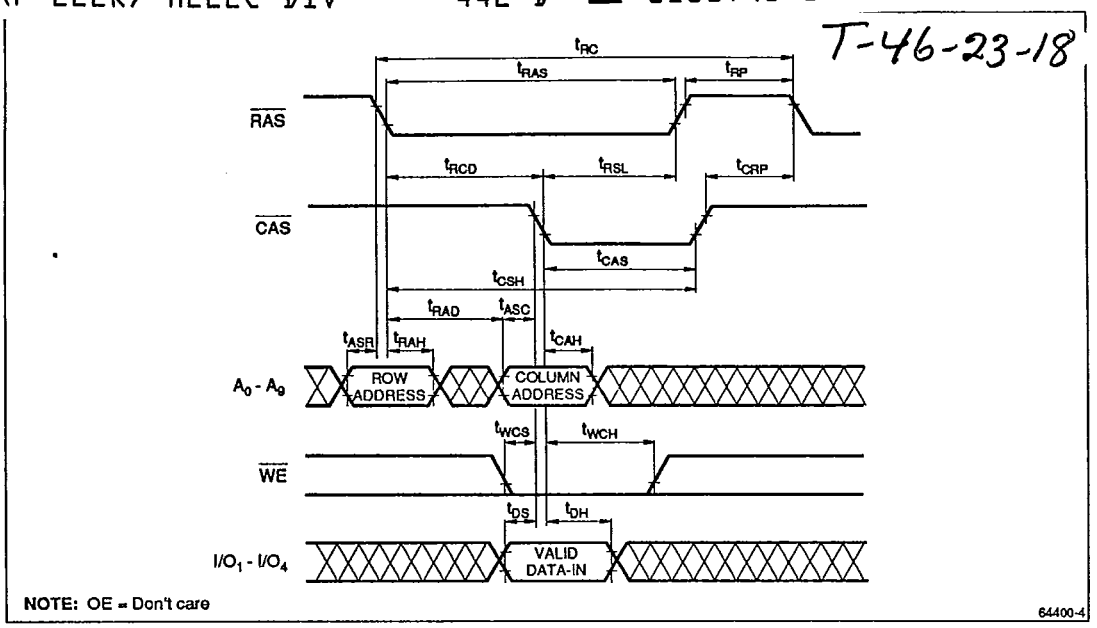

Figure 4. Write Cycle (Early Write)

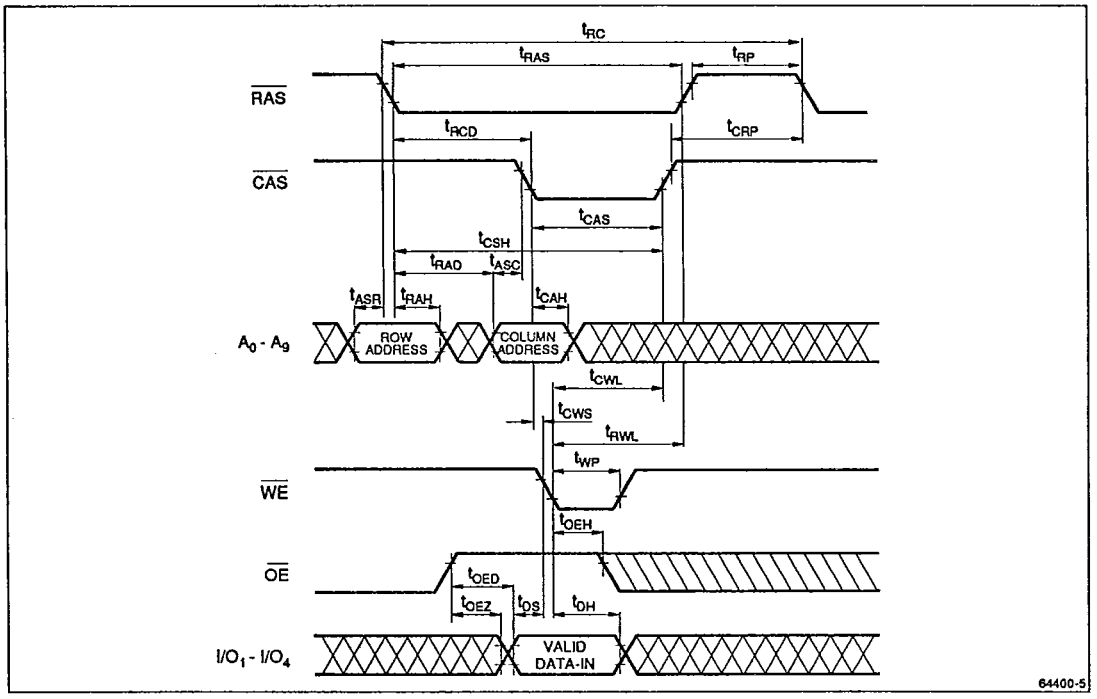

Figure 5. Write Cycle ($\overline{OE}$ Control)

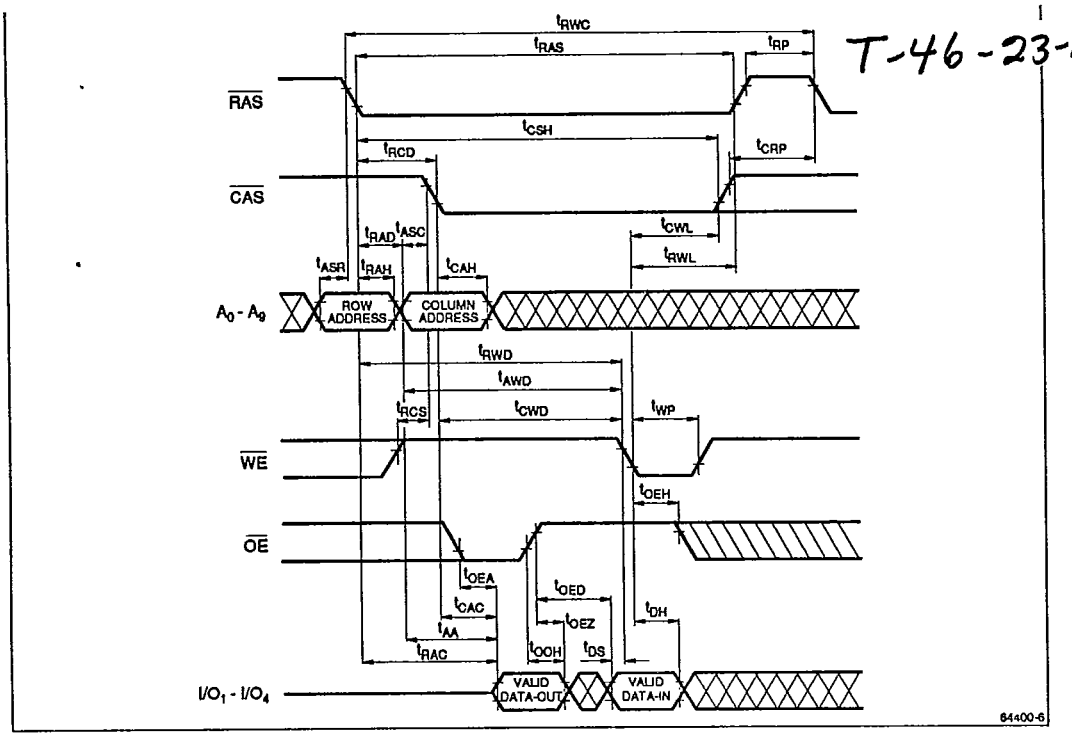

Figure 6. Read/Write Cycle

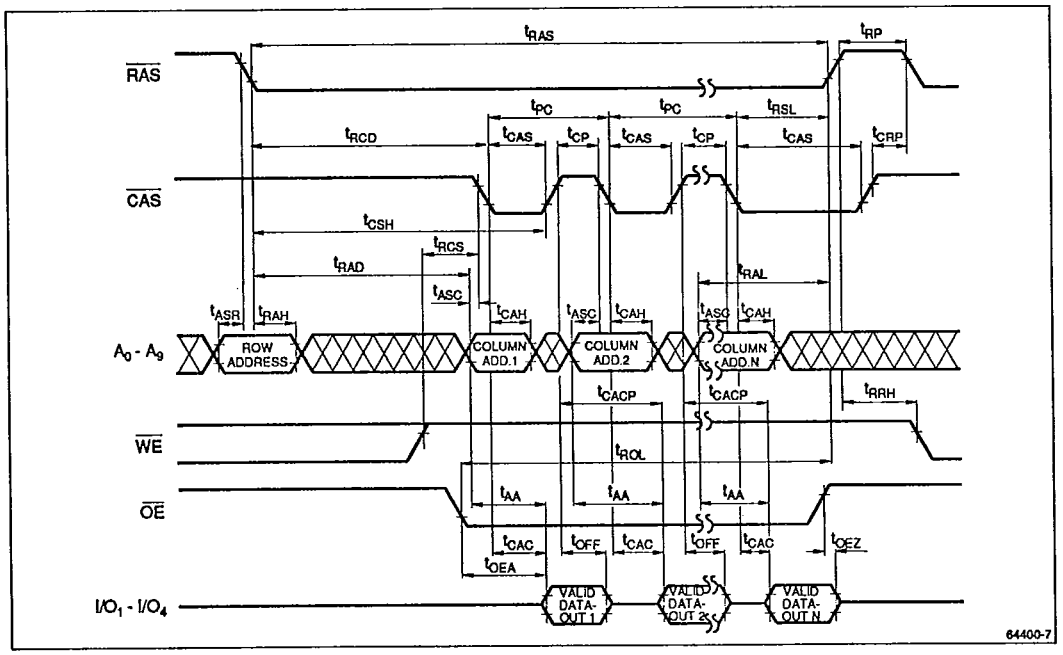

Figure 7. High Speed Page Mode Read Cycle

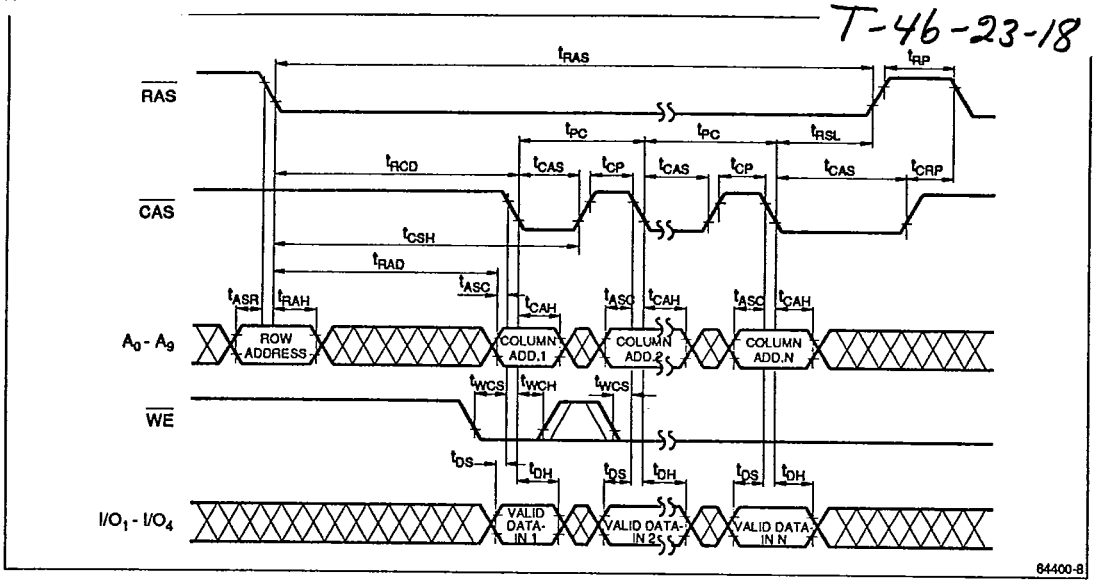

Figure 8. High Speed Page Mode Write Cycle

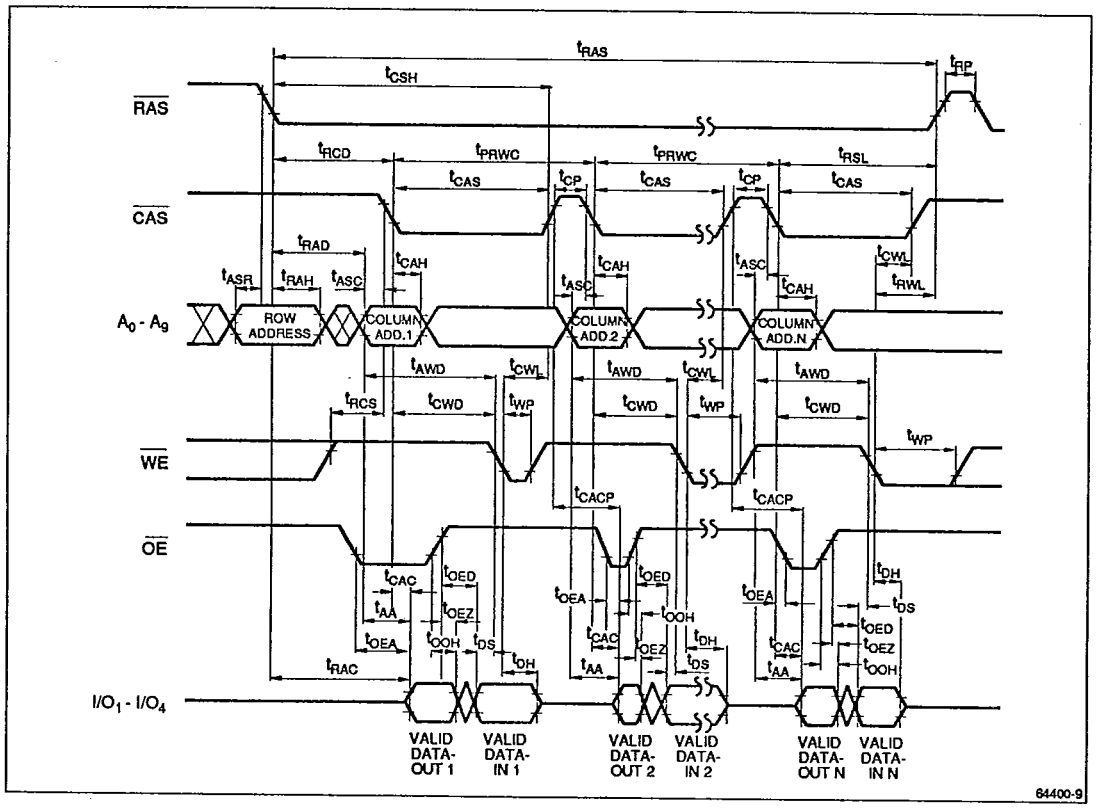

Figure 9. High Speed Page Mode Write Cycle

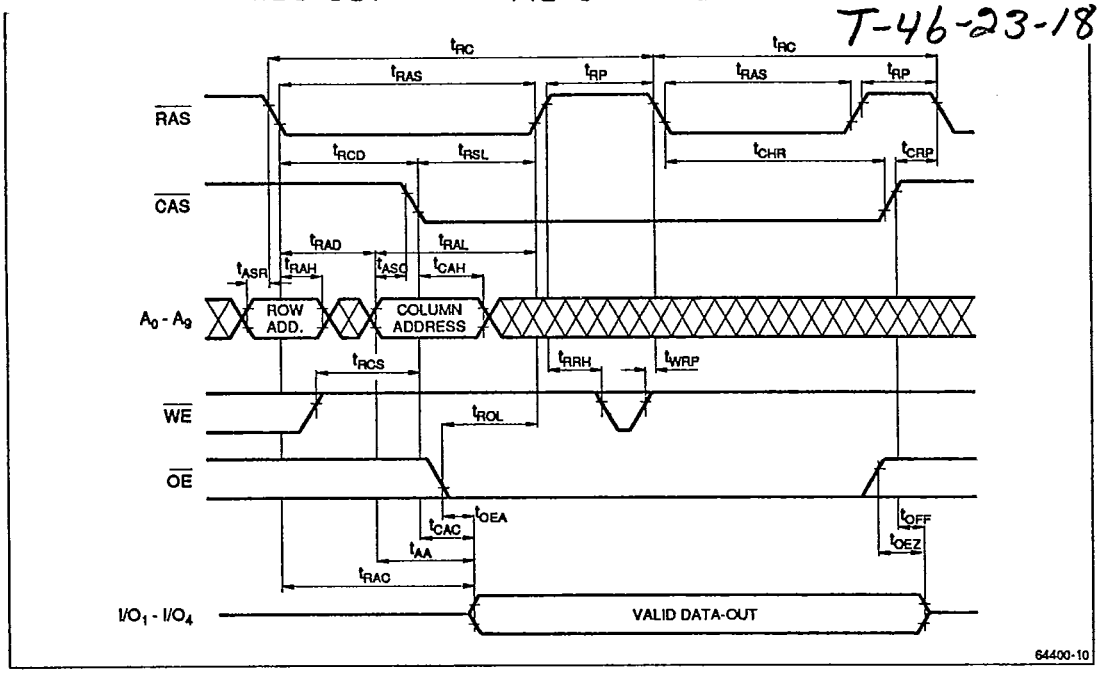

Figure 10. Hidden Refresh Cycle

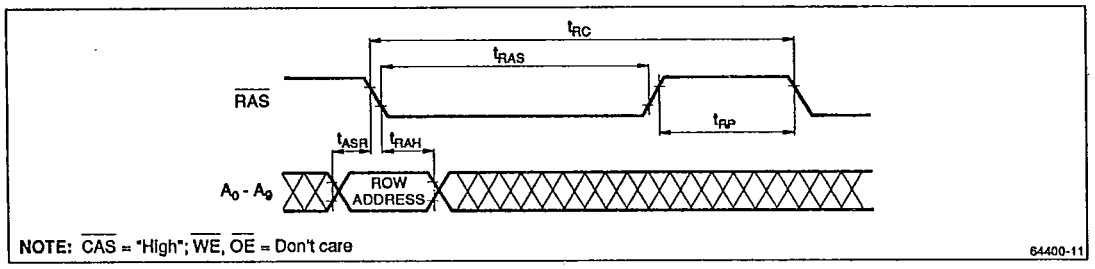

Figure 11. $\overline{RAS}$ Only Refresh Cycle

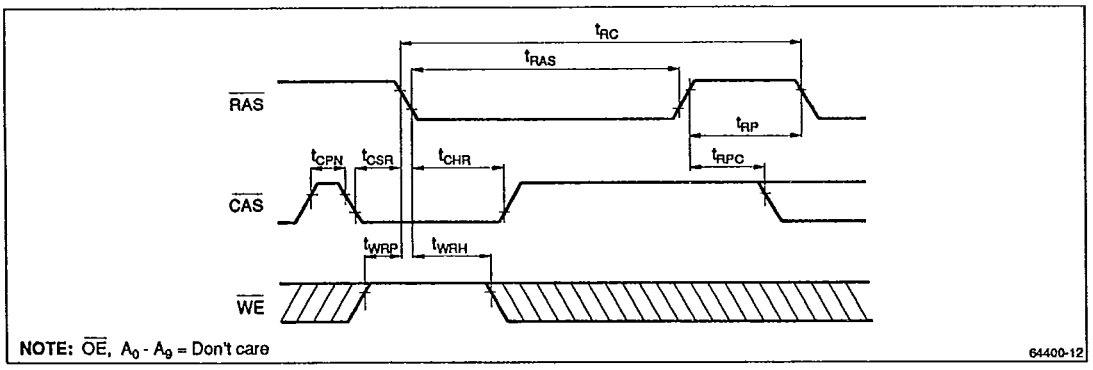

Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

ORDERING INFORMATION

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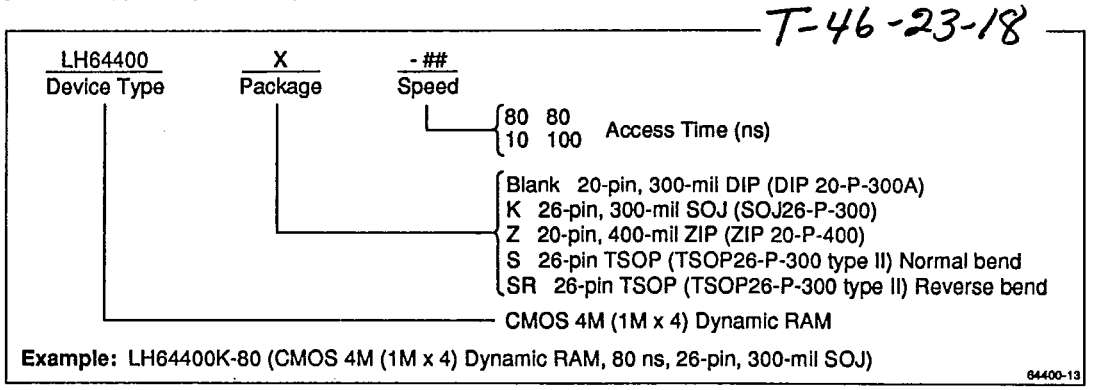

Example: LH64400K-80 (CMOS 4M (1M x 4) Dynamic RAM, 80 ns, 26-pin, 300-mil SOJ)

64400-13