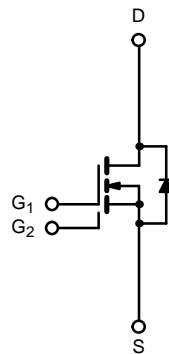
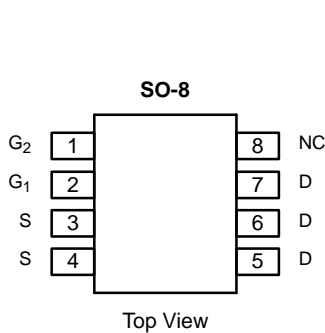




N-Channel 30:1 Ratio Dual-Gate 30-V (D-S) MOSFET

TrenchFET[®]
Power MOSFETs

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
Gate 1	30	0.022 @ $V_{GS} = 10$ V	± 7.7
		0.03 @ $V_{GS} = 4.5$ V	± 6.4
Gate 2		0.25 @ $V_{GS} = 10$ V	± 2.0
		0.40 @ $V_{GS} = 4.5$ V	± 1.5



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Gate 1	Gate 2	Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 7.7	± 6.4
		$T_A = 70^\circ\text{C}$	± 4.4	± 6.0
Pulsed Drain Current	I_{DM}	± 40	± 4.0	A
Continuous Source Current (Diode Conduction) ^a	I_S	2		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.3	
		$T_A = 70^\circ\text{C}$	1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	55	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.



SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1			V	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			5		
On-State Drain Current ^a	I _{D(on)}	(G ₁ = G ₂) V _{DS} = 5 V, V _{GS} = 10 V	40			A	
Drain-Source On-State Resistance ^a	r _{DS1(on)}	(G ₁ = G ₂) V _{GS} = 10 V, I _D = 7.7 A		0.017	0.022	Ω	
		(G ₁ = G ₂) V _{GS} = 4.5 V, I _D = 6.4 A		0.021	0.03		
	r _{DS2(on)}	V _{G1S} = 0 V, V _{G2S} = 10 V, I _D = 2.0 A		0.20	0.25		
		V _{G1S} = 0 V, V _{G2S} = 4.5 V, I _D = 0.3 A		0.30	0.40		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 7.7 A		21		S	
Diode Forward Voltage ^a	V _{SD}	I _S = 2 A, V _{GS} = 0 V		0.72	1.1	V	
Dynamic^b							
Total Gate Charge	Q _g	Gate 1 V _{DS} = 15 V, V _{GS(1,2)} = 10 V I _D = 7.7 A Gate 2 V _{DS} = 15 V, V _{GS(1)} = 0 V V _{GS(2)} = 10 V, I _D = 2.0 A	Gate 1		34	60	nC
			Gate 2		2.2	5	
Gate-Source Charge	Q _{gs}		Gate 1		6.5		
			Gate 2		0.5		
Gate-Drain Charge	Q _{gd}		Gate 1		5.2		
			Gate 2		0.28		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		12	15	ns	
Rise Time	t _r			9	20		
Turn-Off Delay Time	t _{d(off)}			55	80		
Fall Time	t _f			15	30		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs		40	60		

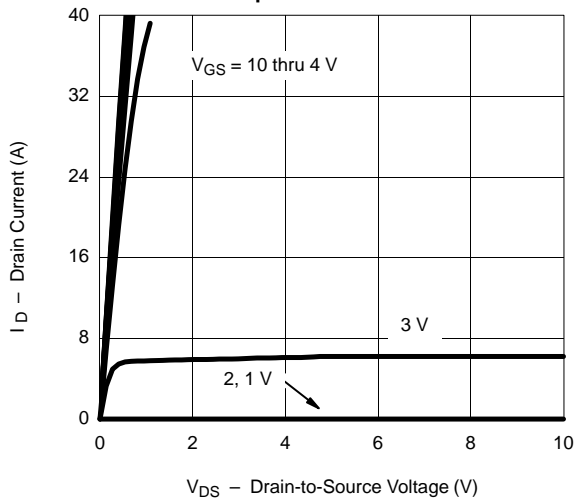
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

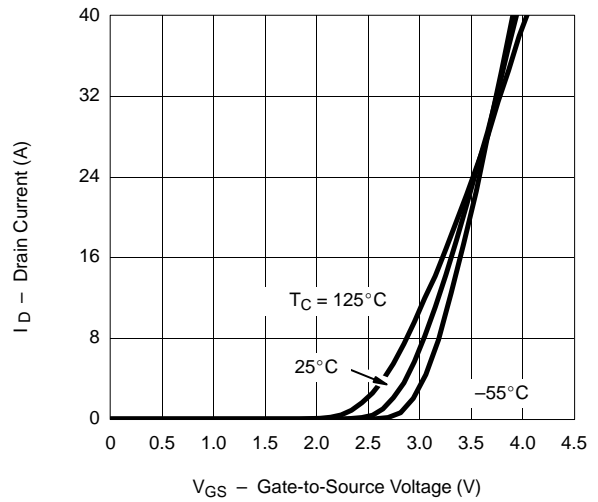


TYPICAL CHARACTERISTICS ($V_{G1} = V_{G2}$, 25°C UNLESS NOTED)

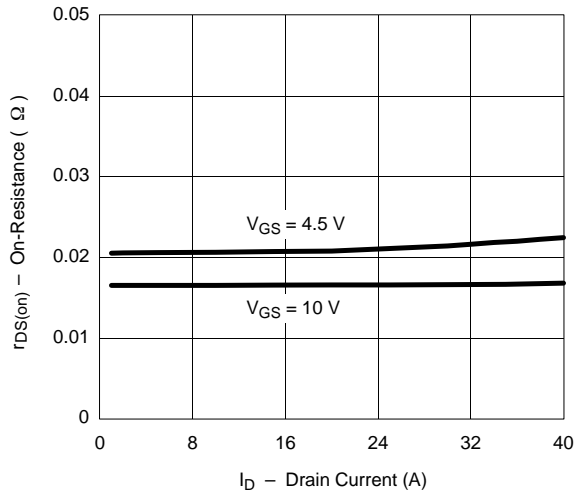
Output Characteristics



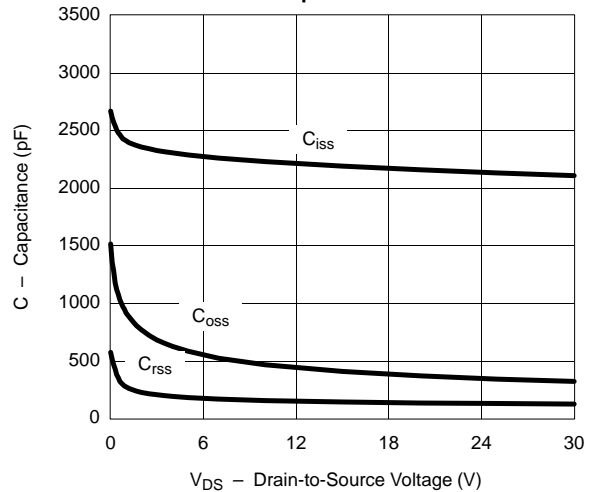
Transfer Characteristics



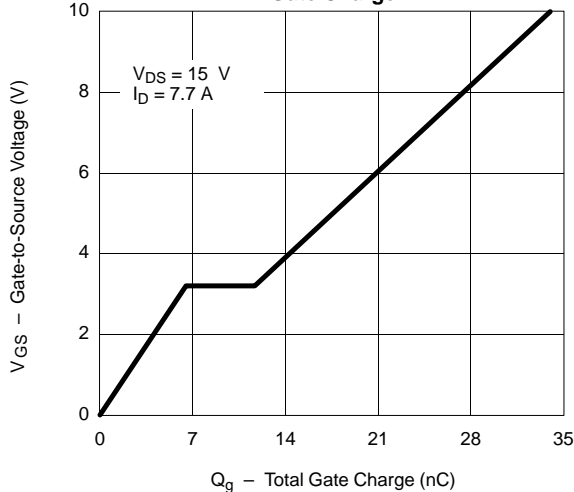
On-Resistance vs. Drain Current



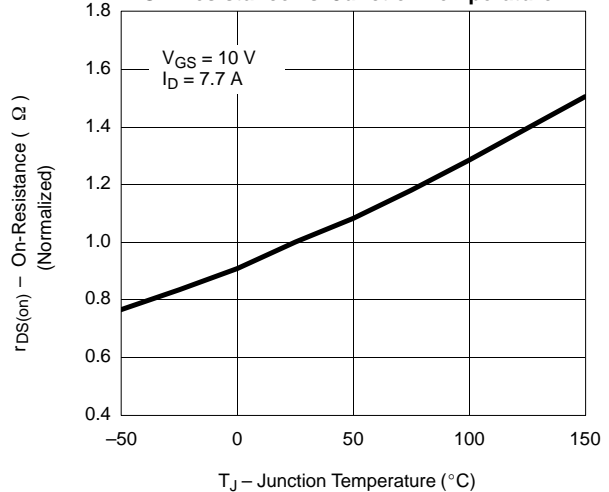
Capacitance



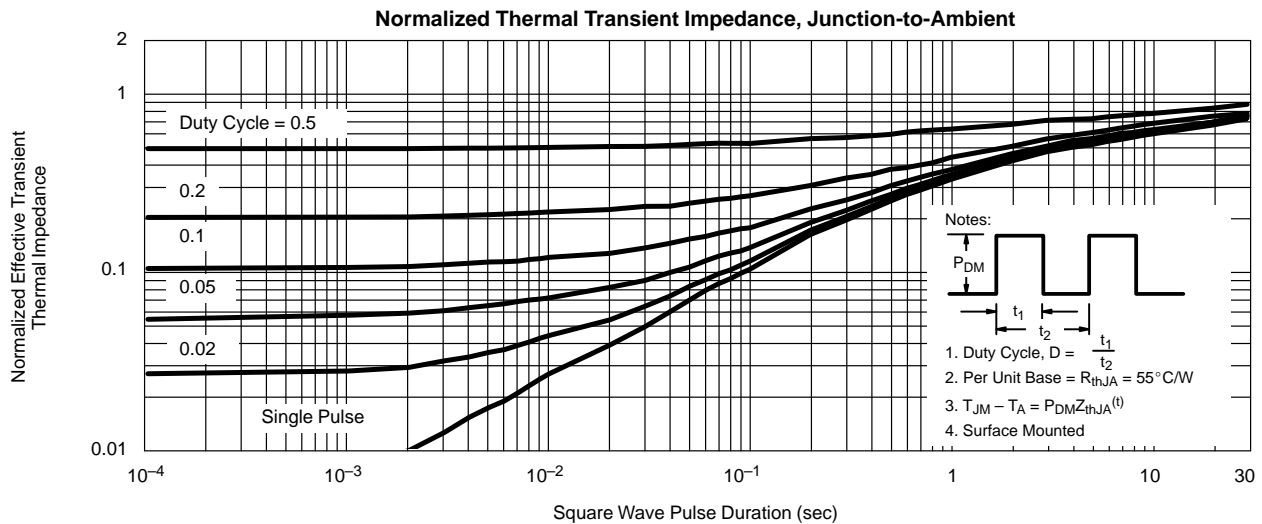
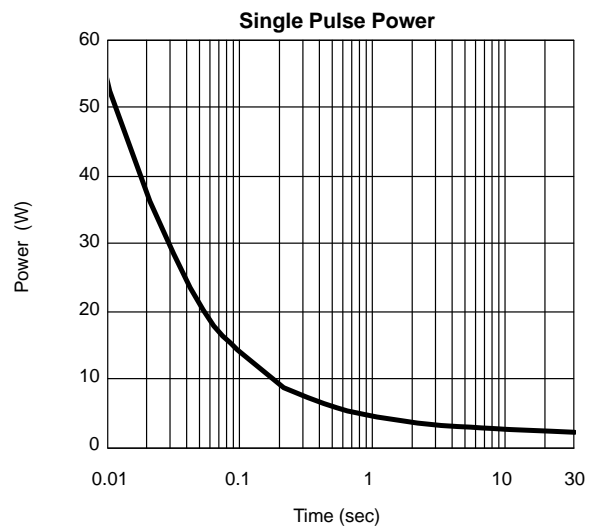
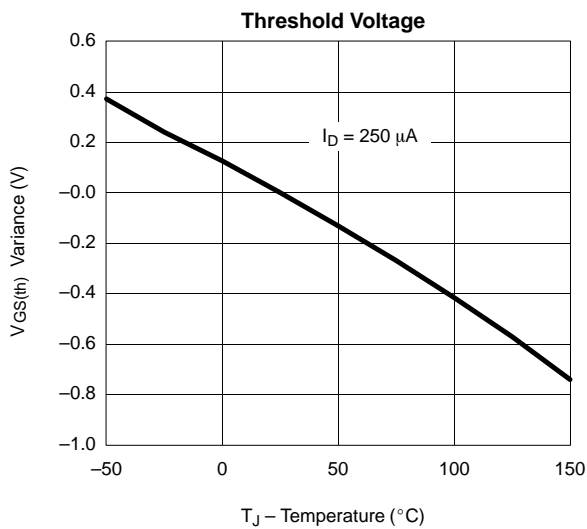
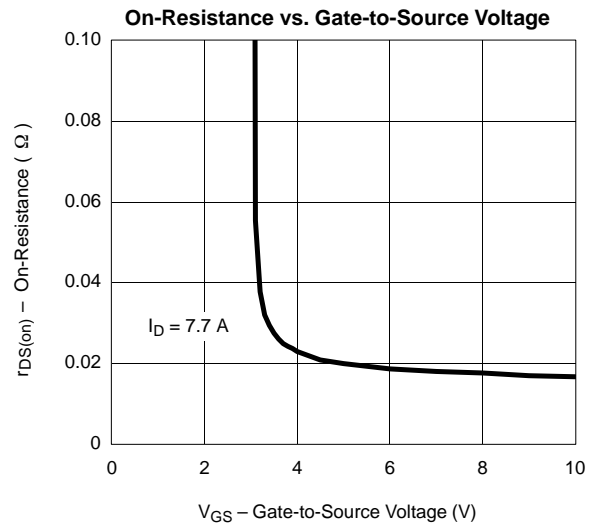
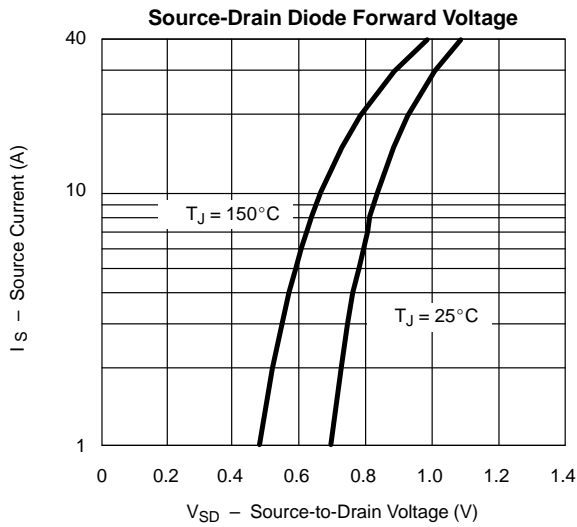
Gate Charge



On-Resistance vs. Junction Temperature



TYPICAL CHARACTERISTICS ($V_{G1} = V_{G2}$, 25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS ($V_{G1} = 0\text{ V}$, 25°C UNLESS NOTED)

