

H/V PROCESSOR FOR TTL V.D.U

HORIZONTAL SECTION

- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 15kHz to 100kHz
- HORIZONTAL OUTPUT PULSE SHAPER AND SHIFTER
- PHASE COMPARATOR BETWEEN SYNCHRO AND OSCILLATOR (PLL1)
- PHASE COMPARATOR BETWEEN FLYBACK AND OSCILLATOR (PLL2)
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR PHASE AND FREQUENCY

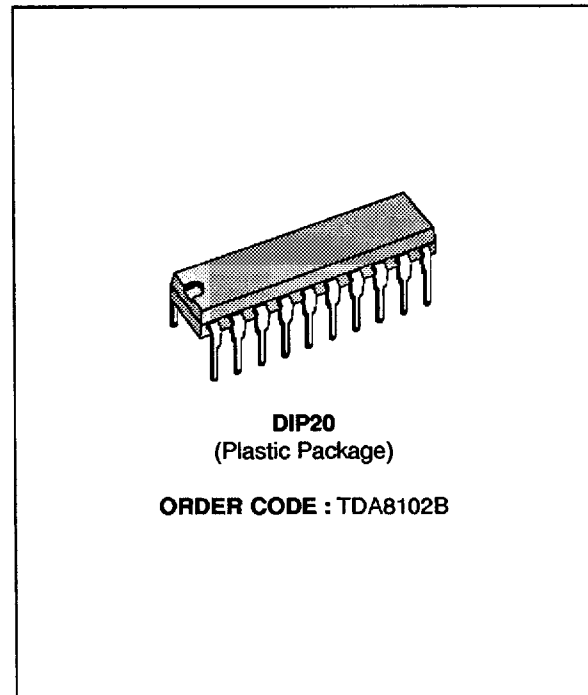
VERTICAL SECTION

- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 30Hz to 120Hz
- RAMP GENERATOR WITH VARIABLE GAIN STAGE
- VERTICAL RAMP VOLTAGE REFERENCE
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR FREQUENCY, AMPLITUDE AND LINEARITY

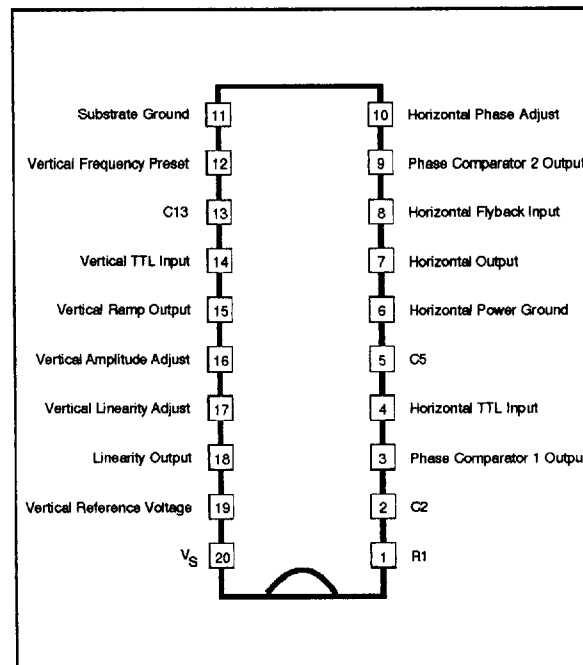
DESCRIPTION

The TDA8102B is a monolithic integrated circuit for horizontal and vertical sync processing in monochrome and color video displays driven by input TTL compatible signals.

The TDA8102B is supplied in a 20 pin dual in line package with pin 11 connected to ground and used for heatsinking.

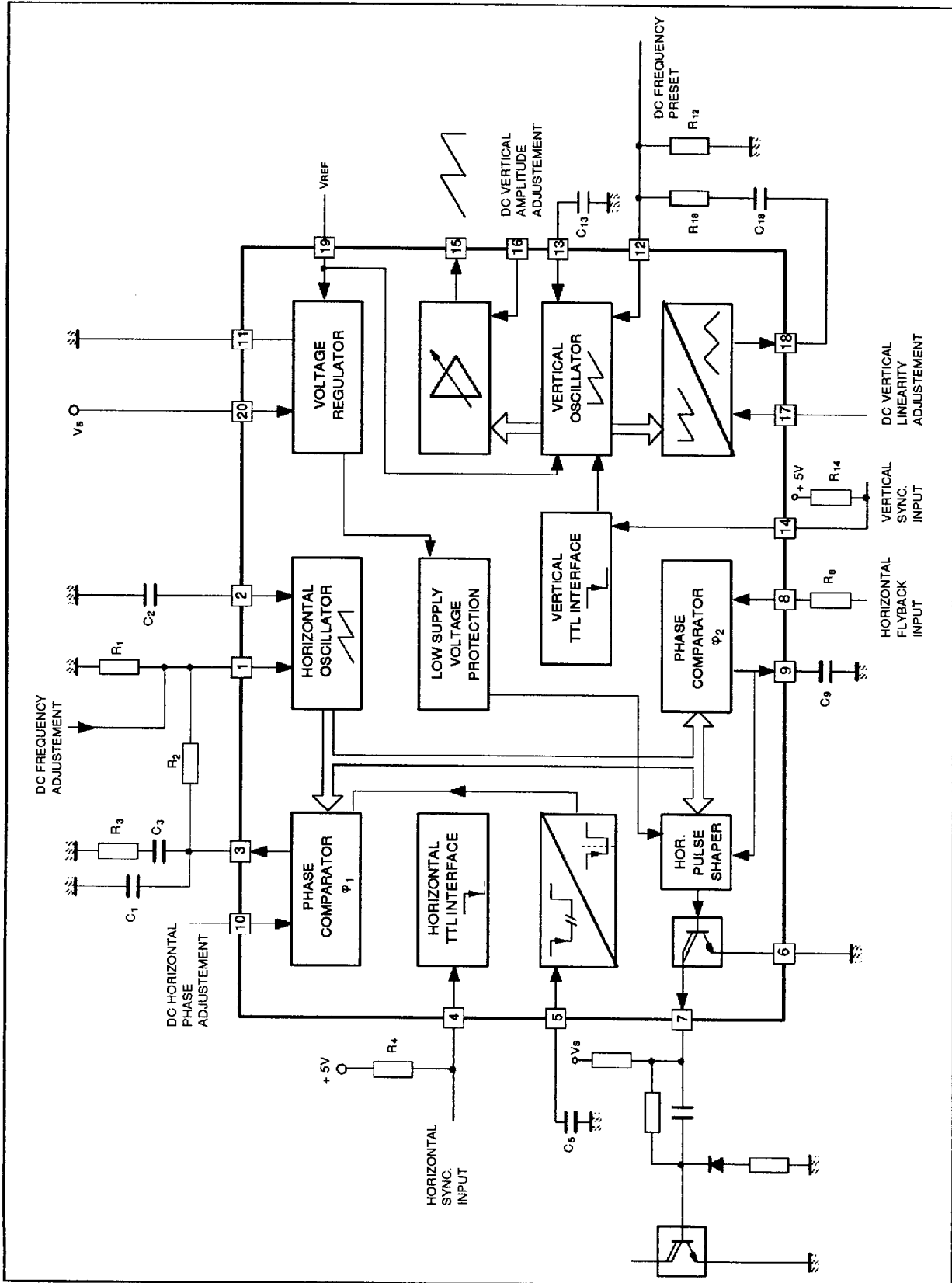


PIN CONNECTIONS



8102B-01 LEPS

BLOCK DIAGRAM



8102B-02 EFS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	18	V
V _{SYNC}	Sync Input Peak Voltage	+ V _S	V
I _{OH}	Output Sinking Peak Current (Pin 7 ; t < 3μs)	2	A
I ₁₅	Output current (Pin 15)	- 10	mA
I ₁₉	Output Current (Pin 19)	- 10	mA
P _{TOT}	Total Power Dissipation T _{amb} < 70°C T _{pin} < 90°C	1.4	W
		1.5	W
T _{STG} , T _J	Storage and Junction Temperature	- 40, +150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
R _{TH(J-C)}	Junction-case Thermal Resistance	40	°C/W
R _{TH(J-A)}	Junction-ambient Thermal Resistance	55	°C/W

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ELECTRICAL CHARACTERISTICS

(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
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HORIZONTAL SECTION

V _S	Supply voltage range		10.5	12	15.5	V
I _S	Supply current			50	70	mA
V ₁	Voltage reference at Pin 1	I ₁ = 0.5mA	3.2	3.5	3.8	V
I ₁	Current at Pin 1		- 1			mA
V ₂	Voltage swing at Pin 2			4		V _{PP}
K ₀	Free running frequency constant	f ₀ = 1/(K ₀ × R ₁ × C ₂)	2.8	3.04	3.2	
V ₃ - V ₁	Control voltage range	(See technical note 1)		2.5		V
I ₃	Peak control current			3		mA
K ₃	Gain phase comparator φ1 K ₃ = 2 × I ₃ / 360			16.6		$\frac{\mu A}{\text{degree}}$
V ₄	Sync threshold input (neg. edge)	Sync high Sync low	2		8 0.8	V V
I ₄	Current at Pin 4	Input high Input low	- 10		10	μA μA
T ₄	Input pulse duration T = 1/f _H		1		0.9T	μs
V ₅	Monostable threshold		5.7	6	6.3	V
t ₅	Internal pulse width t ₅ = C ₅ × V ₅ / I ₅	C ₅ = 220 pF (see technical note 2)		3.6		μs
t ₇	Output pulse duration (low) - T = 1/f _H	@ f _H = 27 kHz @ f _H = 100 kHz		0.33T 0.25T		μs μs
V _{7 sat}	Output Saturation Voltage	I ₇ = 600 mA		1.2	2.5	V
t _D	Permissible delay between output pulse leading edge and flyback pulse leading edge (for keeping a constant duty cycle) ; T = $\frac{1}{f_H}$	See technical note 4		0.30 T - t _{FLY}		s
V _{FLY}	Flyback threshold voltage at Pin 8		0.6	0.7	0.9	V
I _{FLY}	Flyback input current at Pin 8	Flyback On Flyback Off	0.6 -1		2	mA mA
V ₈	Clamp voltage at Pin 8	I ₈ = 1mA I ₈ = -1mA	0.6		- 0.6	V V
I ₈	Current for switching low the output pulse		0.7		2	mA

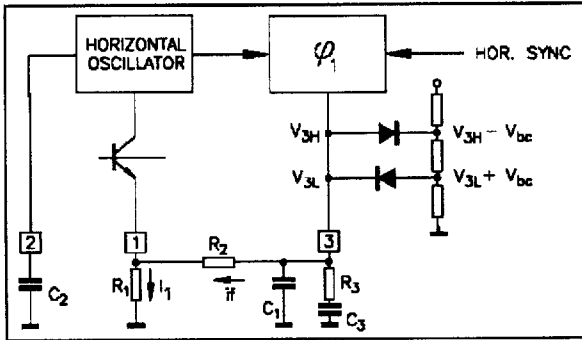
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ELECTRICAL CHARACTERISTICS(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SECTION						
K ₉	Phase sensitivity at Pin 9	(See technical note 3)		67.5		$\frac{\text{degree}}{\text{V}}$
V ₁₀	Control voltage range		0.5		4.5	V
K ₁₀	Phase control sensitivity at Pin 10		20	22.5	30	$\frac{\text{degree}}{\text{V}}$
	Horizontal phase adjustment	Zero degree phase: flyback centered on the center of the pulse at Pin 5	- 45		+ 45	degree
K ₁	Phase jitter constant (jitter = $\frac{K_1}{10^6 \cdot f_H}$)			100	150	ppm
K ₂	Frequency drift versus supply voltage $K_2 = \frac{dF \cdot 10^6}{dV \cdot f_H}$	V _S = 10.5V to 15.5V			2000	$\frac{\text{ppm}}{\text{V}}$
VERTICAL SECTION						
V ₁₂	Voltage reference at Pin 12		3.2	3.5	3.8	V
$\frac{I_{13}}{I_{12}}$	Current gain at Pin 13			1		
V ₁₃	Vertical ramp amplitude			4		V _{PP}
t _{FALL}	Discharge time at Pin 13	C ₁₈ = 0.22 μF V ₁₃ = 4V _{PP}		10	22	μs
K ₁₄	Synchro window constant $t_s = \frac{K_{14}}{f_V}$	(See technical note 6)		0.333		
V ₁₄	Sync input threshold (negative edge)	● Sync high ● Sync Low	2		8 0.8	V V
I ₁₄	Current at Pin 14	● Input high ● Input Low	- 10		10	μA μA
t ₁₄	Input pulse duration $T = \frac{1}{f_V}$		10		0.5T	μs
V ₁₅	Average value of voltage on Pin 15	V ₁₃ = 4V _{PP} V ₁₆ = 2.5V		4		V
I _{15I}	Output current at Pin 15				1	mA
K ₁₅	Buffer gain constant at Pin 15 V _{15PP} = K ₁₅ · V _{13PP}	V ₁₆ = 2.5V		1		
K ₁₆	Buffer variable gain constant at Pin 15 $K_{16} = \frac{\Delta V_{15PP}}{\Delta V_{16} \cdot V_{13PP}}$	2.5V < V ₁₆ < 4.5V 0.5V < V ₁₆ < 2.5V		0.1		V ⁻¹
I ₁₆	Input bias current at Pin 16	V ₁₆ = 0.5V	- 50			μA
I ₁₇	Input bias current at Pin 17	V ₁₇ = 4.5V			50	μA
V ₁₈	Average voltage at Pin 18 : V ₁₈ = 2 + $\frac{V_{18PP}}{2}$	V ₁₇ = 3.5V R ₁₈ not connected		3		V
K ₁₈	Linearity correction constant $K_{18} = \frac{\Delta V_{18PP}}{\Delta V_{17}}$	V _{13PP} = 4V, 1.5V < V ₁₇ < 4.5V		1		
V ₁₉	Voltage reference at Pin 19	(See technical note 5)	7.6	8	8.2	V
I ₁₉	Current at Pin 19				2	mA
K ₁₇	Frequency drift versus supply voltage $K_{17} = \frac{dF \cdot 10^6}{dV \cdot f_V}$	V _S = 10.5V to 15.5V			4500	$\frac{\text{ppm}}{\text{V}}$

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Technical Note 1



$f_H (nom) = 26.8 \text{ kHz}$

$R1 = 6.8 \text{ k}\Omega$

$R2 = 56 \text{ k}\Omega$

$C2 = 1.8 \text{ nF}$

$$f_{pull-in} = f_H (nom) \frac{|V_3 - V_1| / R2}{V_1 / R1} = f_H (nom) \frac{I_f}{I_o} \quad (A)$$

where: $V_1 = 3.5\text{V}$ and $|V_3 - V_1|$ is the control voltage range.

The voltage at Pin 3 is limited by two clamping diodes at the voltage V_{3H} and V_{3L} .

When the PLL1 is synchronized and perfectly tuned, $V_3 = V_1$.

Remark: The value of C2 influences the horizontal oscillator free running frequency; it doesn't effect the pull-in range. If the horizontal frequency is changed by using R1, the pull-in range changes accordingly with the formula (A).

Technical Note 2

The internal pulse "t_s", is generated by the current generator "I₅" charging the external capacitor "C5", according with the formula (B):

$$t_s = \frac{C5 \cdot V_5}{I_5} \quad (B), \quad t_s = \frac{T_H}{12} \quad \text{is recommended.}$$

Technical Note 3

$K_G = 67.5$ degrees/volt represents the slope of the oscillator charging period of the waveform at

Pin 2:

$$K_G = \frac{360 \times 0.75}{4} \frac{\text{degree}}{\text{V}}$$

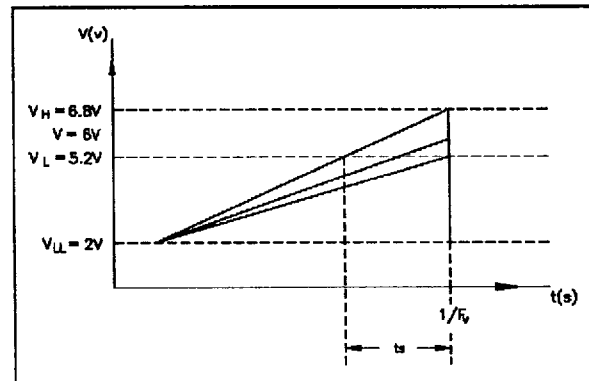
Technical Note 4

The second PLL can recover the storage of horizontal output stage maintaining a constant duty cycle till the trailing edge of the output pulse gets the trailing edge of the flyback pulse. From this point on, only the leading edge of the output pulse will be shifted covering a total phase shift of: $0.30T$; overcoming this value, it will produce a notch in the output pulse (@ $f_H = 27\text{kHz}$).

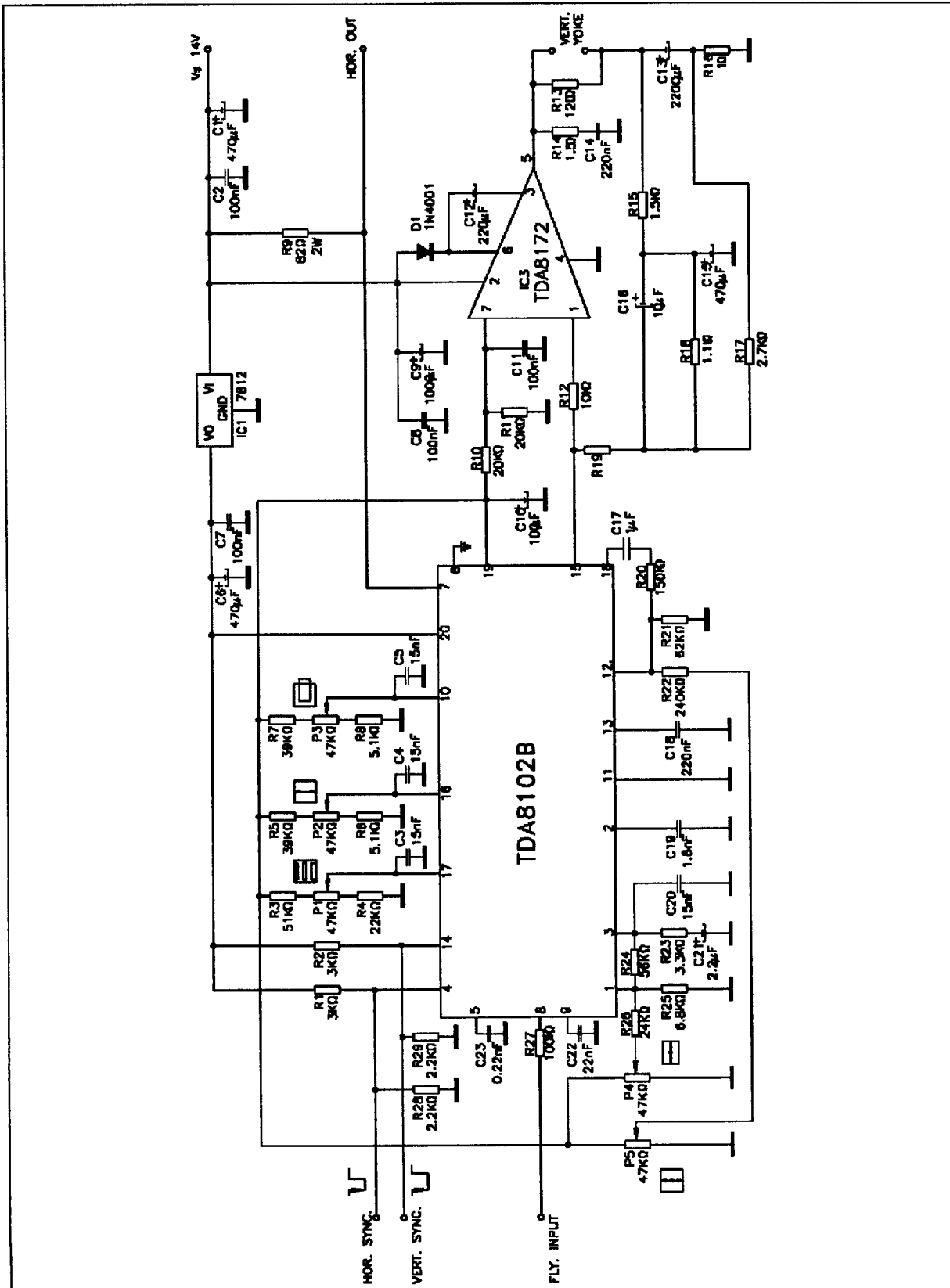
Technical Note 5

The voltage reference at Pin 19 can be used to polarize the DC operating point of the vertical booster. This voltage corresponds to the double of the mean value voltage of the vertical sawtooth at Pin 13.

Technical Note 6

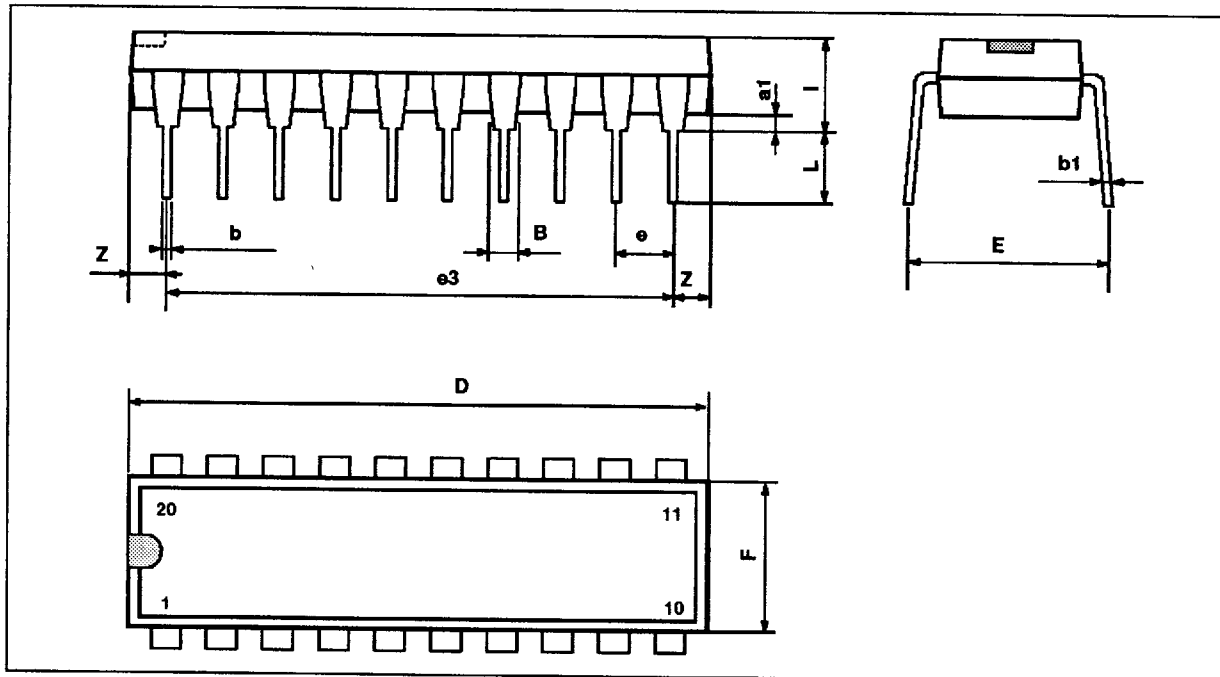


APPLICATION DIAGRAM (with TDA8172)



8102B-05-EPS

PACKAGE MECHANICAL DATA
20 PINS - PLASTIC DIP



PM-DIP20.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45		0.018		
b1		0.25		0.010		
D			25.4			1.000
E		8.5		0.335		
e		2.54		0.100		
e3		22.86		0.900		
F			7.1			0.280
i			3.93			0.155
L		3.3		0.130		
Z			1.34			0.053

DIP20.TBL

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