AN-684

Fairchild Semiconductor
Application Note
February 1990
Revised May 2000

FAIRCHILD SEMICONDUCTOR™

100336 Four-Stage Counter/Shift Register

INTRODUCTION

Many system designs require bi-directional counting and shifting functions. In most cases these functions are separate and unique requirements within the system design. For this reason, separate catalog parts are available. In some cases however, there is a requirement to have a device that will allow both counting and shifting functions. This is especially true in arithmetic, timing, sequential, or communication applications. Fairchild offers a very versatile counter/shift register in the 100336. This application note describes its function in detail and offers some simple uses.

DESCRIPTION

The 100336 contains four synchronous, presettable flip-flops. Synchronous operation is provided by having all flip-flops clocked simultaneously so that all output changes coincide. This mode of operation eliminates counting spikes on the outputs which are normally associated with asynchronous counters. The clock input is buffered and triggers the four flip-flops on the rising (positive-going) edge.

The counters are fully programmable allowing the outputs to be set to either a HIGH (1) or LOW (0). As presetting is synchronous, setting low levels on the select inputs (S_0-S_2) (see Table 1) disables the counter and causes the outputs to agree with the parallel inputs (P_3–P_0) on the next rising edge of the clock. Loading is accomplished regardless of the levels of the two enables ($\overline{CEP}$, $\overline{CET}$).

TABLE 1. Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

The 100336 features both synchronous and asynchronous clear functions. The synchronous clear is performed by setting a binary five (101B) at the select inputs. On the next rising edge of the clock, the outputs will be forced LOW (0000) regardless of the levels at the enable inputs. A buffered asynchronous master reset (MR) is provided to clear all outputs LOW (0000) regardless of the levels of the clock, select, or enable inputs.

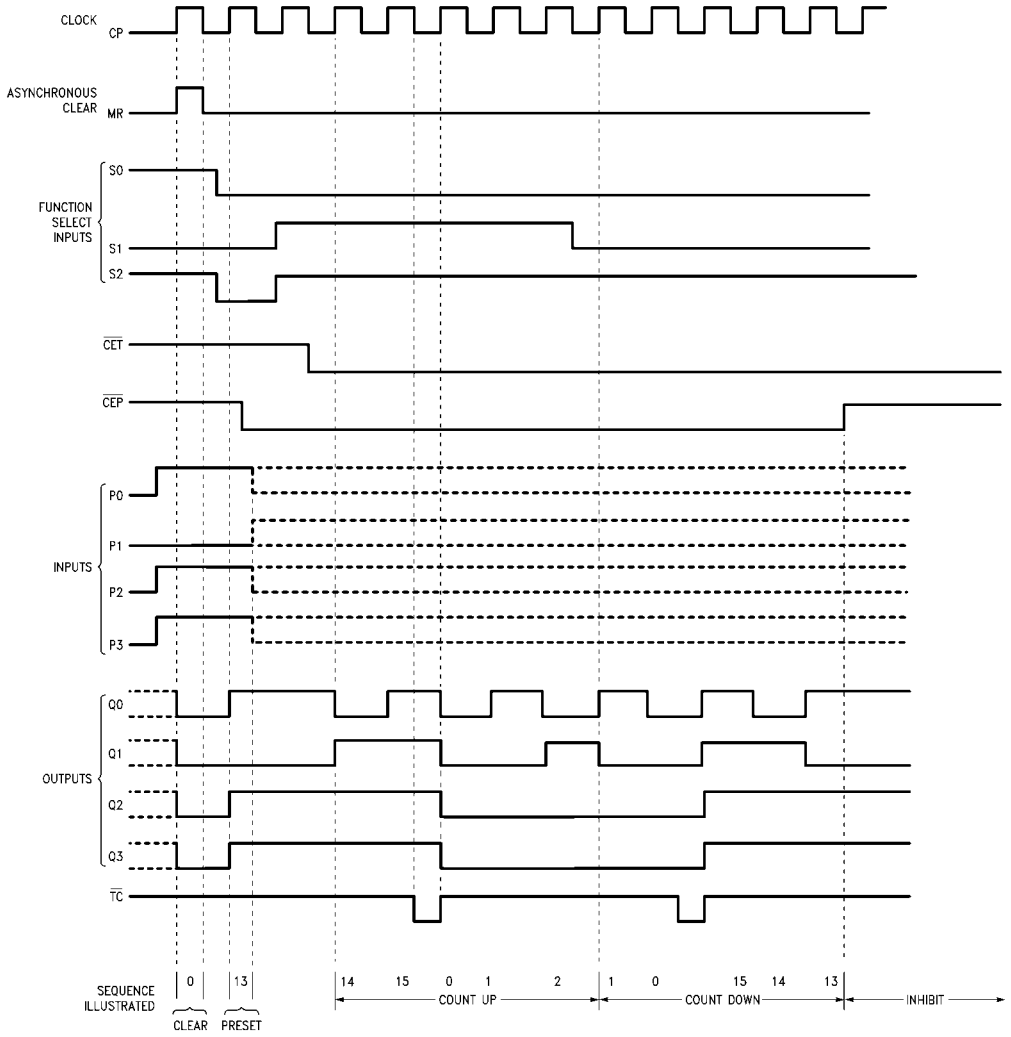
Count up/count down functions are selected with the select inputs (S_2–S_0). These are synchronous operations and the outputs will increment/decrement in value on the rising edge of the clock. Both count enable inputs ($\overline{CEP}$, $\overline{CET}$) must be true (LOW) to count. The terminal count output ($\overline{TC}$) becomes active-LOW when the count reaches zero in the DOWN mode or fifteen in the UP mode. Its duration is approximately equal to one period of the clock. The $\overline{TC}$ output is not recommended for use as a clock or synchronous reset for flip-flops. See Figure 1 for timing relationships in UP/DOWN counting.

In simple ripple-carry cascading applications the terminal count $\overline{TC}$ is fed forward to enable the trickle enable ($\overline{CET}$) input. This method is increasingly inefficient as the counting chain lengthens. The upper limit of the clock frequency is determined by the clock-to-terminal-count delay of the first stage, the cumulative trickle-enable ($\overline{CET}$)-to-terminal-count delay of the intermediate stages, and the trickle-enable-to-clock delay of the last stage. For faster counting rates a carry-lookahead scheme is necessary. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to change over from MAX to MIN in the UP mode, or from MIN to MAX in the DOWN mode. Since the final count cycle takes 16 clocks to complete, there is ample time for the ripple to propagate through the intermediate stages. The critical timing that limits the counting rate is the clock-to-terminal-count of the first stage plus the parallel-enable-to-clock ($\overline{CEP}$) setup time of the last stage. Figure 2 shows the connections for the fast-carry counting scheme.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (Preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
5. Inhibit counting.



Note: A MR overrides enables, data, and count inputs.

FIGURE 1. 100336 Used as Binary Up/Down Counter

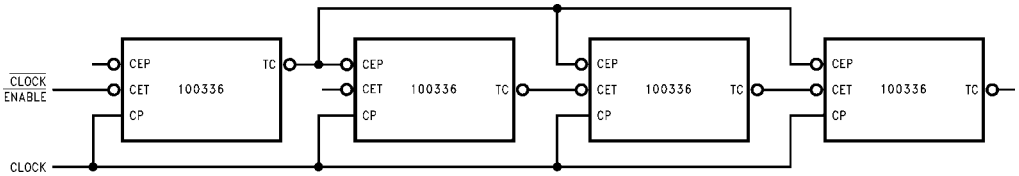


FIGURE 2. Fast Carry Counting Scheme

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES (Continued)

Shift right/left modes are performed by making the appropriate selection on the selection inputs (S_2–S_0). Each rising edge of the clock will cause the outputs to shift once in the direction which is selected. For shift-left operation, input D_3 is used as the serial input. For shift-right operation, input $\overline{CET}/D_0$ is used as the serial input. During shift operation the terminal count output reflects the level at the Q_3 output and the enables are "don't cares". See Figure 3 for shift operation timing relationships and shift sequences.

The 100336 provides two special modes of operation. The complement mode performs a one's complement of the outputs (Q_3–Q_0) on the rising edge of the clock input regardless of the levels at the enable inputs. The hold feature is asynchronous and simply stops counting or shifting operations. Both complement and hold are performed with proper selection of the select inputs. For a complete truth table of the 100336 operation, refer to Table 2.

DESIGN CONSIDERATIONS

Presetting the parallel inputs (P_3–P_0) may require a mixture of HIGH's and LOW's. A LOW may be preset by leaving the respective input open as the 100336 has a 50 kΩ resistor to V_{EE} on the parallel inputs. A HIGH must never be made by tying the input to V_{CC}/V_{CCA}. This saturates the input transistor. Instead the input is set at a diode drop below V_{CC}/V_{CCA} for a preset HIGH. See Applications Note 682.

Unused output pairs ($\overline{Q}_n/Q_n$) may be left unterminated. However, unused single outputs should be terminated to balance current switching in the outputs. For further details on system design considerations refer to the *F100K ECL Design Guide*. For AC/DC performance specifications and critical timing parameters refer to the 100336 datasheet.

APPLICATIONS

Figure 4 and Figure 5 demonstrate the use of the 100336 as UP/DOWN BCD counters. One additional gate is required to detect the limit count. Notice the alternate gate methods in Figure 4. The 100304 shows the classical AND/NAND design similar to TTL and the 100302 shows the OR/NOR design of ECL.

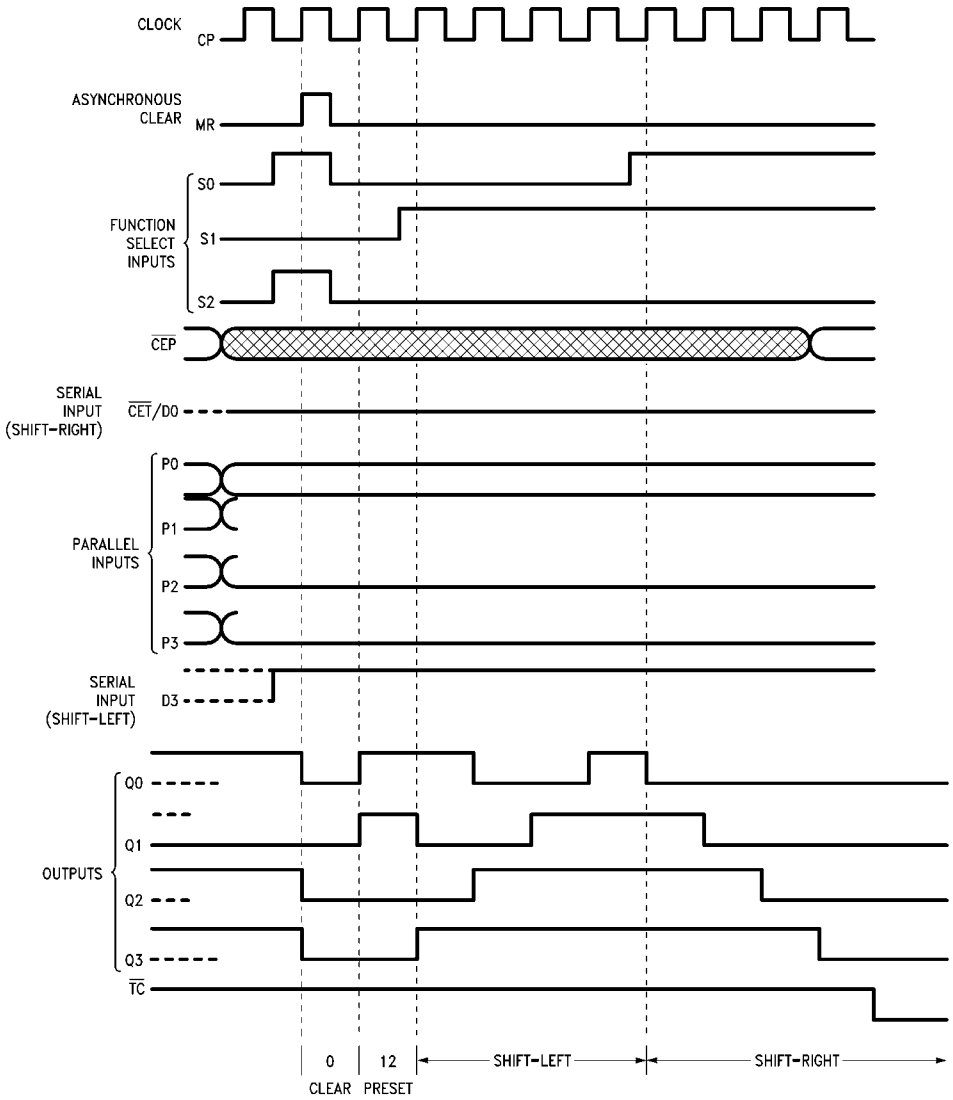
Figure 6 incorporates the use of a 100331 triple D-type flip-flop. By using one stage of the 100331, a 50/50 duty cycle can be realized from the divider.

An 8-bit parallel-to-serial shifter can be constructed by cascading two 100336's as shown in Figure 7. The third counter reloads another 8-bit data word after eight serial counts.

TYPICAL, CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary twelve.
3. Shift-left using D_3 as serial input.
4. Shift-right using $\overline{CET}/D_0$ as serial input.



Note: In shift-right mode $\overline{TC}$ follows the Q_3 output.

Note: In shift-left mode $\overline{TC}$ follows the D_3 input.

Note: $\overline{CEP}$ is a "don't care" during shifting.

FIGURE 3. 100336 Used as Bi-Directional Shift Register

TRUTH TABLE Q_0 = LSB

TABLE 2. Truth Table

Inputs								Outputs					
MR	**S_2**	**S_1**	**S_0**	**$\overline{CEP}$**	**$D_0/\overline{CET}$**	**D_3**	**CP**	**Q_3**	**Q_2**	**Q_1**	**Q_0**	**$\overline{TC}$**	**Mode**
L	L	L	L	X	X	X	↗	P_3	P_2	P_1	P_0	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	L	Invert
L	L	H	L	X	X	X	↗	D_3	Q_3	Q_2	Q_1	D_3	Shift Left
L	L	H	H	X	X	X	↗	Q_2	Q_1	Q_0	D_0	Q_3 (Note 1)	Shift Right
L	H	L	L	L	L	X	↗	(Q_0–Q_3) minus 1				1	Count Down
L	H	L	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	1	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q_0–Q_3) plus 1				2	Count Up
L	H	H	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	2	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_3	Q_2	Q_1	Q_0	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	Asynchronous
H	H	L	L	X	L	X	X	L	L	L	L	L	Master Reset
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

1 = L if Q_0–Q_3 = LLLL
H if Q_0–$Q_3 \neq$ LLLL
2 = L if Q_0–Q_3 = HHHH
H if Q_0–$Q_3 \neq$ HHHH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW-to-HIGH Transition

Note 1: Before the clock, $\overline{TC}$ is Q_3

After the clock, $\overline{TC}$ is Q2

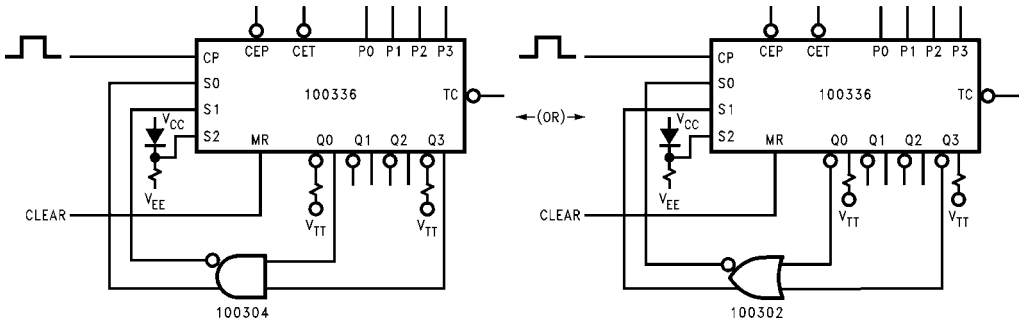


FIGURE 4. BCD Up Counter (0–9)

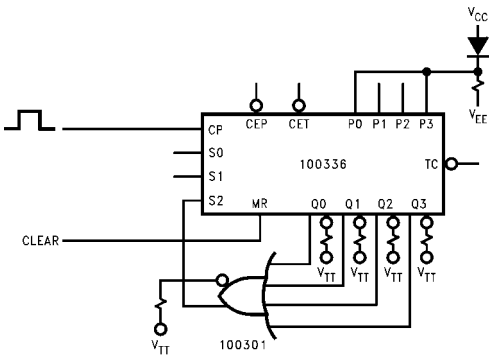


FIGURE 5. BCD Down Counter (9–0)

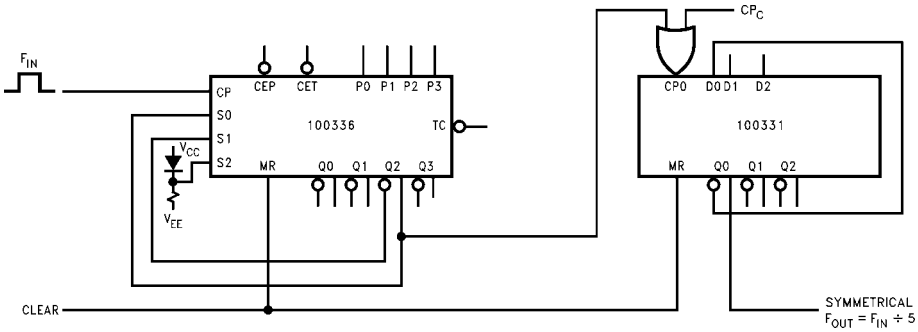


FIGURE 6. Divide by Five

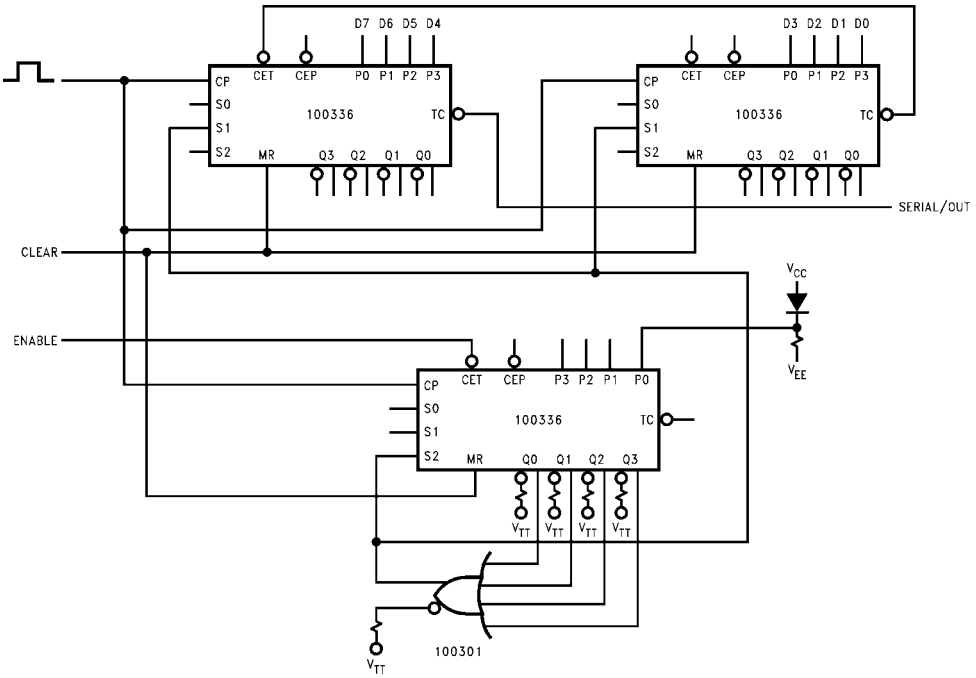


FIGURE 7. 8-Bit Shift Left