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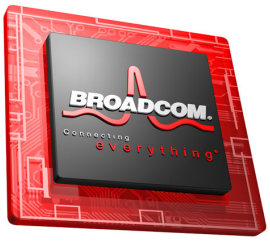
BCM8124
PRODUCT Brief



LOW-JITTER 10-GBPS 16:1 MUX WITH CLOCK GENERATION AND MSA FEATURES

FEATURES

- **Supports 10-Gigabit MSA (Multi-Source Agreement) features**
- **Enhanced 10-Gbps serial output data:**
  - Minimum 500 mV, single-ended output voltage swing
- **Fully integrated Clock Multiplication Unit (CMU) and multiplexer**
- **Support for multiple rates—OC-192: 9.953 Gbps, OC-192 FEC: 10.664 and 10.709 Gbps, 10G Ethernet: 10.3125 Gbps**
- **16:1 multiplexer with LVDS data inputs**
- **Configurable bus clock for divide either by 32 or 16 of the selected high-speed output rate**
- **Configurable LVDS input clock to data bus timing skew control for 311.04-MHz clock mode**
- **On-chip 16 x 10 FIFO to eliminate system timing issues**
- **Lock detect**
- **Core power supply: 1.8V**
- **I/O power supply: CML and LVPECL at 1.8V, LVDS and CMOS at 1.8V or 3.3V, phase detector at 3.3V**
- **Power consumption: 450 mW typical @ 1.8V**
- **Standard CMOS fabrication process**
- **11 x 11 mm, 127-pin BGA pacakge**

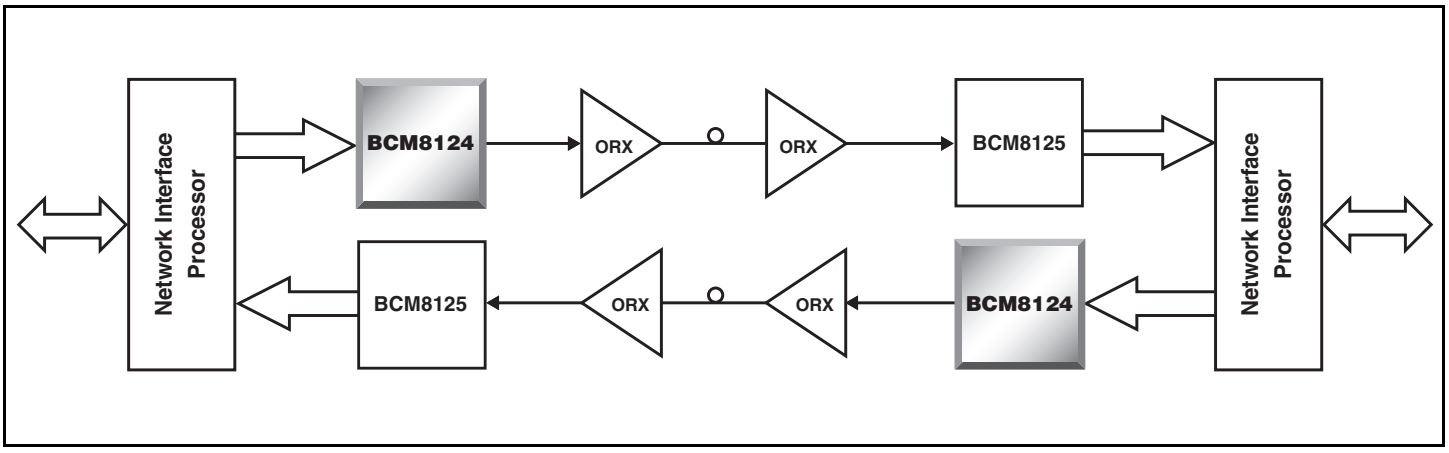
SUMMARY OF BENEFITS

- **Compliant with industry standards such as Optical Internetworking Forum (OIF), Telcordia, ITU-T, and IEEE 802.3ae standards.**
- **Reduces design cycle and time to market.**
- **High level of integration allows for higher port density solutions.**
- **Uses the most effective silicon economy of scale for CMOS-based devices.**
- **Low power consumption eliminates the need for external cooling sources.**

APPLICATIONS

- **OC-192/STM-64/10GE transmission equipment**
- **SONET/SDH optical modules**
- **ADD/DROP multiplexers**
- **Digital cross-connects**
- **ATM switch backbones**
- **SONET test equipment**
- **Terabit routers**

BCM8124 Application Diagram



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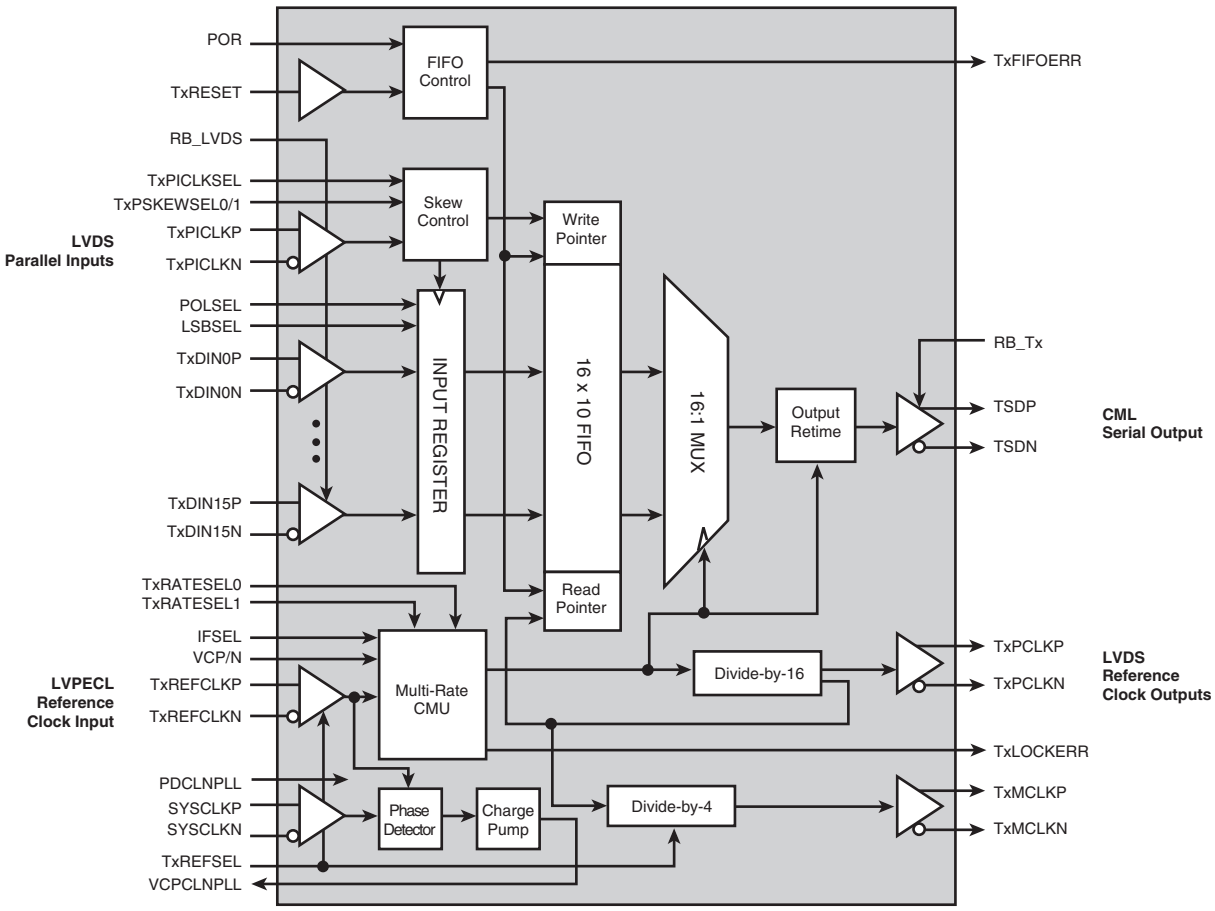
OVERVIEW



The **BCM8124** is a fully integrated MSA-compatible quad-rate SONET/SDH/10GE/FEC transmitter operating at 9.953, 10.3125, 10.664, and 10.709 Gbps with serializer and Clock Multiplication Unit (CMU). The low-jitter LVDS interface and onboard low-jitter PLL exceed Optical Internetworking Forum (OIF), IEEE 802.3ae, Telcordia, ANSI, and ITU-T jitter standards.

The **BCM8124** reference clock input frequency is user-selectable to the line rate divided by either 16 or 64. The **BCM8124** provides skew control between the LVDS transmit parallel input clock and data to accommodate difficult timing variances. A 10-word FIFO decouples the parallel input timing domain from the serial output timing domain.

An internal phase detector and charge pump can be used to implement a cleanup phase-locked loop (PLL) for line/loop timing applications.

The **BCM8124** can be powered with a single 1.8V supply or dual 1.8/3.3V supplies without any special power supply sequencing requirements. Boosted input voltage range is available at the LVDS inputs to interface with devices operating non-standard common-mode output voltages ranging from 0.85 to 2.2V.

The data bit order and/or polarity can be reversed to facilitate ease in printed circuit board (PCB) layouts.

The **BCM8124** comes in a 11 x 11 mm, 127-pin BGA package.

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