10K & 100K ECL BUFFERED DELAY MODULES

GENERAL OPERATING SPECIFICATIONS 10K ECL:

V_{EE} Supply Voltage ..... -5.20 ± 0.25 VDC
I_{EE} Supply Current (5-TAP MODULES) ..... 65 mA typical
Logic "1" Input:
V_{IH} ..... -0.98V min.
I_{IH} ..... 265µA max.
Logic "0" Input:
V_{IL} ..... -1.63V max.
I_{IL} ..... 0.5µA max.
V_{OH} Logic "1" Voltage Out ..... -0.96V min.
V_{OL} Logic "0" Voltage Out ..... -1.65V max.
T_{RO} Output Rise Time ..... <3.00ns typ.
P_{WI} Input Pulse Width Tapped units ..... 40% of total delay min.
P_{WI} Input Pulse Width Multiple units ..... 100% of total delay min.
Operating Temperature Range ..... -30° to +85°C
Storage Temperature Range ..... -65° to +150°C

TEST CONDITIONS 10K ECL: (Measurments at 25°C)

V_{EE} Supply Voltage ..... -5.20 VDC
Input Pulse Voltage ..... -0.80V to -1.80V
Input Pulse Rise Time ..... 3.00ns max.
Input Pulse Period ..... 4.0 x Total Delay
Input Pulse Duty Cycle 50%
Outputs terminated through 100 Ohms to -2.00VDC.

1. Rise Times are measured from 20% to 80% points.
2. Delay Times measured at 50% point on the leading edge.

GENERAL OPERATING SPECIFICATIONS 100K ECL:

V_{EE} Supply Voltage ..... -4.50 ± 0.30 VDC
I_{EE} Supply Current (5-TAP MODULES) ..... 90 mA typical
Logic "1" Input:
V_{IH} ..... -1.165V min.
I_{IH} ..... 350µA max.
Logic "0" Input:
V_{IL} ..... -1.475V max.
I_{IL} ..... 0.5µA max.
V_{OH} Logic "1" Voltage Out ..... -1.025V min.
V_{OL} Logic "0" Voltage Out ..... -1.620V max.
T_{RO} Output Rise Time ..... <1.00ns typ.
P_{WI} Input Pulse Width Tapped units ..... 40% of total delay min.
P_{WI} Input Pulse Width Multiple units ..... 100% of total delay min.
Operating Temperature Range ..... 0° to +85°C
Storage Temperature Range ..... -65° to +150°C

TEST CONDITIONS 100K ECL: (Measurments at 25°C)

V_{EE} Supply Voltage ..... -4.50 VDC
Input Pulse Voltage ..... -0.80V to -1.80V
Input Pulse Rise Time ..... 1.00ns max.
Input Pulse Period ..... 4.0 x Total Delay
Input Pulse Duty Cycle 50%
Outputs terminated through 50 Ohms to -2.00VDC.

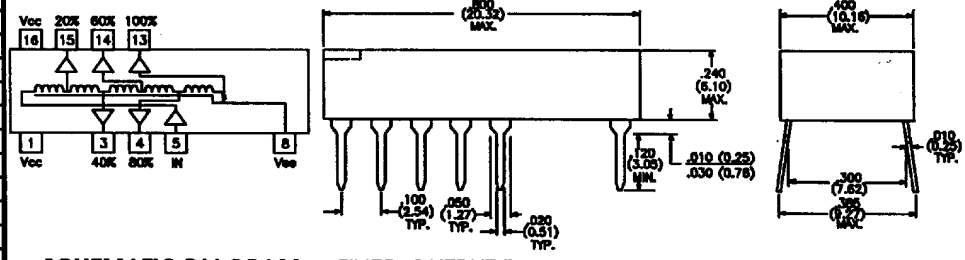
1. Rise Times are measured from 20% to 80% points.
2. Delay Times measured at 50% point on the leading edge.

5-TAP & FIXED 10K ECL THROUGH -HOLE DIL ..... DECL-XXX , FECL-XXX SERIES

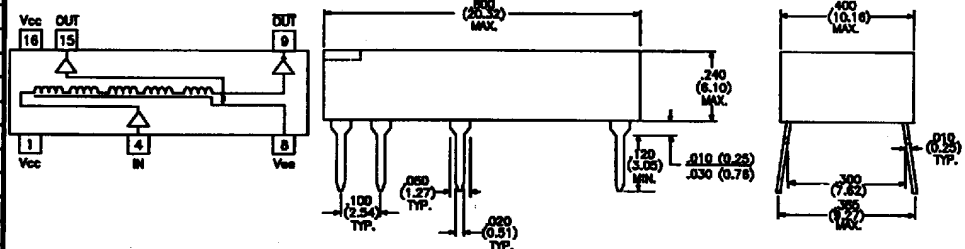
PART NUMBERS 5-TAP	PART NUMBERS FIXED	OUTPUT DELAY (ns)	TAPS (ns)
DECL-10	FECL-10	10 ± 2.00	2 ± 1.0
DECL-15	FECL-25	15 ± 2.00	3 ± 2.0
DECL-20	FECL-25	20 ± 2.00	4 ± 2.0
DECL-25	FECL-25	25 ± 2.00	5 ± 2.0
DECL-30	FECL-30	30 ± 2.00	6 ± 2.0
DECL-35	FECL-35	35 ± 2.00	7 ± 2.0
DECL-40	FECL-40	40 ± 2.00	8 ± 2.0
DECL-45	FECL-45	45 ± 2.25	9 ± 2.0
DECL-50	FECL-50	50 ± 2.50	10 ± 2.0
DECL-60	FECL-55	60 ± 3.00	12 ± 2.0
DECL-70	FECL-70	70 ± 3.50	14 ± 2.0
DECL-75	FECL-75	75 ± 3.75	15 ± 2.5
DECL-100	FECL-100	100 ± 5.00	20 ± 3.0
DECL-125	FECL-125	125 ± 6.25	25 ± 3.0
DECL-150	FECL-150	150 ± 7.50	30 ± 3.0
DECL-175	FECL-175	175 ± 8.75	35 ± 3.5
DECL-200	FECL-200	200 ± 10.00	40 ± 4.0
DECL-225	FECL-225	225 ± 11.25	45 ± 4.5
DECL-250	FECL-250	250 ± 12.50	50 ± 5.0
DECL-275	FECL-275	275 ± 13.75	55 ± 5.5
DECL-300	FECL-300	300 ± 15.00	60 ± 6.0
DECL-325	FECL-325	325 ± 16.25	65 ± 6.5
DECL-350	FECL-350	350 ± 17.50	70 ± 7.0
DECL-375	FECL-375	375 ± 18.75	75 ± 7.5
DECL-400	FECL-400	400 ± 20.00	80 ± 8.0
DECL-425	FECL-425	425 ± 21.25	85 ± 8.5
DECL-450	FECL-450	450 ± 22.50	90 ± 9.0
DECL-475	FECL-475	475 ± 23.75	95 ± 9.5
DECL-500	FECL-500	500 ± 25.00	100 ± 10

PHYSICAL DIMENSIONS All dimensions in inches (mm)
Military Part Height for DECL-XXXM or FECL-XXXM: .300 Max. (7.62)

SCHEMATIC DIAGRAM 5-TAP DIL ..... DECL-XXX



SCHEMATIC DIAGRAM FIXED OUTPUT DIL ..... FECL-XXX



PART NUMBER DESCRIPTION XXXX - XXX X

10K ECL Delay Line
DECL = 5-TAP
FECL = FIXED OUTPUT
Total Delay in nanoseconds (ns)
Grade
Blank = Commercial M = Military (see note)

Specifications subject to change without notice

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