HB56AW873E-A Series

8,388,608-word × 72-bit High Density Dynamic RAM Module

HITACHI

ADE-203-816A (Z)
Rev. 1.0
Aug. 29, 1996

Description

The HB56AW873E-A belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56AW873E-A is a 8M × 72 dynamic RAM module, mounted 9 pieces of 64-Mbit DRAM (HM5165800A) sealed in TSOP package and 2 pieces of 16-bit BiCMOS line driver (74LVT16244) sealed in TSSOP package. An outline of the HB56AW873E-A is 168-pin socket type package (dual lead out). Therefore, the HB56AW873E-A makes high density mounting possible without surface mount technology. The HB56AW873E-A provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the its module board.

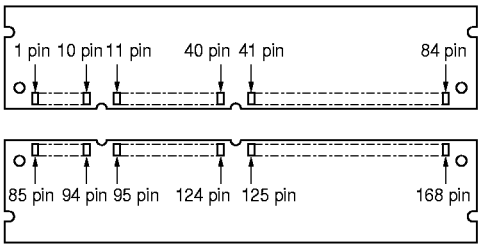
Features

- 168-pin socket type package (Dual lead out)
  - — Lead pitch: 1.27 mm
- Single 3.3 V (±0.3 V) supply
- High speed
  - — Access time: t_{RAC} = 60/70 ns (max)
  - — Access time: t_{CAC} = 20/23 ns (max)
- Low power dissipation
  - — Active mode: 4.73/4.41 W (max)
  - — Standby mode (TTL): 100 mW (max)
- Buffered input except $\overline{RAS}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 4,096 refresh cycle: 64 ms
- 2 variations of refresh
  - — $\overline{RAS}$-only refresh
  - — $\overline{CAS}$-before-$\overline{RAS}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56AW873E-6A	60 ns	168-pin dual lead out socket type	Gold
HB56AW873E-7A	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	43	DQ9	85	NC	127	A8
2	DQ0	44	DQ10	86	V_{CC}	128	A10
3	DQ1	45	DQ11	87	$\overline{WE0}$	129	NC
4	DQ2	46	DQ12	88	$\overline{CE0}$	130	V_{CC}
5	DQ3	47	DQ13	89	NC	131	NC
6	V_{CC}	48	V_{CC}	90	$\overline{RE0}$	132	NC
7	DQ4	49	DQ14	91	$\overline{OE0}$	133	V_{SS}
8	DQ5	50	DQ15	92	V_{SS}	134	$\overline{OE2}$
9	DQ6	51	DQ16	93	A0	135	$\overline{RE2}$
10	DQ7	52	DQ17	94	A2	136	$\overline{CE4}$
11	DQ8	53	V_{SS}	95	A4	137	NC
12	V_{SS}	54	NC	96	A6	138	$\overline{WE2}$

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
13	V_{CC}	55	PD1	97	NC	139	DQ56
14	NC	56	PD3	98	V_{CC}	140	DQ57
15	NC	57	PD5	99	NC	141	DQ58
16	DQ18	58	PD7	100	NC	142	DQ59
17	DQ19	59	ID0 (V_{SS})	101	NC	143	V_{CC}
18	V_{SS}	60	V_{CC}	102	NC	144	DQ60
19	DQ20	61	V_{SS}	103	NC	145	NC
20	DQ21	62	DQ36	104	V_{SS}	146	NC
21	DQ22	63	DQ37	105	A1	147	NC
22	DQ23	64	DQ38	106	A3	148	NC
23	V_{CC}	65	DQ39	107	A5	149	DQ61
24	DQ24	66	V_{CC}	108	A7	150	DQ62
25	NC	67	DQ40	109	A9	151	DQ63
26	NC	68	DQ41	110	A11	152	V_{SS}
27	NC	69	DQ42	111	NC	153	DQ64
28	NC	70	DQ43	112	V_{CC}	154	DQ65
29	DQ25	71	DQ44	113	NC	155	DQ66
30	DQ26	72	V_{SS}	114	B0	156	DQ67
31	DQ27	73	DQ45	115	V_{SS}	157	V_{CC}
32	V_{SS}	74	DQ46	116	NC	158	DQ68
33	DQ28	75	DQ47	117	NC	159	DQ69
34	DQ29	76	DQ48	118	NC	160	DQ70
35	DQ30	77	DQ49	119	NC	161	DQ71
36	DQ31	78	V_{CC}	120	$\overline{PDE}$	162	V_{SS}
37	V_{CC}	79	DQ50	121	Vcc	163	PD2
38	DQ32	80	DQ51	122	NC	164	PD4
39	DQ33	81	DQ52	123	NC	165	PD6
40	DQ34	82	DQ53	124	DQ54	166	PD8
41	DQ35	83	V_{SS}	125	DQ55	167	ID1 (V_{SS})
42	V_{SS}	84	NC	126	V_{SS}	168	V_{CC}

Pin Description

Pin Name	Function
A0 to A11, B0	Address Input (D0 to D8) : A0 to A11, B0 Row Address (D0 to D8) : A0 to A11, B0 Column Address (D0 to D8) : A0 to A10, B0 Refresh Address (D0 to D8) : A0 to A11, B0
DQ0 to DQ71	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row Address Strobe ($\overline{RAS}$)
$\overline{CE0}$, $\overline{CE4}$	Column Address Strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
PD1 to PD8	Presence Detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence Detect Enable
NC	Non Connection

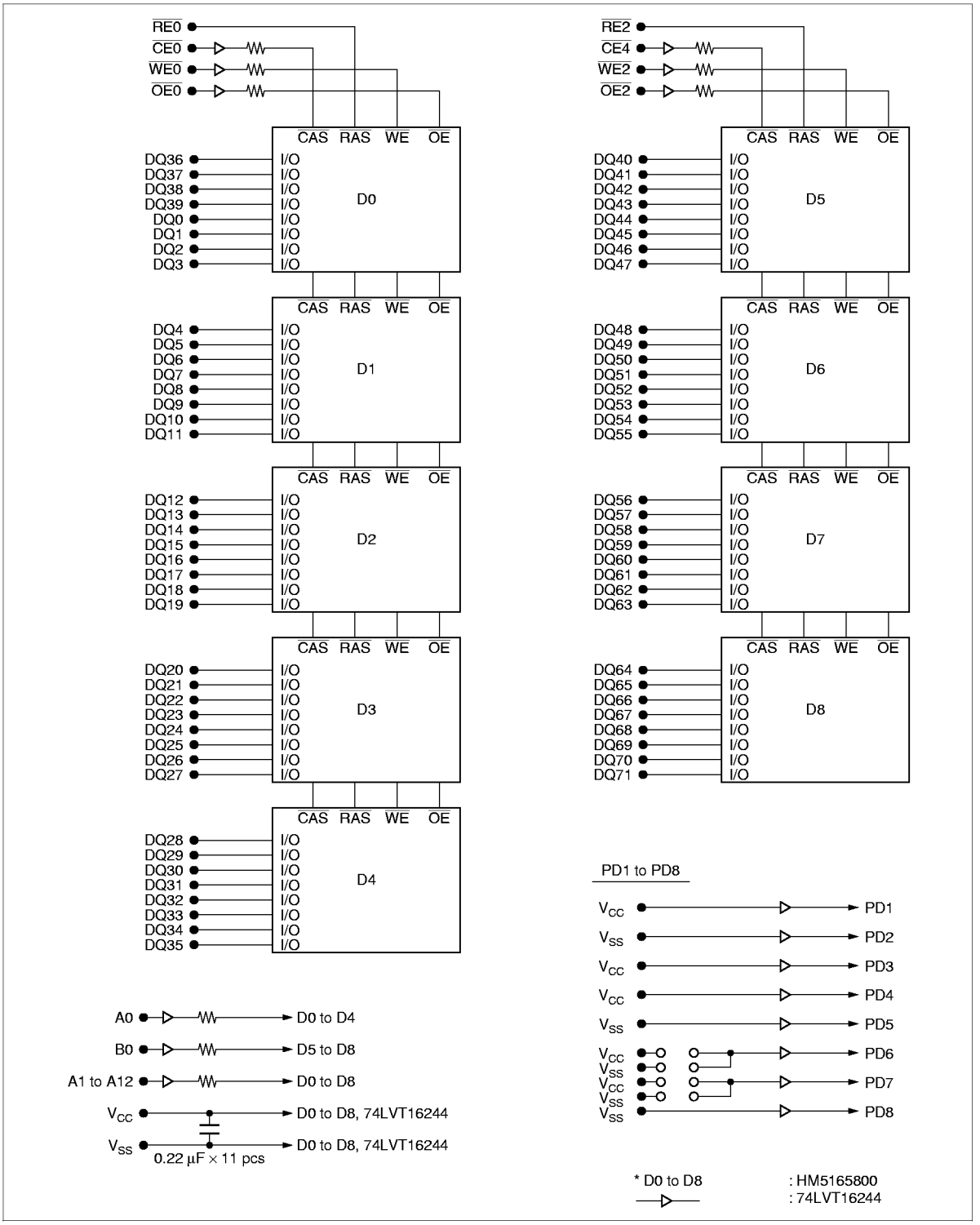
Presence Detect Pin Assignment

		$\overline{PDE}$ = Low		$\overline{PDE}$ = High
Pin Name	**Pin No.**	**60 ns**	**70 ns**	**All**
PD1	79	1	1	High-Z
PD2	163	0	0	High-Z
PD3	80	1	1	High-Z
PD4	164	1	1	High-Z
PD5	81	0	0	High-Z
PD6	165	1	0	High-Z
PD7	82	1	1	High-Z
PD8	166	0	0	High-Z

1 : High Level (Driver Output)

0 : Low Level (Driver Output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	10	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB56AW873E-A						
		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test condition**	**Note**
Operating current	I_{CC1}	—	1675	—	1495	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	28	—	28	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	19	—	19	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1675	—	1495	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	55	—	55	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1360	—	1180	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	1135	—	1045	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less within one page mode cycle t_{PC}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	55	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V)[*1, *2, *17]

Test Conditions

- Input rise and fall times: 5 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	110	—	130	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	18	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	47	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	14	25	15	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	20	—	23	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	20	—	23	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	ns	7

Read Cycle

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	23	ns	9, 10, 16
Access time from address	t_{AA}	—	35	—	40	ns	9, 11, 16
Access time from $\overline{OE}$	t_{OEA}	—	20	—	23	ns	9, 19
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	30	—	35	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	20	—	20	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	23	—	ns	5

Write Cycle

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	23	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	—	18	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	18	—	ns	

Read-Modify-Write Cycle

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	155	—	181	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	90	—	103	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	ns	

Refresh Cycle

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	ns	

Fast Page Mode Cycle

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	15
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	40	—	45	ns	9, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HB56AW873E-A					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{HPRWC}	85	—	96	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	60	—	68	—	ns	14

Refresh

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	64	ms	4096 cycles

Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.
16. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
17. All the V_{CC} and V_{SS} pin shall be supplied with the same voltages.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.

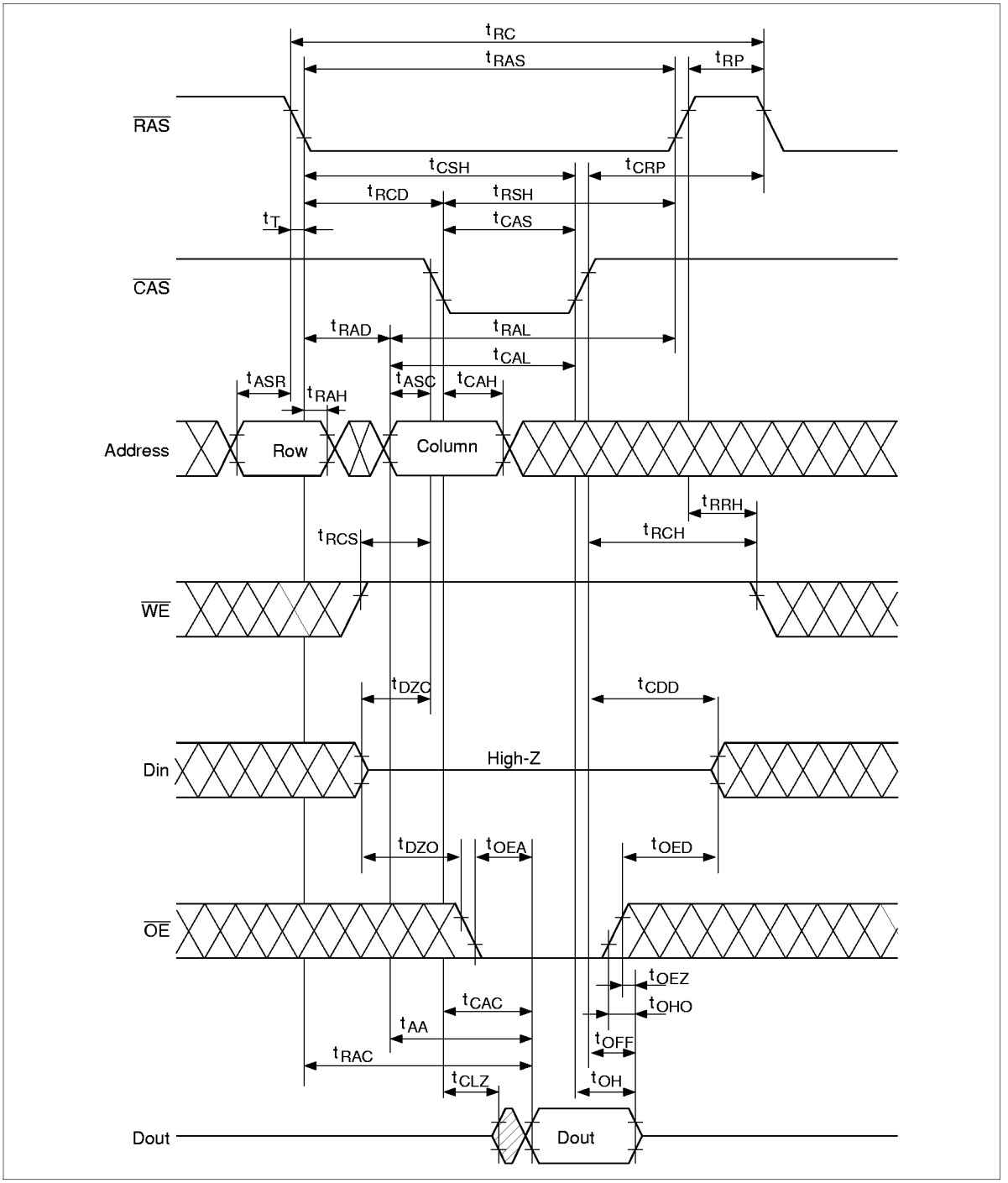
19. When output buffers are enable once, sustain the low impedance state until valid data is obtained. when output buffer is turned on and off within a vary short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

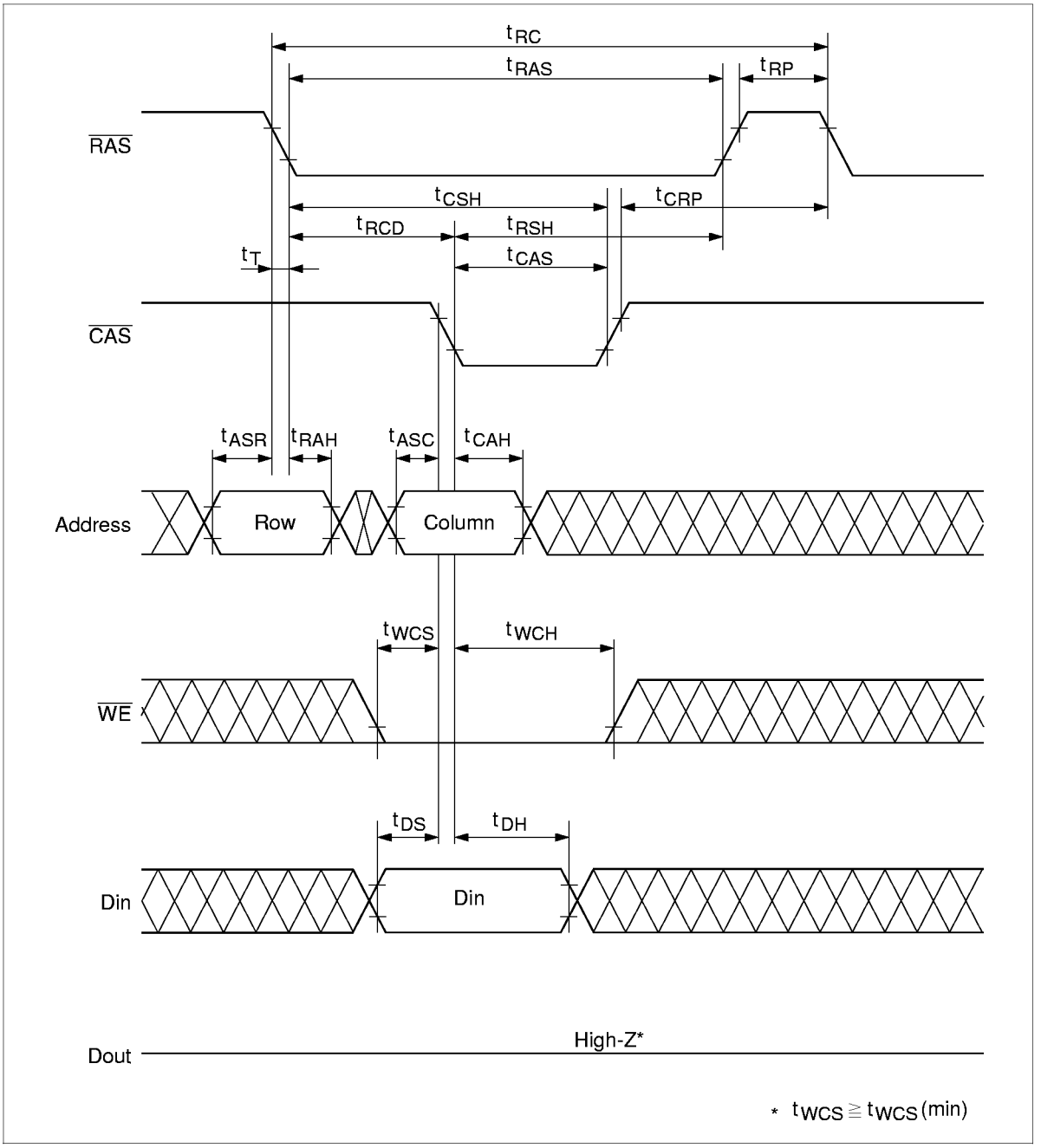
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveform[*20]

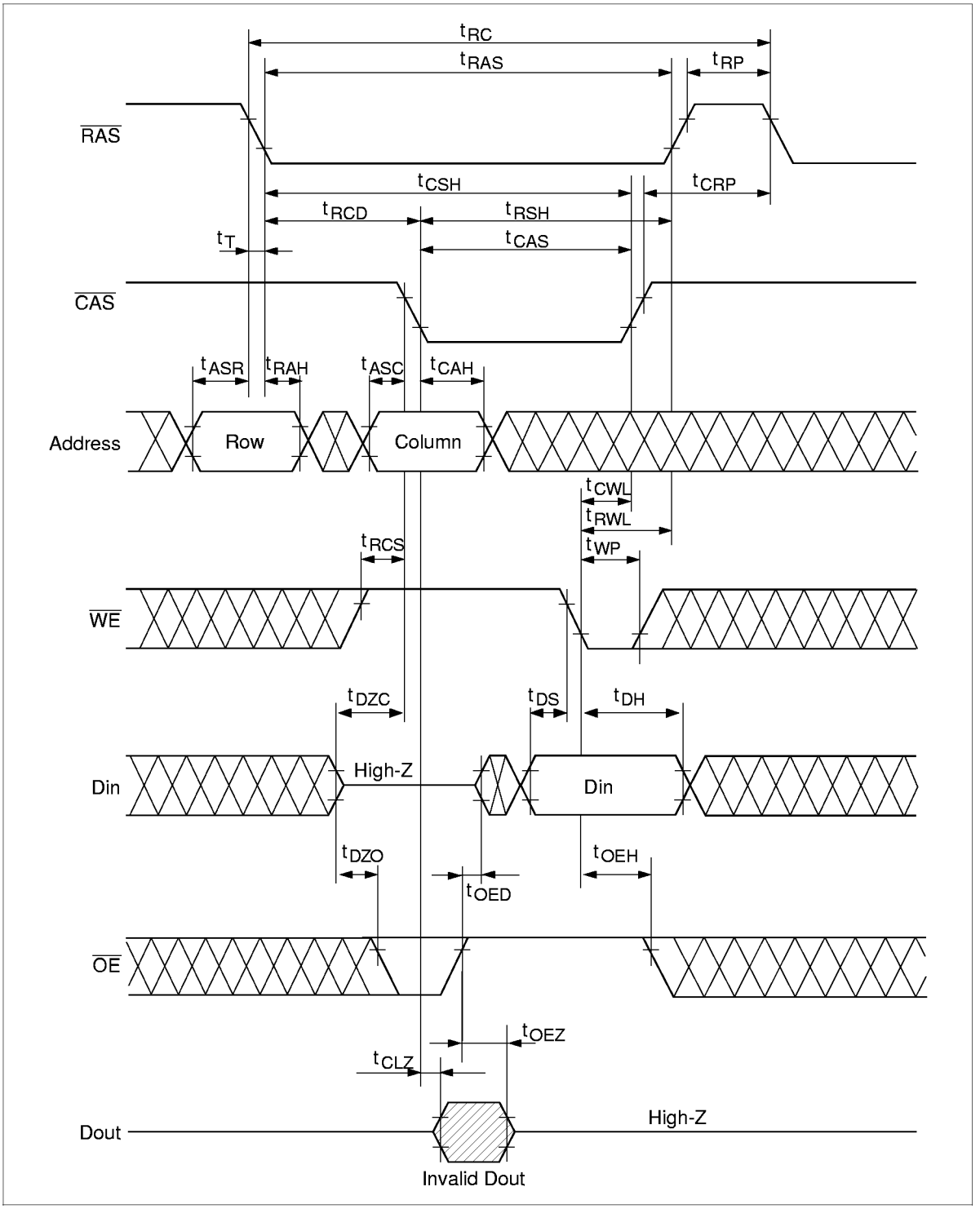
Read Cycle



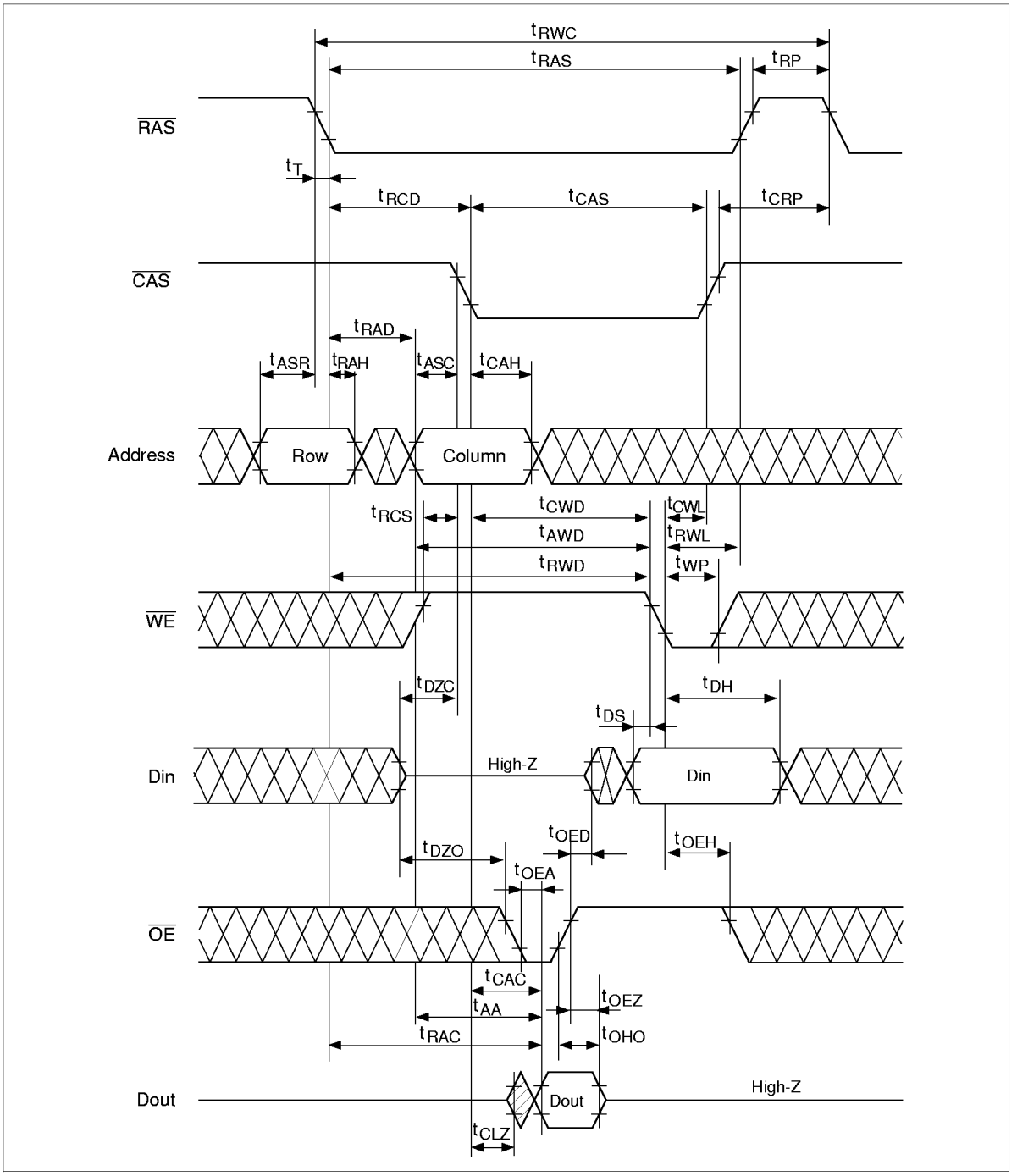
Early Write Cycle



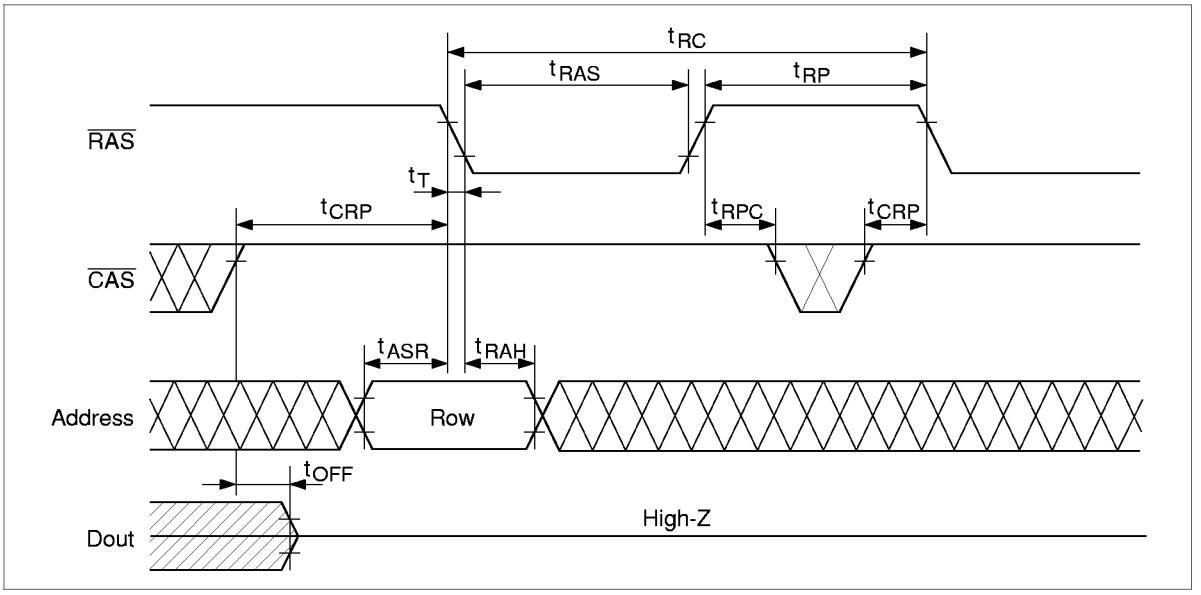
Delayed Write Cycle[*18]



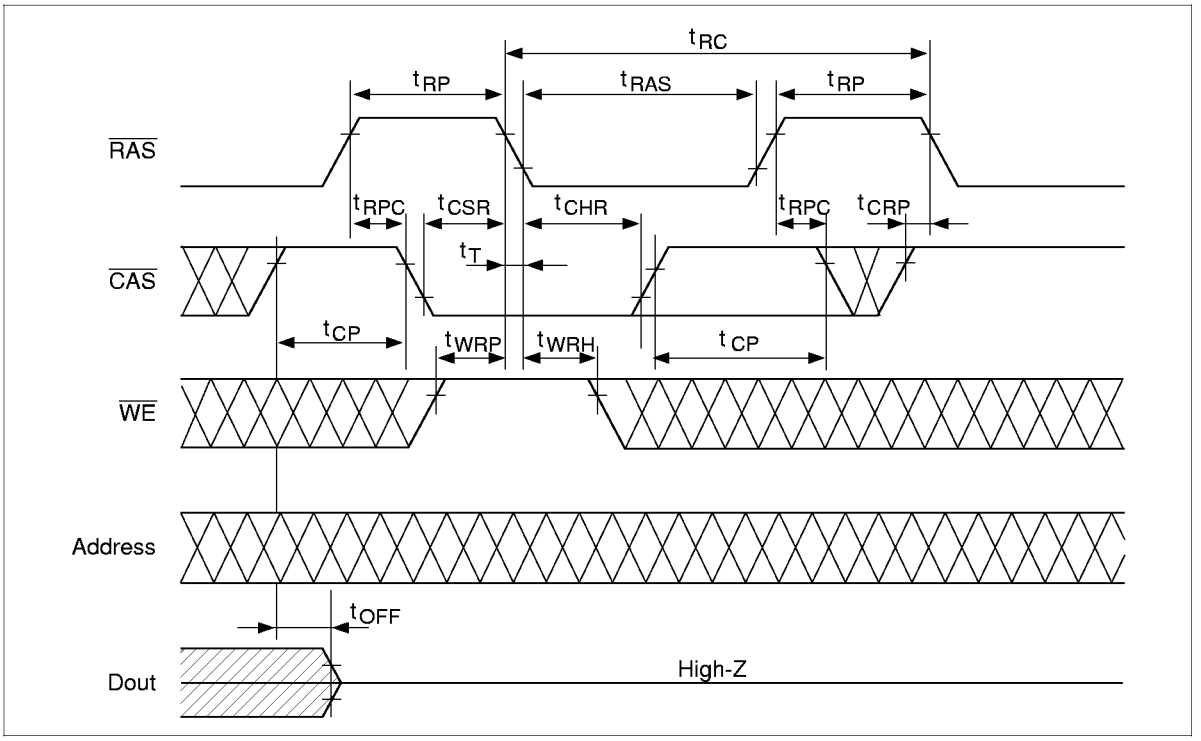
Read-Modify-Write Cycle[*18]



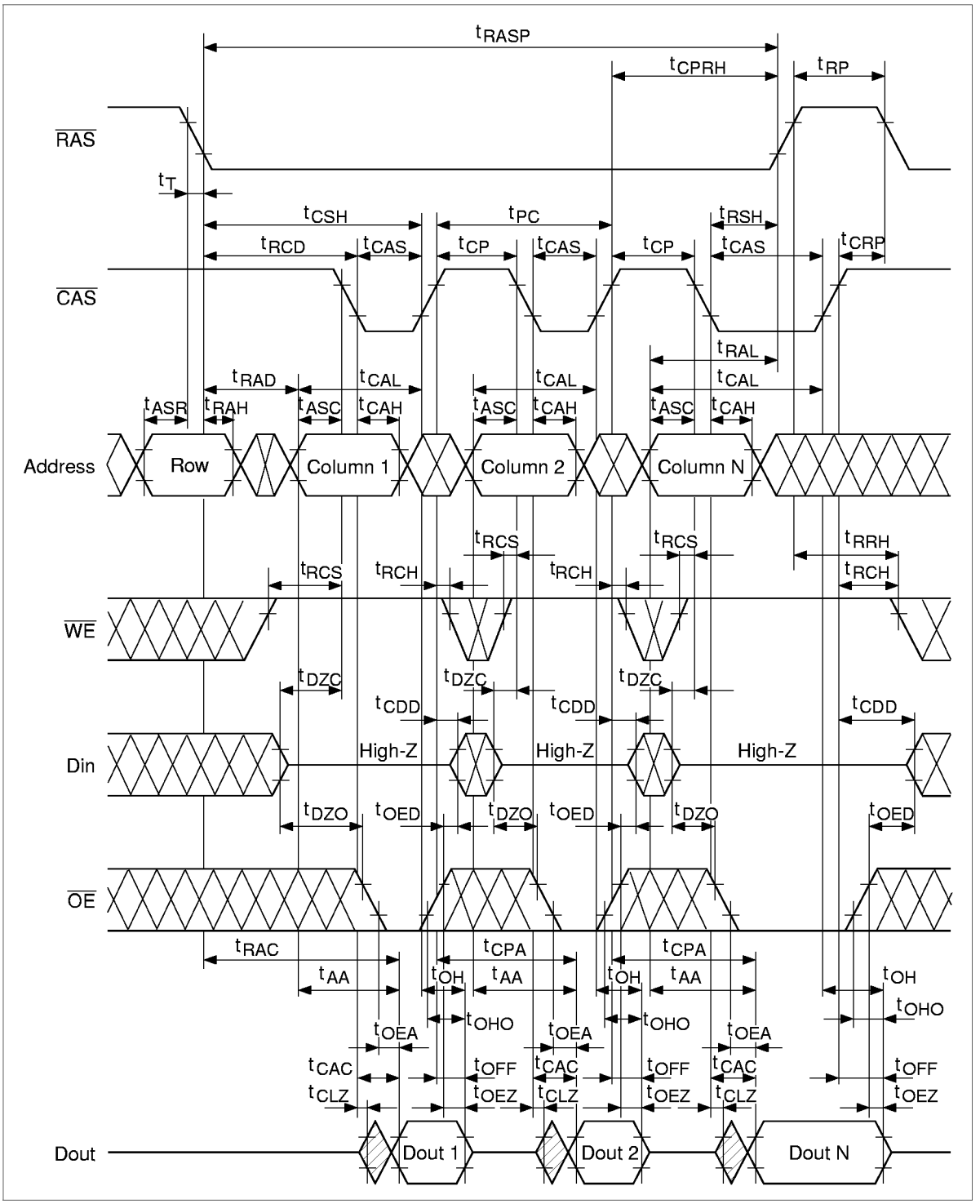
$\overline{\text{RAS}}$-Only Refresh Cycle



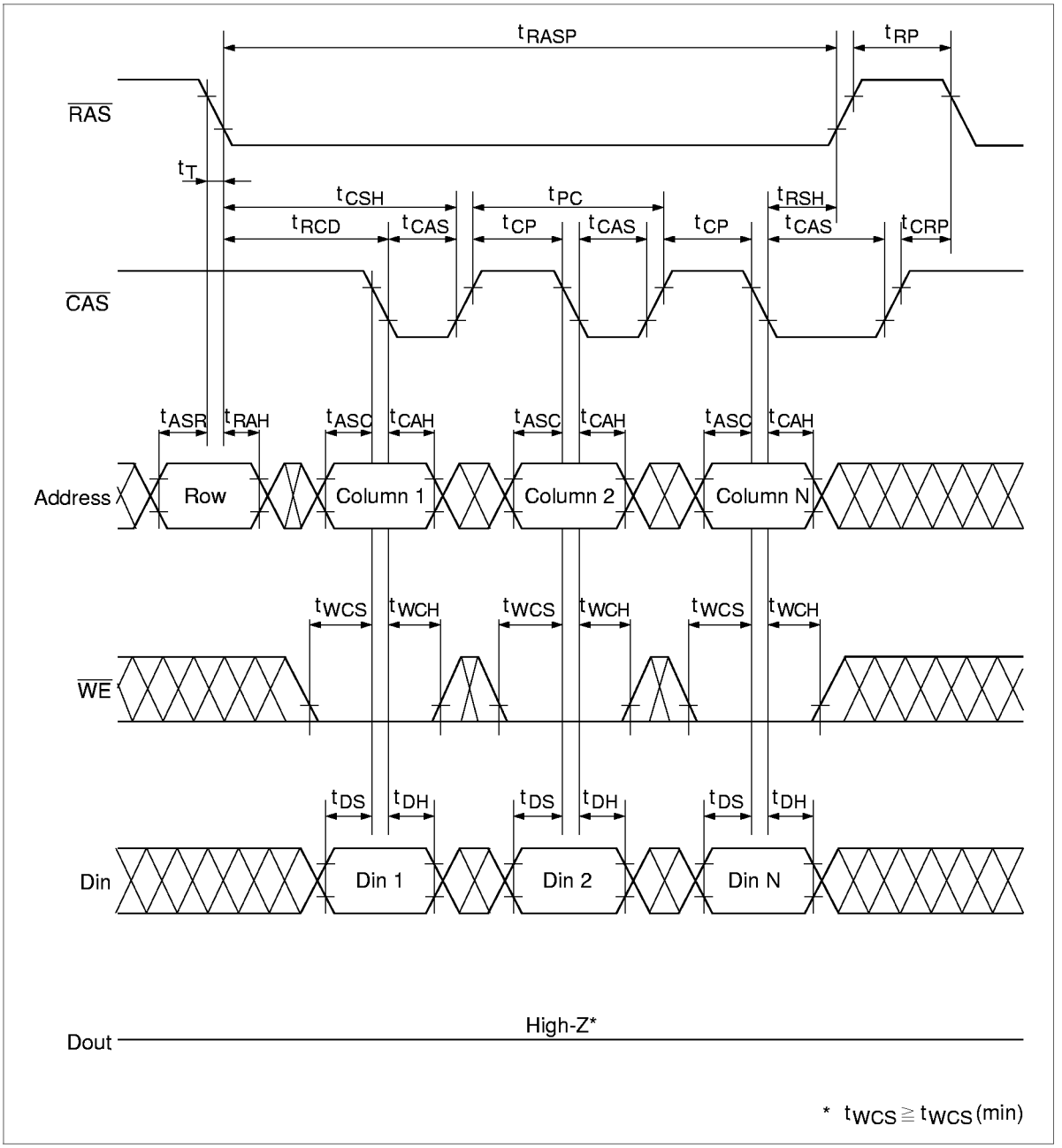
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



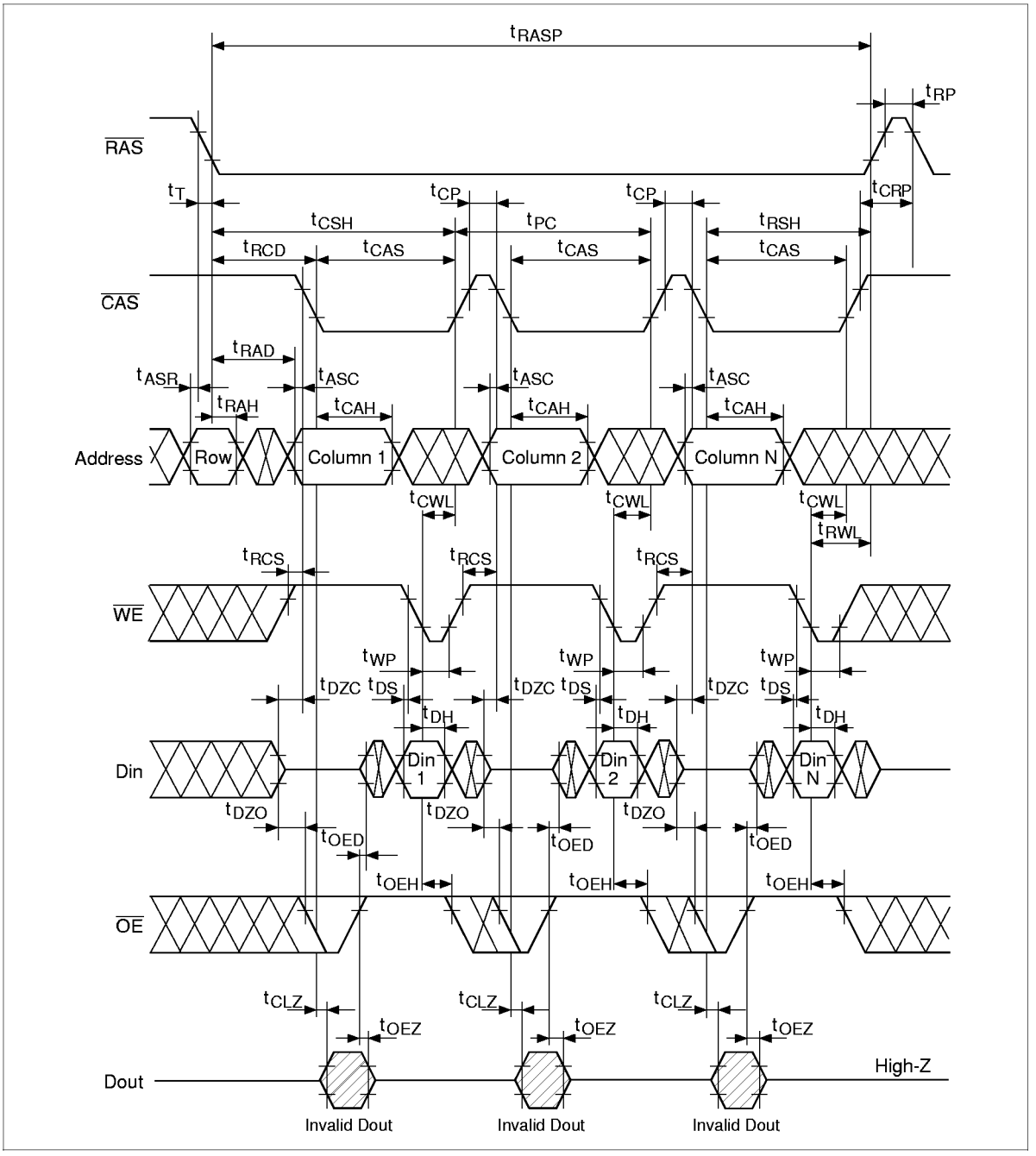
Fast Page Mode Read Cycle



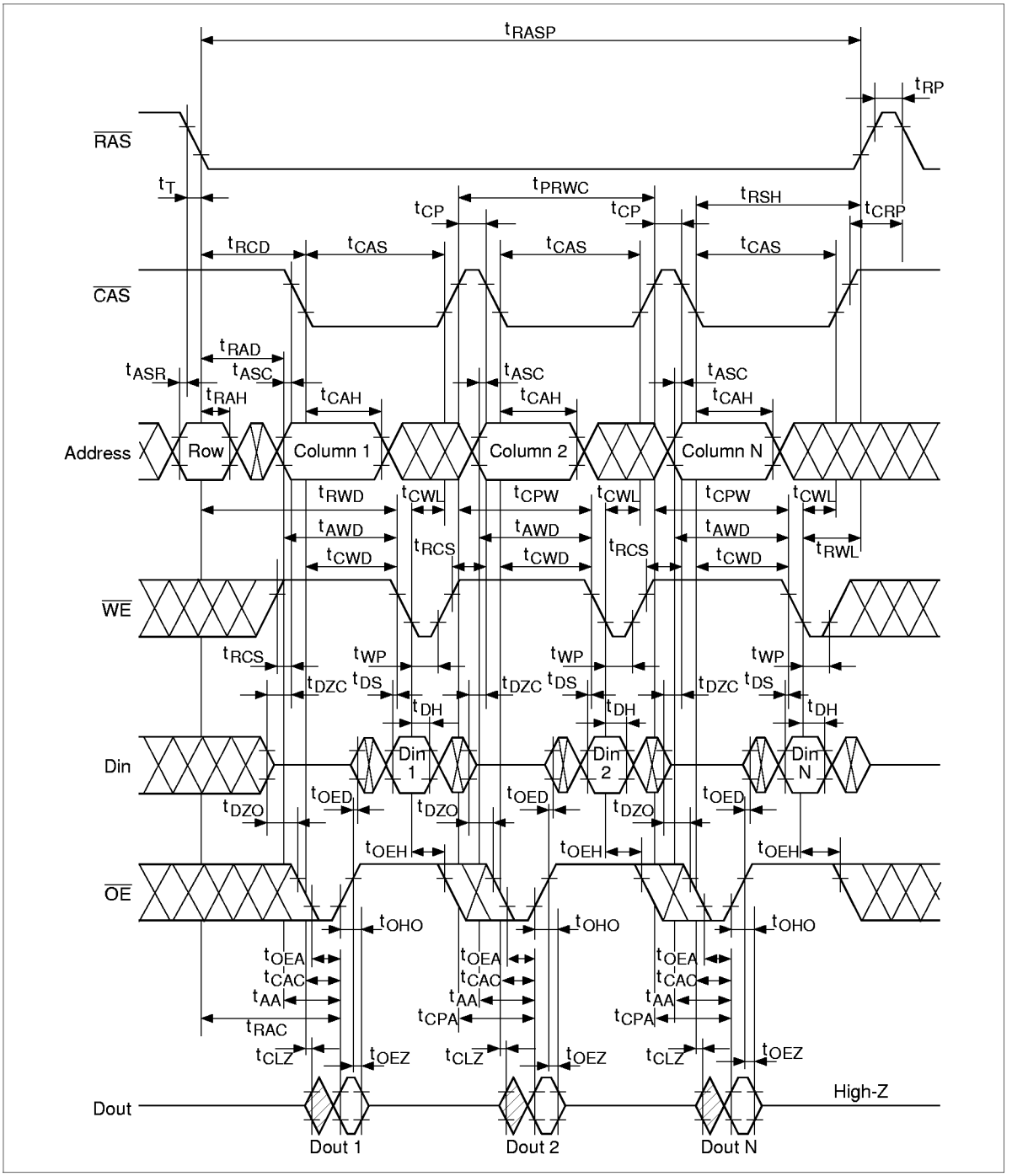
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle[*18]

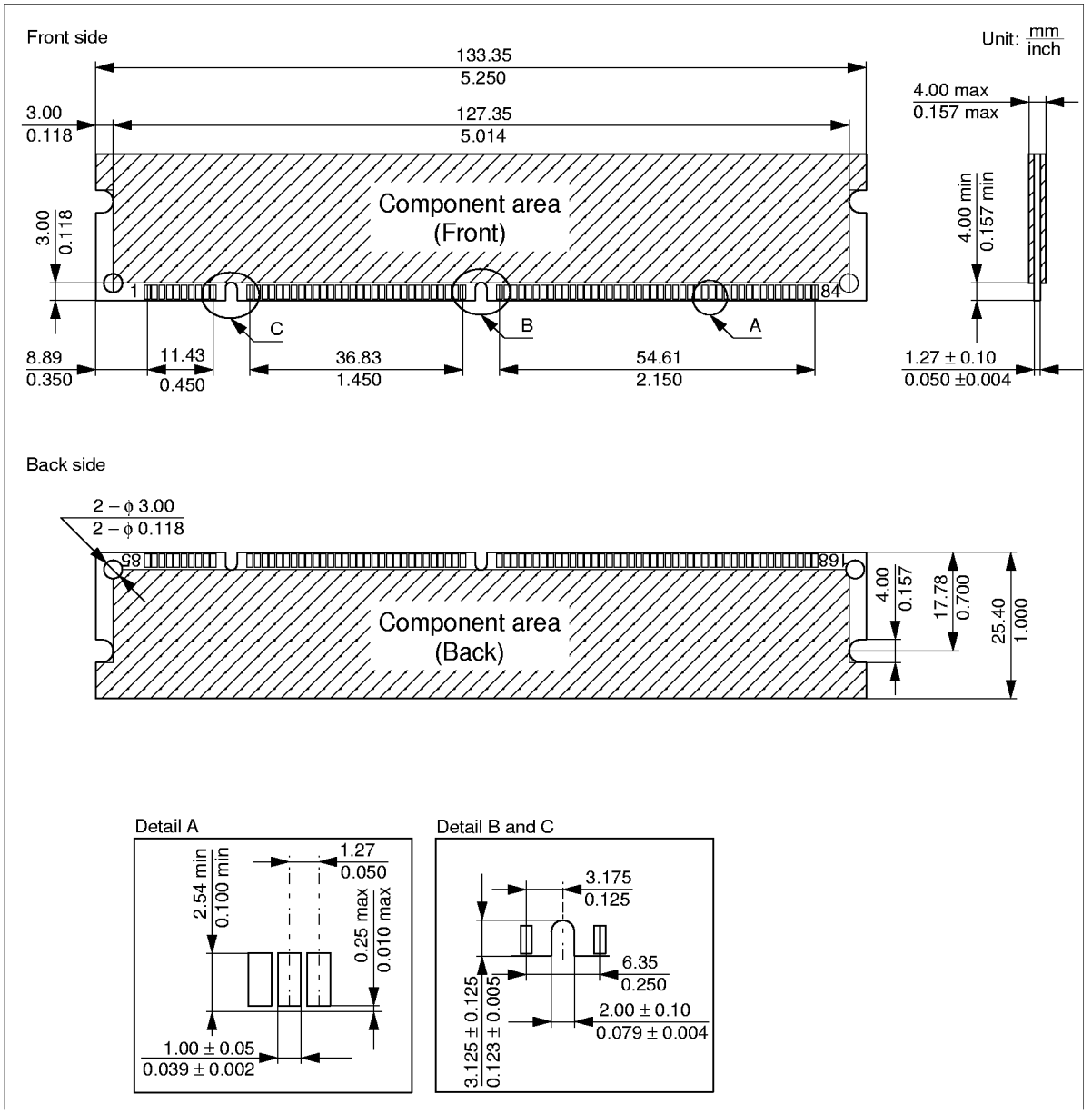


Fast Page Mode Read-Modify-Write Cycle[*18]



Physical Outline

HB56AW873E-A Series



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