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COP620C/COP621C/COP622C/COP640C/COP641C/ COP642C/COP820C/COP821C/COP822C/COP840C/ COP841C/COP842C Single-Chip microCMOS Microcontrollers

General Description

The COP820C and COP840C are members of the COPSTM microcontroller family. They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. This low cost microcontroller is a complete microcomputer containing all system timing, interrupt logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUSTM serial I/O, a 16-bit timer/counter with capture register and a multi-sourced interrupt. Each I/O pin has software selectable options to adapt the COP820C and COP840C to the specific application. The part operates over a voltage range of 2.5 to 6.0V. High throughput is achieved with an efficient, regular instruction set operating at a 1 microsecond per instruction rate. The part may be operated in the ROMless mode to provide for accurate emulation and for applications requiring external program memory.

Features

- Low Cost 8-bit microcontroller
- Fully static CMOS
- 1 μs Instruction time (20 MHz clock)
- Low current drain (2.2 mA at 3 μs Instruction rate)
Low current static HALT mode (Typically < 1 μA)
- Single supply operation: 2.5 to 6.0V
- 1024 bytes ROM/64 Bytes RAM—COP820C
- 2048 bytes ROM/128 Bytes RAM—COP840C

- 16-bit read/write timer operates in a variety of modes
 - Timer with 16-bit auto reload register
 - 16-bit external event counter
 - Timer with 16-bit capture register (selectable edge)
- Multi-source interrupt
 - Reset master clear
 - External interrupt with selectable edge
 - Timer interrupt or capture interrupt
 - Software interrupt
- 8-bit stack pointer (stack in RAM)
- Powerful instruction set, most instructions single byte
- BCD arithmetic instructions
- MICROWIRE PLUSTM serial I/O
- 28 pin package (optionally 24 or 20 pin package)
- 24 input/output pins (28-pin package)
- Software selectable I/O options (TRI-STATE®, push-pull, weak pull-up)
- Schmitt trigger inputs on Port G
- Temperature ranges: -40°C to +85°C, -55°C to +125°C
- ROMless mode for accurate emulation and external program capability—expandable to 32k bytes in ROMless mode
- Form, fit and function EEPROM emulation device (COP8720C)
- Piggyback emulation devices (COP820CP/COP840CP)
- Fully supported by National's MOLETM development system

Block Diagram

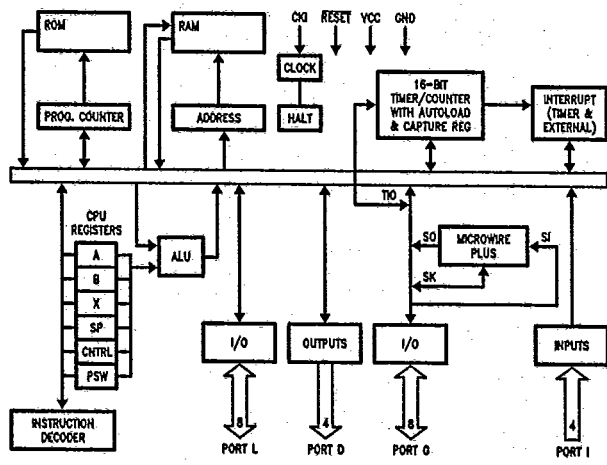


FIGURE 1

TL/DD/8103-1

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

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COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

COP820C/COP821C/COP822C/COP840C/COP841C/COP842C
AC Electrical Characteristics -40°C < T_A < +85°C unless otherwise specified T-49-19-08

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (t _c)					
High Speed Mode (Div-by 20)	V _{CC} ≥ 4.5V	1		DC	μs
	2.5V ≤ V _{CC} < 4.5V	2.5		DC	μs
Normal Mode (Div-by 10)	V _{CC} ≥ 4.5V	2		DC	μs
	2.5V ≤ V _{CC} < 4.5V	5		DC	μs
R/C Oscillator Mode (Div-by 10)	V _{CC} ≥ 4.5V	3		DC	μs
	2.5V ≤ V _{CC} < 4.5V	7.5		DC	μs
CKI Clock Duty Cycle (Note 6)	f _r = Max (+20 Mode)	33		66	%
Rise Time (Note 6)	f _r = 20 MHz Ext Clock			12	ns
Fall Time (Note 6)	f _r = 20 MHz Ext Clock			8	ns
Inputs					
t _{SETUP}	V _{CC} ≥ 4.5V	200			ns
	2.5V ≤ V _{CC} < 4.5V	500			ns
t _{HOLD}	V _{CC} ≥ 4.5V	60			ns
	2.5V ≤ V _{CC} < 4.5V	150			ns
Output Propagation Delay	C _L = 100 pF, R _L = 2.2 kΩ				
t _{PD1} , t _{PD0}	V _{CC} ≥ 4.5V			0.7	μs
SO, SK	2.5V ≤ V _{CC} < 4.5V			1.75	μs
All Others	V _{CC} ≥ 4.5V			1	μs
	2.5V ≤ V _{CC} < 4.5V			2.5	μs
MICROWIRE™ Setup Time (t _{UWS})		20			ns
MICROWIRE Hold Time (t _{UWH})		56			ns
MICROWIRE Output Propagation Delay (t _{UPD})				220	ns
Input Pulse Width					
Interrupt Input High Time		t _c			
Interrupt Input Low Time		t _c			
Timer Input High Time		t _c			
Timer Input Low Time		t _c			
Reset Pulse Width		1.0			μs

Note 6: Parameter sampled but not 100% tested.

AC Electrical Characteristics in ROMless Mode -40°C < T_A < 85°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (t _c)					
High Speed Mode (Div-by 20)	V _{CC} ≥ 4.5V		2	DC	μs
	2.5V ≤ V _{CC} < 4.5V		5	DC	μs
Normal Mode (Div-by 10)	V _{CC} ≥ 4.5V		4	DC	μs
	2.5V ≤ V _{CC} < 4.5V		10	DC	μs
R/C Oscillator Mode	V _{CC} ≥ 4.5V		6	DC	μs
	2.5V ≤ V _{CC} < 4.5V		15	DC	μs
CKI Clock Duty Clock	f _r = Max (+20 Mode)	40		60	%
Rise Time	f _r = 10 MHz Ext Clock		24		ns
Fall Time	f _r = 10 MHz Ext Clock		16		ns
Inputs					
t _{SETUP}	V _{CC} ≥ 4.5V		400		ns
	2.5V ≤ V _{CC} < 4.5V		800		ns
t _{HOLD}	V _{CC} ≥ 4.5V		120		ns
	2.5V ≤ V _{CC} < 4.5V		300		ns
Output Propagation Delay	C _L = 100 pF, R _L = 2.2 kΩ				
t _{PD1} , t _{PD0}	V _{CC} ≥ 4.5V		1.4		μs
SO, SK	2.5V ≤ V _{CC} < 4.5V		3.5		μs
All Others	V _{CC} ≥ 4.5V		2		μs
	2.5V ≤ V _{CC} < 4.5V		5		μs
Minimum Pulse Width					
Interrupt Input		t _c			
Timer Input		t _c			
Reset Pulse Width		1.0			μs

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Absolute Maximum Ratings

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If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Current out of GND Pin (Sink) 48 mA
 Storage Temperature Range -65°C to +140°C
 Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

Supply Voltage (V_{CC}) 6V
 Voltage at any Pin -0.3V to V_{CC} + 0.3V
 ESD Susceptibility (Note 4) 2000V
 Total Current into V_{CC} Pin (Source) 40 mA

DC Electrical Characteristics -55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Operating Voltage		4.5		5.5	V
Power Supply Ripple (Note 1)	Peak to Peak			0.1 V _{CC}	V
Supply Current					
High Speed Mode, CKI = 18 MHz	V _{CC} = 5.5V, t _o = 1.1 μs			15	mA
Normal Mode, CKI = 4.5 MHz	V _{CC} = 5.5V, t _o = 2.2 μs			5	mA
(Note 2)					
HALT Current (Note 3)	V _{CC} = 5.5V, CKI = 0 MHz		<10	30	μA
Input Levels					
RESET, CKI					
Logic High		0.9 V _{CC}			V
Logic Low				0.1 V _{CC}	V
All Other Inputs					
Logic High		0.7 V _{CC}			V
Logic Low				0.2 V _{CC}	V
Hi-Z Input Leakage	V _{CC} = 5.5V	-5		+5	μA
Input Pullup Current	V _{CC} = 4.5V	35		300	μA
G Port Input Hysteresis			0.05 V _{CC}		V
Output Current Levels					
D Outputs					
Source	V _{CC} = 4.5V, V _{OH} = 3.8V	0.35			mA
Sink	V _{CC} = 4.5V, V _{OL} = 1.0V	9			mA
All Others					
Source (Weak Pull-Up)	V _{CC} = 4.5V, V _{OH} = 3.2V	9		120	μA
Source (Push-Pull Mode)	V _{CC} = 4.5V, V _{OH} = 3.8V	0.35			mA
Sink (Push-Pull Mode)	V _{CC} = 4.5V, V _{OL} = 0.4V	1.4			mA
TRI-STATE Leakage		-5.0		+5.0	μA
Allowable Sink/Source Current Per Pin					
D Outputs (Sink)				12	mA
All Others				2.5	mA
Maximum Input Current (Room Temp) Without Latchup (Note 5)	Room Temp			±100	mA
RAM Retention Voltage, V _r	500 ns Rise and Fall Time (Min)	2.5			V
Input Capacitance				7	pF
Load Capacitance on D2				1000	pF

Note 1: Rate of voltage change must be less than 0.5V/ms.

Note 2: Supply current is measured after running 2000 cycles with a square wave CKI input, CKO open, inputs at rails and outputs open.

Note 3: The HALT mode will stop CKI from oscillating in the RC and the Crystal configurations. Test conditions: All inputs tied to V_{CC}; L and G ports TRI-STATE and tied to ground, all outputs low and tied to ground.

Note 4: Human body mode, 100 pF through 1500Ω.

Note 5: Except pins G6, G7, RESET
 pins G6, RESET: +60 mA, -100 mA
 pin G7: +100, -25 mA
 Sampled but not 100% tested.

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C

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AC Electrical Characteristics -55°C < T_A < +125°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (t _c) High Speed Mode (Div-by 20) Normal Mode (Div-by 10)	V _{CC} ≥ 4.5V	1.1		DC	μs
	V _{CC} ≥ 4.5V	2.2		DC	μs
CKI Clock Duty Cycle (Note 6) Rise Time (Note 6) Fall Time (Note 6)	fr = Max (+20 Mode)	33		66	%
	fr = 18 MHz Ext Clock			12	ns
	fr = 18 MHz Ext Clock			8	ns
Inputs t _{SETUP} t _{HOLD}	V _{CC} ≥ 4.5V	220			ns
	V _{CC} ≥ 4.5V	66			ns
Output Propagation Delay t _{PD1} , t _{PD0} SO, SK All Others	R _L = 2.2k, C _L = 100 pF				
	V _{CC} ≥ 4.5V V _{CC} ≥ 4.5V			0.8 1.1	μs μs
MICROWIRE Setup Time (t _{WS}) MICROWIRE Hold Time (t _{WH}) MICROWIRE Output Valid Time (t _{VP})		20			ns
		56			ns
				220	ns
Input Pulse Width Interrupt Input High Time Interrupt Input Low Time Timer Input High Time Timer Input Low Time		t _c			
		t _c			
		t _c			
		t _c			
Reset Pulse Width		1			μs

Note 6: Parameter sampled but not 100% tested.

AC Electrical Characteristics in ROMless Mode -55°C < T_A < +125°C unless otherwise specified

Parameter	Condition	Min	Typ	Max	Units
Instruction Cycle Time (t _c) High Speed Mode (Div-by 20) Normal Mode (Div-by 10)	V _{CC} ≥ 4.5V		2.2	DC	μs
	V _{CC} ≥ 4.5V		4.4	DC	μs
CKI Clock Duty Cycle Rise Time Fall Time	fr = Max (+20 Mode)	40		60	%
	fr = 9 MHz Ext Clock		24		ns
	fr = 9 MHz Ext Clock		16		ns
Inputs t _{SETUP} t _{HOLD}	V _{CC} ≥ 4.5V		440		ns
	V _{CC} ≥ 4.5V		132		ns
Output Propagation Delay t _{PD1} , t _{PD0} SO, SK All Others	R _L = 2.2k, C _L = 100 pF				
	V _{CC} ≥ 4.5V V _{CC} ≥ 4.5V		1.55 2.2		μs μs
Minimum Pulse Width Interrupt Input Timer Input		t _c			
		t _c			
		t _c			
Reset Pulse Width		1			μs

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Timing Diagrams

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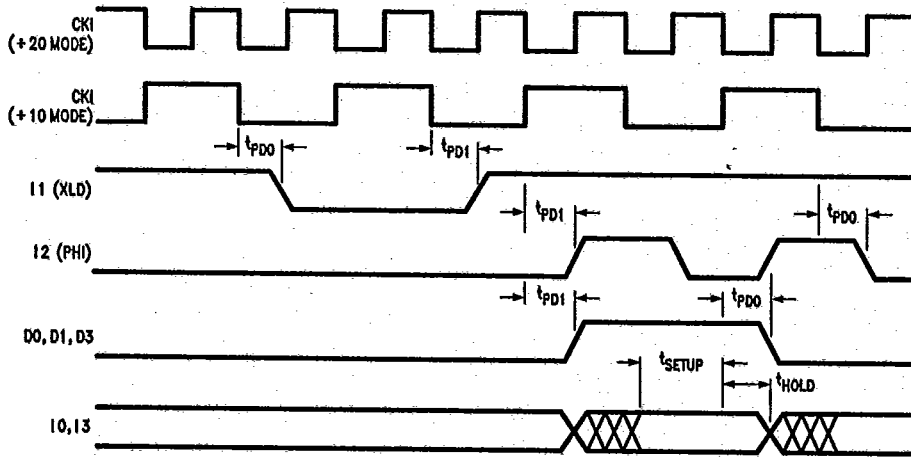


FIGURE 2a. AC Timing Diagrams in ROMless Mode

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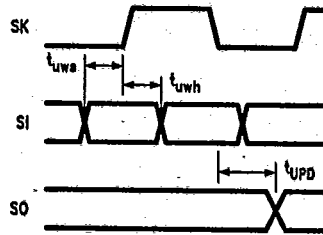


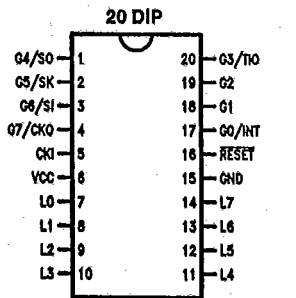
FIGURE 2b. MICROWIRE/PLUS Timing

TL/DD/9103-19

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Connection Diagrams

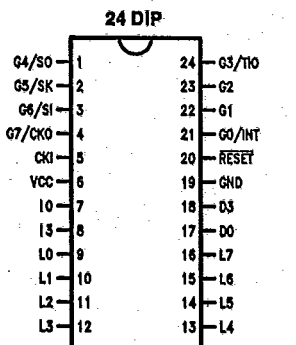
DUAL-IN-LINE PACKAGE



Top View

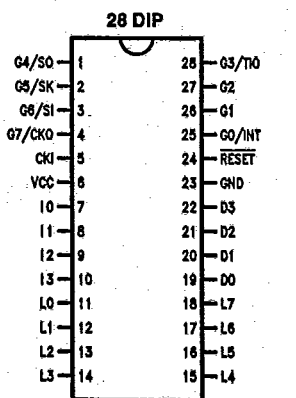
TL/DD/9103-3

Order Number COP822C-XXX/D,
COP822C-XXX/N, COP842C-XXX/D
or COP842C-XXX/N
See NS Package Number
D20A or N20A



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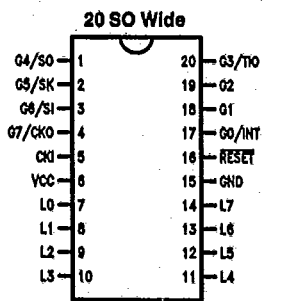
Order Number COP821C-XXX/D,
COP821C-XXX/N, COP841C-XXX/D
or COP841C-XXX/N
See NS Package Number
D24C or N24A



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Order Number COP820C-XXX/D,
COP820C-XXX/N, COP840C-XXX/D
or COP840C-XXX/N
See NS Package Number
D28C or N28B

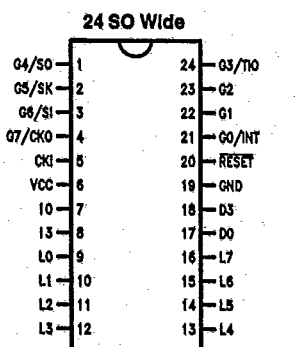
SURFACE MOUNT



Top View

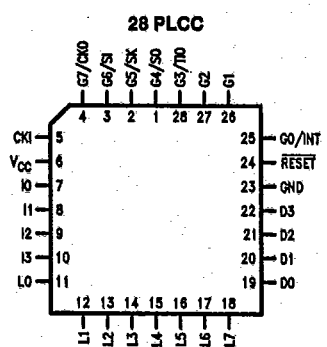
TL/DD/9103-3

Order Number COP822C-XXX/WM
or COP842C-XXX/WM
See NS Package Number M20B



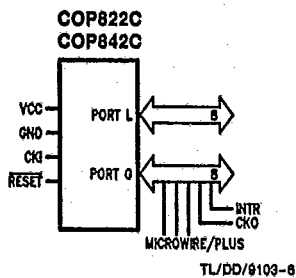
TL/DD/9103-4

Order Number COP821C-XXX/WM
or COP841C-XXX/WM
See NS Package Number M24B

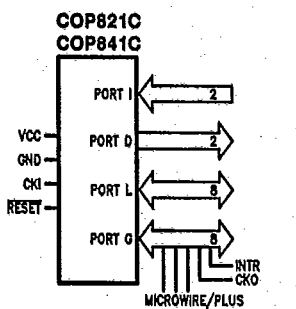


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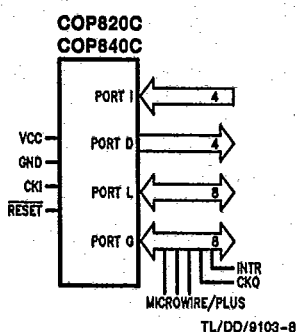
Order Number COP820C-XXX/V or
COP840C-XXX/V
See NS Package Number V28A



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TL/DD/9103-7



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FIGURE 3

COP820C/COP821C/COP822C/COP840C/COP841C/COP842C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

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Pin Descriptions

V_{CC} and GND are the power supply pins.
 CKI is the clock input. This can come from an external source, a R/C generated oscillator or a crystal (in conjunction with CKO). See Oscillator description.
 RESET is the master reset input. See Reset description.
 PORT I is a four bit Hi-Z input port.
 PORT L is an 8-bit I/O port.
 There are two registers associated with each L I/O port: a data register and a configuration register. Therefore, each L I/O bit can be individually configured under software control as shown below:

Port L Config.	Port L Data	Port L Setup
0	0	Hi-Z Input (TRI-STATE)
0	1	Input With Weak Pull-Up
1	0	Push-Pull "0" Output
1	1	Push-Pull "1" Output

Three data memory address locations are allocated for these ports, one for data register, one for configuration register and one for the input pins.

PORT G is an 8-bit port with 6 I/O pins (G0-G5) and 2 input pins (G6, G7). All eight G-pins have Schmitt Triggers on the inputs. The G7 pin functions as an input pin under normal operation and as the continue pin to exit the HALT mode. There are two registers with each I/O port: a data register and a configuration register. Therefore, each I/O bit can be individually configured under software control as shown below.

Port G Config.	Port G Data	Port G Setup
0	0	Hi-Z Input (TRI-STATE)
0	1	Input With Weak Pull-Up
1	0	Push-Pull "0" Output
1	1	Push-Pull "1" Output

Three data memory address locations are allocated for these ports, one for data register, one for configuration register and one for the input pins. Since G6 and G7 are input only pins, any attempt by the user to set them up as outputs by writing a one to the configuration register will be disregarded. Reading the G6 and G7 configuration bits will return zeros. Note that the chip will be placed in the HALT mode by setting the G7 data bit.

Six bits of Port G have alternate features:
 G0 INTR (an external interrupt)
 G3 TIO (timer/counter input/output)
 G4 SO (MICROWIRE serial data output)
 G5 SK (MICROWIRE clock I/O)
 G6 SI (MICROWIRE serial data input)
 G7 CKO crystal oscillator output (selected by mask option) or HALT restart input (general purpose input)
 Pins G1 and G2 currently do not have any alternate functions.
 PORT D is a four bit output port that is set high when RESET goes low.
 The D2 pin is sampled at reset. If it is held low at reset the COP820C/COP840C enters the ROMless mode of operation.

Functional Description

Figure 1 shows the block diagram of the internal architecture. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device.

ALU AND CPU REGISTERS

The ALU can do an 8-bit addition, subtraction, logical or shift operation in one cycle time.

There are five CPU registers: T-49-19-08

A is the 15-bit Program Counter register
 PU is the upper 7 bits of the program counter (PC)
 PL is the lower 8 bits of the program counter (PC)
 B is the 8-bit address register, can be auto incremented or decremented.
 X is the 8-bit alternate address register, can be incremented or decremented.
 SP is the 8-bit stack pointer, points to subroutine stack (in RAM).

B, X and SP registers are mapped into the on chip RAM. The B and X registers are used to address the on chip RAM. The SP register is used to address the stack in RAM during subroutine calls and returns.

PROGRAM MEMORY

Program memory for the COP820C consists of 1024 bytes of ROM (2048 bytes of ROM for the COP840C). These bytes may hold program instructions or constant data. The program memory is addressed by the 15-bit program counter (PC). ROM can be indirectly read by the LAID instruction for table lookup.

DATA MEMORY

The data memory address space includes on chip RAM, I/O and registers. Data memory is addressed directly by the instruction or indirectly by the B, X and SP registers.

The COP820C has 64 bytes of RAM and the COP840C has 128 bytes of RAM. Sixteen bytes of RAM are mapped as "registers" that can be loaded immediately, decremented or tested. Three specific registers: B, X and SP are mapped into this space, the other bytes are available for general usage.

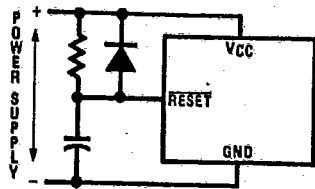
The instruction set permits any bit in memory to be set, reset or tested. All I/O and registers (except the A & PC) are memory mapped; therefore, I/O bits and register bits can be directly and individually set, reset and tested.

RESET

The RESET input when pulled low initializes the microcontroller. Initialization will occur whenever the RESET input is pulled low. Upon initialization, the ports L and G are placed in the TRI-STATE mode and the Port D is set high. The PC, PSW and CNTRL registers are cleared. The data and configuration registers for Ports L & G are cleared.

The external RC network shown in Figure 4 should be used to ensure that the RESET pin is held low until the power supply to the chip stabilizes.

Functional Description (Continued)



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RC ≥ 5X Power Supply Rise Time

FIGURE 4. Recommended Reset Circuit

OSCILLATOR CIRCUITS

Figure 5 shows the three clock oscillator configurations available for the COP820C and COP840C.

A. CRYSTAL OSCILLATOR

The COP820C/COP840C can be driven by a crystal clock. The crystal network is connected between the pins CKI and CKO.

Table I shows the component values required for various standard crystal values.

B. EXTERNAL OSCILLATOR

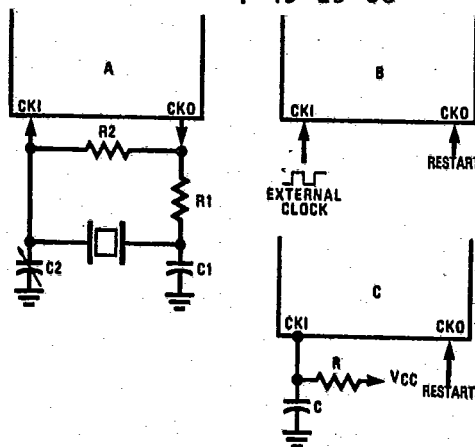
CKI can be driven by an external clock signal. CKO is available as a general purpose input and/or HALT restart control.

C. R/C OSCILLATOR

CKI is configured as a single pin RC controlled Schmitt trigger oscillator. CKO is available as a general purpose input and/or HALT restart control.

Table II shows the variation in the oscillator frequencies as functions of the component (R and C) values.

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FIGURE 5. Crystal and R-C Connection Diagrams

OSCILLATOR MASK OPTIONS

The COP820C and COP840C can be driven by clock inputs between DC and 20 MHz. For low input clock frequencies (≤ 5 MHz) the instruction cycle frequency can be selected to be the input clock frequency divided by 10. This mode is known as the Normal Mode.

For oscillator frequencies that are greater than 5 MHz the chip must run with a divide by 20. This is known as the High Speed mode.

TABLE I. Crystal Oscillator Configuration, T_A = 25°C

R1 (kΩ)	R2 (MΩ)	C1 (pF)	C2 (pF)	CKI Freq (MHz)	Conditions
0	1	30	30-36	20	V _{CC} = 5V
0	1	30	30-36	10	V _{CC} = 5V
0	1	30	30-36	4 (+ 20)	V _{CC} = 2.5V
0	1	200	100-150	0.455	V _{CC} = 2.5V

TABLE II. RC Oscillator Configuration, T_A = 25°C

R (kΩ)	C (pF)	CKI Freq. (MHz)	Instr. Cycle (μs)	Conditions
3.3	82	2.8 to 2.2	3.6 to 4.5	V _{CC} = 5V
5.6	100	1.5 to 1.1	6.7 to 9	V _{CC} = 5V
6.8	100	1.1 to 0.8	9 to 12.5	V _{CC} = 2.5V

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COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

Functional Description (Continued)

The COP820C and COP840C microcontrollers have five mask options for configuring the clock input. The CKI and CKO pins are automatically configured upon selecting a particular option.

- High Speed Crystal (CKI/20) CKO for crystal configuration
- Normal Mode Crystal (CKI/10) CKO for crystal configuration
- High Speed External (CKI/20) CKO available as G7 input
- Normal Mode External (CKI/10) CKO available as G7 input
- R/C (CKI/10) CKO available as G7 input

G7 can be used either as a general purpose input or as a control input to continue from the HALT mode.

CURRENT DRAIN

The total current drain of the chip depends on:

- 1) Oscillator operating mode—I1
- 2) Internal switching current—I2
- 3) Internal leakage current—I3
- 4) Output source current—I4
- 5) DC current caused by external input not at V_{CC} or GND—I5

Thus the total current drain, It is given as

$$I_t = I_1 + I_2 + I_3 + I_4 + I_5$$

To reduce the total current drain, each of the above components must be minimum.

The chip will draw the least current when in the normal mode. The high speed mode will draw additional current. The R/C mode will draw the most. Operating with a crystal network will draw more current than an external square-wave. Switching current, governed by the equation below, can be reduced by lowering voltage and frequency. Leakage current can be reduced by lowering voltage and temperature. The other two items can be reduced by carefully designing the end-user's system.

$$I_2 = C \times V \times f$$

Where

C = equivalent capacitance of the chip.

V = operating voltage

f = CKI frequency

Some sample current drain values at V_{CC} = 6V are:

CKI (MHz)	Inst. Cycle (μs)	I _t (mA)
20	1	9
3.58	3	2.2
2	5	1.2
0.3	33	0.2
0 (HALT)	—	<0.0001

HALT MODE

The COP820C and COP840C support a power saving mode of operation: HALT. The controller is placed in the HALT mode by setting the G7 data bit, alternatively the user can stop the clock input. In the HALT mode all internal processor activities including the clock oscillator are stopped. The fully static architecture freezes the state of the control

ler and retains all information until continuing. In the HALT mode, power requirements are minimal as it draws only leakage currents and output current. The applied voltage (V_{CC}) may be decreased down to V_r (minimum RAM retention voltage) without altering the state of the machine.

There are two ways to exit the HALT mode: via the RESET or by the CKO pin. A low on the RESET line reinitializes the microcontroller and starts executing from the address 0000H. A low to high transition on the CKO pin causes the microcontroller to continue with no reinitialization from the address following the HALT instruction. This also resets the G7 data bit.

INTERRUPTS

The COP820C and COP840C have a sophisticated interrupt structure to allow easy interface to the real world. There are three possible interrupt sources, as shown below.

A maskable interrupt on external G0 input (positive or negative edge sensitive under software control)

A maskable interrupt on timer carry or timer capture

A non-maskable software/error interrupt on opcode zero

INTERRUPT CONTROL

The GIE (global interrupt enable) bit enables the interrupt function. This is used in conjunction with ENI and ENTI to select one or both of the interrupt sources. This bit is reset when interrupt is acknowledged.

ENI and ENTI bits select external and timer interrupt respectively. Thus the user can select either or both sources to interrupt the microcontroller when GIE is enabled.

IEDG selects the external interrupt edge (0 = rising edge, 1 = falling edge). The user can get an interrupt on both rising and falling edges by toggling the state of IEDG bit after each interrupt.

IPND and TPND bits signal which interrupt is pending. After interrupt is acknowledged, the user can check these two bits to determine which interrupt is pending. This permits the interrupts to be prioritized under software. The pending flags have to be cleared by the user. Setting the GIE bit high inside the interrupt subroutine allows nested interrupts.

The software interrupt does not reset the GIE bit. This means that the controller can be interrupted by other interrupt sources while servicing the software interrupt.

INTERRUPT PROCESSING

The interrupt, once acknowledged, pushes the program counter (PC) onto the stack and the stack pointer (SP) is decremented twice. The Global Interrupt Enable (GIE) bit is reset to disable further interrupts. The microcontroller then vectors to the address 00FFH and resumes execution from that address. This process takes 7 cycles to complete. At the end of the interrupt subroutine, any of the following three instructions return the processor back to the main program: RET, RETSK or RETI. Either one of the three instructions will pop the stack into the program counter (PC). The stack pointer is then incremented twice. The RETI instruction additionally sets the GIE bit to re-enable further interrupts.

Any of the three instructions can be used to return from a hardware interrupt subroutine. The RETSK instruction should be used when returning from a software interrupt subroutine to avoid entering an infinite loop.

Functional Description (Continued)

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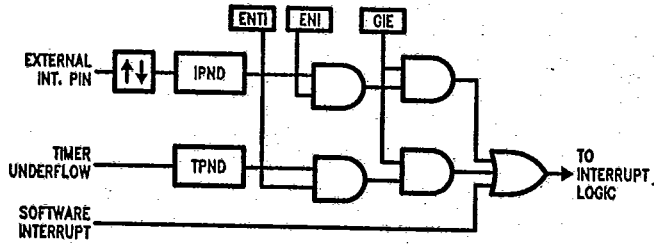


FIGURE 6. Interrupt Block Diagram

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DETECTION OF ILLEGAL CONDITIONS

The COP820C and COP840C incorporate a hardware mechanism that allows it to detect illegal conditions which may occur from coding errors, noise and 'brown out' voltage drop situations. Specifically it detects cases of executing out of undefined ROM area and unbalanced stack situations.

Reading an undefined ROM location returns 00 (hexadecimal) as its contents. The opcode for a software interrupt is also '00'. Thus a program accessing undefined ROM will cause a software interrupt.

Reading an undefined RAM location returns an FF (hexadecimal). The subroutine stack on the COP820C and COP840C grows down for each subroutine call. By initializing the stack pointer to the top of RAM, the first unbalanced return instruction will cause the stack pointer to address undefined RAM. As a result the program will attempt to execute from FFFF (hexadecimal), which is an undefined ROM location and will trigger a software interrupt.

MICROWIRE/PLUSTM

MICROWIRE/PLUS is a serial synchronous bidirectional communications interface. The MICROWIRE/PLUS capability enables the COP820C and COP840C to interface with any of National Semiconductor's MICROWIRE peripherals (i.e. A/D converters, display drivers, EEPROMS, etc.) and with other microcontrollers which support the MICROWIRE/PLUS interface. It consists of an 8-bit serial shift register (SIO) with serial data input (SI), serial data output (SO) and serial shift clock (SK). Figure 7 shows the block diagram of the MICROWIRE/PLUS interface.

The shift clock can be selected from either an internal source or an external source. Operating the MICROWIRE/PLUS interface with the internal clock source is called the Master mode of operation. Similarly, operating the MICROWIRE/PLUS interface with an external shift clock is called the Slave mode of operation.

The CNTRL register is used to configure and control the MICROWIRE/PLUS mode. To use the MICROWIRE/PLUS, the MSEL bit in the CNTRL register is set to one. The SK clock rate is selected by the two bits, S0 and S1, in the CNTRL register. Table III details the different clock rates that may be selected.

TABLE III

S1	S0	SK Cycle Time
0	0	2t _c
0	1	4t _c
1	x	8t _c

where,
t_c is the instruction cycle clock.

MICROWIRE/PLUS OPERATION

Setting the BUSY bit in the PSW register causes the MICROWIRE/PLUS arrangement to start shifting the data. It gets reset when eight data bits have been shifted. The user may reset the BUSY bit by software to allow less than 8 bits to shift. The COP820C and COP840C may enter the MICROWIRE/PLUS mode either as a Master or as a Slave. Figure 8 shows how two COP820C microcontrollers and several peripherals may be interconnected using the MICROWIRE/PLUS arrangement.

Master MICROWIRE/PLUS Operation

In the MICROWIRE/PLUS Master mode of operation the shift clock (SK) is generated internally by the COP820C. The MICROWIRE/PLUS Master always initiates all data exchanges. (See Figure 8). The MSEL bit in the CNTRL register must be set to enable the SO and SK functions onto the G Port. The SO and SK pins must also be selected as outputs by setting appropriate bits in the Port G configuration register. Table IV summarizes the bit settings required for Master mode of operation.

SLAVE MICROWIRE/PLUS OPERATION

In the MICROWIRE/PLUS Slave mode of operation the SK clock is generated by an external source. Setting the MSEL bit in the CNTRL register enables the SO and SK functions onto the G Port. The SK pin must be selected as an input and the SO pin is selected as an output pin by appropriately setting up the Port G configuration register. Table IV summarizes the settings required to enter the Slave mode of operation.

The user must set the BUSY flag immediately upon entering the Slave mode. This will ensure that all data bits sent by the Master will be shifted properly. After eight clock pulses the BUSY flag will be cleared and the sequence may be repeated. (See Figure 8.)

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

2

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP620C/COP621C/COP622C/COP640C/COP641C/COP642C

Functional Description (Continued)

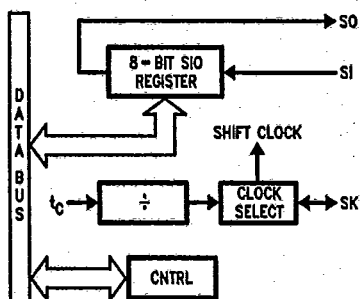
T-49-19-08

TABLE IV

G4 Config. Bit	G5 Config. Bit	G4 Fun.	G5 Fun.	G6 Fun.	Operation
1	1	SO	Int. SK	SI	MICROWIRE Master
0	1	TRI-STATE	Int. SK	SI	MICROWIRE Master
1	0	SO	Ext. SK	SI	MICROWIRE Slave
0	0	TRI-STATE	Ext. SK	SI	MICROWIRE Slave

TIMER/COUNTER

The COP820C and COP840C have a powerful 16-bit timer with an associated 16-bit register enabling them to perform extensive timer functions. The timer T1 and its register R1 are each organized as two 8-bit read/write registers. Control bits in the register CNTRL allow the timer to be started and stopped under software control. The timer-register pair can be operated in one of three possible modes. Table V details various timer operating modes and their requisite control settings.



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FIGURE 7. MICROWIRE/PLUS Block Diagram

MODE 1. TIMER WITH AUTO-LOAD REGISTER

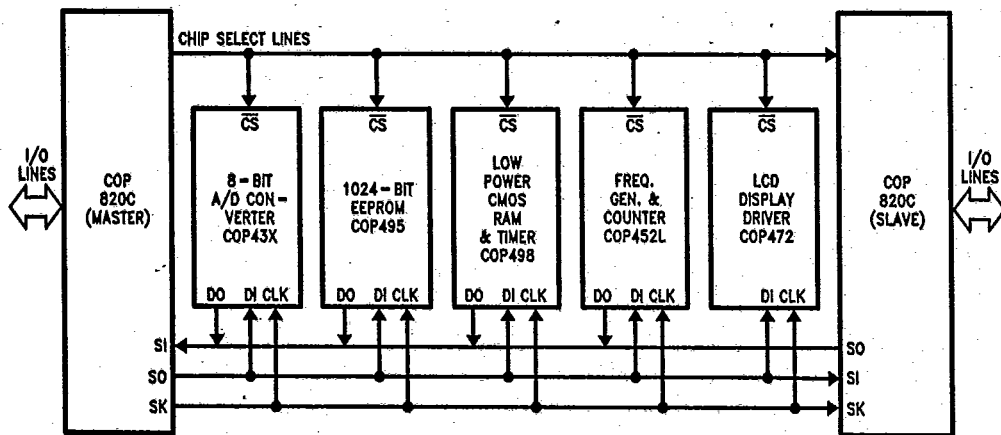
In this mode of operation, the timer T1 counts down at the instruction cycle rate. Upon underflow the value in the register R1 gets automatically reloaded into the timer which continues to count down. The timer underflow can be programmed to interrupt the microcontroller. A bit in the control register CNTRL enables the TIO (G3) pin to toggle upon timer underflows. This allows the generation of square-wave outputs or pulse width modulated outputs under software control. (See Figure 9)

MODE 2. EXTERNAL COUNTER

In this mode, the timer T1 becomes a 16-bit external event counter. The counter counts down upon an edge on the TIO pin. Control bits in the register CNTRL program the counter to decrement either on a positive edge or on a negative edge. Upon underflow the contents of the register R1 are automatically copied into the counter. The underflow can also be programmed to generate an interrupt. (See Figure 9)

MODE 3. TIMER WITH CAPTURE REGISTER

Timer T1 can be used to precisely measure external frequencies or events in this mode of operation. The timer T1 counts down at the instruction cycle rate. Upon the occurrence of a specified edge on the TIO pin the contents of the timer T1 are copied into the register R1. Bits in the control register CNTRL allow the trigger edge to be specified either as a positive edge or as a negative edge. In this mode the user can elect to be interrupted on the specified trigger edge. (See Figure 10.)



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FIGURE 8. MICROWIRE/PLUS Application

Functional Description (Continued)

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TABLE V. Timer Operating Modes

CNTRL Bits 765	Operation Mode	T Interrupt	Timer Counts On
000	External Counter W/Auto-Load Reg.	Timer Carry	TIO Pos. Edge
001	External Counter W/Auto-Load Reg.	Timer Carry	TIO Neg. Edge
010	Not Allowed	Not Allowed	Not Allowed
011	Not Allowed	Not Allowed	Not Allowed
100	Timer W/Auto-Load Reg.	Timer Carry	t_c
101	Timer W/Auto-Load Reg./Toggle TIO Out	Timer Carry	t_c
110	Timer W/Capture Register	TIO Pos. Edge	t_c
111	Timer W/Capture Register	TIO Neg. Edge	t_c

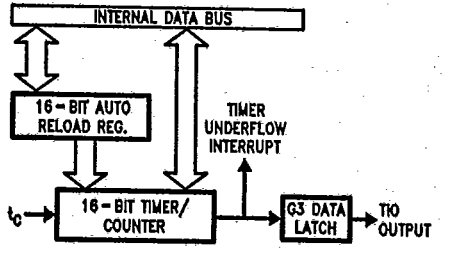


FIGURE 9. Timer/Counter Auto Reload Mode Block Diagram

TIMER PWM APPLICATION

Figure 11 shows how a minimal component D/A converter can be built out of the Timer-Register pair in the Auto-Reload mode. The timer is placed in the "Timer with auto reload" mode and the TIO pin is selected as the timer output. At the outset the TIO pin is set high, the timer T1 holds the on time and the register R1 holds the signal off time. Setting TRUN bit starts the timer which counts down at the instruction cycle rate. The underflow toggles the TIO output and copies the off time into the timer, which continues to run. By alternately loading in the on time and the off time at each successive interrupt a PWM frequency can be easily generated.

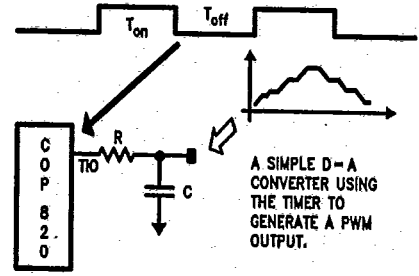


FIGURE 11. Timer Application

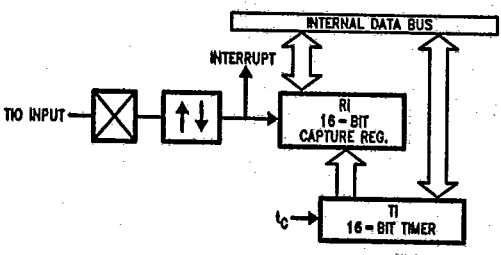


FIGURE 10. Timer Capture Mode Block Diagram

COP820C/COP821C/COP822C/COP840C/COP841C/COP842C/COP8820C/COP8821C/COP8822C/COP8840C/COP8841C/COP8842C

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

Control Registers

CNTRL REGISTER (ADDRESS X'00EE)

The Timer and MICROWIRE/PLUS control register contains the following bits:

- S1 & S0 Select the MICROWIRE/PLUS clock divide-by
- IEDG External interrupt edge polarity select (0 = rising edge, 1 = falling edge)
- MSEL Enable MICROWIRE/PLUS functions SO and SK
- TRUN Start/Stop the Timer/Counter (1 = run, 0 = stop)
- TC3 Timer input edge polarity select (0 = rising edge, 1 = falling edge)
- TC2 Selects the capture mode
- TC1 Selects the timer mode

TC1	TC2	TC3	TRUN	MSEL	IEDG	S1	S0
BIT 7							BIT 0

PSW REGISTER (ADDRESS X'00EF)

The PSW register contains the following select bits:

- GIE Global interrupt enable
- ENI External interrupt enable
- BUSY MICROWIRE/PLUS busy shifting
- IPND External interrupt pending
- ENTI Timer interrupt enable
- TPND Timer interrupt pending
- C Carry Flag
- HC Half carry Flag

HC	C	TPND	ENTI	IPND	BUSY	ENI	GIE
BIT 7							BIT 0

Operating Modes

These controllers have two operating modes: Single Chip mode and the ROMless mode. The operating mode is determined by the state of the D2 pin at power on reset.

SINGLE CHIP MODE

In the Single Chip mode, the controller functions as a self contained microcontroller. It can address internal RAM and ROM. All ports configured as memory mapped I/O ports.

ROMLESS MODE

The COP820C and COP840C enter the ROMless mode of operation if the D2 pin is held at logical "0" at reset. In this case the internal ROM is disabled and the controller can now address up to 32 kbytes of external program memory. In the ROMless mode of operation, the COP820C uses the 64 bytes of onboard RAM and the COP840C uses the 128 bytes of onboard RAM. The ports D and I are used to access the external program memory. By providing a serial interface to external program memory, a large address space can be managed without the penalty of losing a large number of I/O pins in the process. *Figure 12* shows in schematic form the logic required for the ROMless mode operation and all support logic required to recreate the I/O.

Memory Map

All RAM, ports and registers (except A and PC) are mapped into data memory address space.

Address	Contents
COP820C	
00 to 2F	On Chip RAM Bytes T-49-19-08
30 to 7F	Unused RAM Address Space (Reads as all Ones)
COP840C	
00 to 6F	On Chip RAM Bytes
70 to 7F	Unused RAM Address Space (Reads as all Ones)
COP820C and COP840C	
80 to BF	Expansion Space for on Chip EERAM
C0 to CF	Expansion Space for I/O and Registers
D0 to DF	On Chip I/O and Registers
D0	Port L Data Register
D1	Port L Configuration Register
D2	Port L Input Pins (Read Only)
D3	Reserved for Port L
D4	Port G Data Register
D5	Port G Configuration Register
D6	Port G Input Pins (Read Only)
D7	Port I Input Pins (Read Only)
D8-DB	Reserved for Port C
DC	Port D Data Register
DD-DF	Reserved for Port D
E0 to EF	On Chip Functions and Registers
E0-E7	Reserved for Future Parts
E8	Reserved
E9	MICROWIRE/PLUS Shift Register
EA	Timer Lower Byte
EB	Timer Upper Byte
EC	Timer Autoload Register Lower Byte
ED	Timer Autoload Register Upper Byte
EE	CNTRL Control Register
EF	PSW Register
F0 to FF	On Chip RAM Mapped as Registers
FC	X Register
FD	SP Register
FE	B Register

Reading unused memory locations below 7FH will return all ones. Reading other unused memory locations will return undefined data.

Addressing Modes

REGISTER INDIRECT

This is the "normal" mode of addressing for COP820C and COP840C. The operand is the memory addressed by the B register or X register.

DIRECT

The instruction contains an 8-bit address field that directly points to the data memory for the operand.

IMMEDIATE

The instruction contains an 8-bit immediate field as the operand.

REGISTER INDIRECT (AUTO INCREMENT AND DECREMENT)

This is a register indirect mode that automatically increments or decrements the B or X register after executing the instruction.

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP821C/COP822C/COP840C/COP841C/COP842C

Addressing Modes (Continued)

RELATIVE

This mode is used for the JP instruction, the instruction field is added to the program counter to get the new program location. JP has a range of from -31 to +32 to allow a one byte relative jump (JP + 1 is implemented by a NOP instruction). There are no 'pages' when using JP, all 15 bits of PC are used.

Instruction Set

REGISTER AND SYMBOL DEFINITIONS

Registers

- A 8-bit Accumulator register
- B 8-bit Address register
- X 8-bit Address register
- SP 8-bit Stack pointer register

- PC 15-bit Program counter register
- PU upper 7 bits of PC
- PL lower 8 bits of PC
- C 1-bit of PSW register for carry
- HC Half Carry
- GIE 1-bit of PSW register for global interrupt enable

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Symbols

- [B] Memory indirectly addressed by B register
- [X] Memory indirectly addressed by X register
- Mem Direct address memory or [B]
- MemI Direct address memory or [B] or Immediate data
- Imm 8-bit Immediate data
- Reg Register memory; addresses F0 to FF (Includes B, X and SP)
- Bit Bit number (0 to 7)
- ← Loaded with
- ↔ Exchanged with

Instruction Set

ADD ADC SUBC AND OR XOR IFEQ IFGT IFBNE DRSZ SBIT RBIT IFBIT	add add with carry subtract with carry Logical AND Logical OR Logical Exclusive-OR IF equal IF greater than IF B not equal Decrement Reg. skip if zero Set bit Reset bit If bit	A ← A + MemI A ← A + MemI + C, C ← Carry HC ← Half Carry A ← A + MemI + C, C ← Carry HC ← Half Carry A ← A and MemI A ← A or MemI A ← A xor MemI Compare A and MemI, Do next if A = MemI Compare A and MemI, Do next if A > MemI Do next if lower 4 bits of B ≠ Imm Reg ← Reg - 1, skip if Reg goes to 0 1 to bit, Mem (bit = 0 to 7 Immediate) 0 to bit, Mem If bit, Mem is true, do next instr.
X LDA LD mem LD Reg	Exchange A with memory Load A with memory Load Direct memory Immed. Load Register memory Immed.	A ↔ Mem A ← MemI Mem ← Imm Reg ← Imm
X X LDA LDA LDM	Exchange A with memory [B] Exchange A with memory [X] Load A with memory [B] Load A with memory [X] Load Memory Immediate	A ↔ [B] (B ← B ± 1) A ↔ [X] (X ← X ± 1) A ← [B] (B ← B ± 1) A ← [X] (X ← X ± 1) [B] ← Imm (B ← B ± 1)
CLRA INCA DECA LAID DCORA RRCA SWAPA SC RC IFC IFNC	Clear A Increment A Decrement A Load A indirect from ROM DECIMAL CORRECT A ROTATE A RIGHT THRU C Swap nibbles of A Set C Reset C If C If not C	A ← 0 A ← A + 1 A ← A - 1 A ← ROM(PU,A) A ← BCD correction (follows ADC, SUBC) C → A7 → ... → A0 → C A7 ... A4 ↔ A3 ... A0 C ← 1, HC ← 1 C ← 0, HC ← 0 If C is true, do next instruction If C is not true, do next instruction
JMPL JMP JP JSRL JSR JID RET RETSK RETI INTR NOP	Jump absolute long Jump absolute Jump relative short Jump subroutine long Jump subroutine Jump indirect Return from subroutine Return and Skip Return from Interrupt Generate an Interrupt No operation	PC ← II (II = 15 bits, 0 to 32k) PC11..0 ← I (I = 12 bits) PC ← PC + r (r is -31 to +32, not 1) [SP] ← PL, [SP-1] ← PU, SP-2, PC ← II [SP] ← PL, [SP-1] ← PU, SP-2, PC11..0 ← I PL ← ROM(PU,A) SP+2, PL ← [SP], PU ← [SP-1] SP+2, PL ← [SP], PU ← [SP-1], Skip next instruction SP+2, PL ← [SP], PU ← [SP-1], GIE ← 1 [SP] ← PL, [SP-1] ← PU, SP-2, PC ← OFF PC ← PC + 1

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OPCODE LIST

Bits 3-0

Bits 7-4

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
JP-15	JP-31	LD 0F0, #i	DRSZ 0F0	RRCA	RC	ADCA, #i	ADCA, [B]	IFBIT 0, [B]	*	LD B, 0F	IFBNE 0	JSR 0000-00FF	JMP 0000-00FF	JP + 17	INTR
JP-14	JP-30	LD 0F1, #i	DRSZ 0F1	*	SC	SUBCA, #i	SUBC A, [B]	IFBIT 1, [B]	*	LD B, 0E	IFBNE 1	JSR 0100-01FF	JMP 0100-01FF	JP + 18	JP + 2
JP-13	JP-29	LD 0F2, #i	DRSZ 0F2	X A, [X+]	X A, [B+]	IFEQA, #i	IFEQ A, [B]	IFBIT 2, [B]	*	LD B, 0D	IFBNE 2	JSR 0200-02FF	JMP 0200-02FF	JP + 19	JP + 3
JP-12	JP-28	LD 0F3, #i	DRSZ 0F3	X A, [X-]	X A, [B-]	IFGTA, #i	IFGT A, [B]	IFBIT 3, [B]	*	LD B, 0C	IFBNE 3	JSR 0300-03FF	JMP 0300-03FF	JP + 20	JP + 4
JP-11	JP-27	LD 0F4, #i	DRSZ 0F4	*	LAID	ADD A, #i	ADD A, [B]	IFBIT 4, [B]	CLRA	LD B, 0B	IFBNE 4	JSR 0400-04FF	JMP 0400-04FF	JP + 21	JP + 5
JP-10	JP-26	LD 0F5, #i	DRSZ 0F5	*	JID	AND A, #i	AND A, [B]	IFBIT 5, [B]	SWAPA	LD B, 0A	IFBNE 5	JSR 0500-05FF	JMP 0500-05FF	JP + 22	JP + 6
JP-9	JP-25	LD 0F6, #i	DRSZ 0F6	X A, [X]	X A, [B]	XOR A, #i	XOR A, [B]	IFBIT 6, [B]	DCORA	LD B, 9	IFBNE 6	JSR 0600-06FF	JMP 0600-06FF	JP + 23	JP + 7
JP-8	JP-24	LD 0F7, #i	DRSZ 0F7	*	*	ORA, #i	OR A, [B]	IFBIT 7, [B]	*	LD B, 8	IFBNE 7	JSR 0700-07FF	JMP 0700-07FF	JP + 24	JP + 8
JP-7	JP-23	LD 0F8, #i	DRSZ 0F8	NOP	*	LD A, #i	IFC	SBIT 0, [B]	RBIT 0, [B]	LD B, 7	IFBNE 8	JSR 0800-08FF	JMP 0800-08FF	JP + 25	JP + 9
JP-6	JP-22	LD 0F9, #i	DRSZ 0F9	*	*	*	IFNC	SBIT 1, [B]	RBIT 1, [B]	LD B, 6	IFBNE 9	JSR 0900-09FF	JMP 0900-09FF	JP + 26	JP + 10
JP-5	JP-21	LD 0FA, #i	DRSZ 0FA	LD A, [X+]	LD A, [B+]	LD [B+], #i	INCA	SBIT 2, [B]	RBIT 2, [B]	LD B, 5	IFBNE 0A	JSR 0A00-0AFF	JMP 0A00-0AFF	JP + 27	JP + 11
JP-4	JP-20	LD 0FB, #i	DRSZ 0FB	LD A, [X-]	LD A, [B-]	LD [B-], #i	DECA	SBIT 3, [B]	RBIT 3, [B]	LD B, 4	IFBNE 0B	JSR 0B00-0BFF	JMP 0B00-0BFF	JP + 28	JP + 12
JP-3	JP-19	LD 0FC, #i	DRSZ 0FC	LD Md, #i	JMPL #i	X A, Md	*	SBIT 4, [B]	RBIT 4, [B]	LD B, 3	IFBNE 0C	JSR 0C00-0CFF	JMP 0C00-0CFF	JP + 29	JP + 13
JP-2	JP-18	LD 0FD, #i	DRSZ 0FD	DIR	JSRL	LD A, Md	RETSK	SBIT 5, [B]	RBIT 5, [B]	LD B, 2	IFBNE 0D	JSR 0D00-0DFF	JMP 0D00-0DFF	JP + 30	JP + 14
JP-1	JP-17	LD 0FE, #i	DRSZ 0FE	LD A, [X]	LD A, [B]	LD [B], #i	RET	SBIT 6, [B]	RBIT 6, [B]	LD B, 1	IFBNE 0E	JSR 0E00-0EFF	JMP 0E00-0EFF	JP + 31	JP + 15
JP-0	JP-16	LD 0FF, #i	DRSZ 0FF	*	*	*	RETI	SBIT 7, [B]	RBIT 7, [B]	LD B, 0	IFBNE 0F	JSR 0F00-0FFF	JMP 0F00-0FFF	JP + 32	JP + 16

* is an unused opcode (see following table)

Md is a directly addressed memory location

i is the immediate data

where,

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

COP620C/COP621C/COP622C/COP640C/COP641C/COP642C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

Instruction Execution Time

Most instructions are single byte (with immediate addressing mode instruction taking two bytes).

Most single instructions take one cycle time (1 μ s at 20 MHz) to execute.

See the BYTES and CYCLES per INSTRUCTION table for details.

BYTES and CYCLES per INSTRUCTION

The following table shows the number of bytes and cycles for each instruction in the format of byte/cycle (a cycle is 1 μ s at 20 MHz).

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	[B]	Direct	Immed.
ADD	1/1	3/4	2/2
ADC	1/1	3/4	2/2
SUBC	1/1	3/4	2/2
AND	1/1	3/4	2/2
OR	1/1	3/4	2/2
XOR	1/1	3/4	2/2
IFEQ	1/1	3/4	2/2
IFGT	1/1	3/4	2/2
IFBNE	1/1		
DRSZ		1/3	
SBIT	1/1	3/4	
RBIT	1/1	3/4	
IFBIT	1/1	3/4	

Memory Transfer Instructions

	Register Indirect		Direct	Immed.	Register Indirect Auto Incr & Decr	
	[B]	[X]			[B+, B-]	[X+, X-]
XA,*	1/1	1/3	2/3		1/2	1/3
LD A,*	1/1	1/3	2/3	2/2	1/2	1/3
LD B,Imm				1/1		
LD B,Imm				2/3		
LD Mem,Imm	2/2		3/3		2/2	
LD Reg,Imm				2/3		

(If B < 16)
(If B > 15)

* -> Memory location addressed by B or X or directly.

Instructions Using A & C

Transfer of Control Instructions

CLRA	1/1	JMPL	3/4
INCA	1/1	JMP	2/3
DECA	1/1	JP	1/3
LAID	1/3	JSRL	3/5
DCORA	1/1	JSR	2/5
RRCA	1/1	JID	1/3
SWAPA	1/1	RET	1/5
SC	1/1	RETSK	1/5
RC	1/1	RETI	1/5
IFC	1/1	INTR	1/7
IFNC	1/1	NOP	1/1

The following table shows the instructions assigned to unused opcodes. This table is for information only. The operations performed are subject to change without notice. Do not use these opcodes.

Unused Opcode	Instruction	Unused Opcode	Instruction
60	NOP	A9	NOP
61	NOP	AF	LD A, [B]
62	NOP	B1	C → HC
63	NOP	B4	NOP
67	NOP	B5	NOP
8C	RET	B7	X A, [X]
99	NOP	B9	NOP
9F	LD [B], #i	BF	LD A, [X]
A7	X A, [B]		
A8	NOP		

Development Support

MOLE DEVELOPMENT SYSTEM

The MOLE (Microcomputer On Line Emulator) is a low cost development system and emulator for all microcontroller products. These include COP8™ and the HPCT™ family of products. The MOLE consists of a BRAIN Board, Personality Board and optional host software.

The purpose of the MOLE is to provide the user with a tool to emulate code for the target microcontroller and assist in both software and hardware debugging of the system.

It is a self contained computer with its own firmware which provides for all system operation, emulation control, communication, PROM programming and diagnostic operations.

It contains three serial ports to optionally connect to a terminal, a host system, a printer or a modem, or to connect to other MOLEs in a multi-MOLE environment.

MOLE can be used in either a stand alone mode or in conjunction with a selected host system using PC-DOS communicating via a RS-232 port.

Single Chip Emulator Device

The COP820C is fully supported by a form, fit and function emulator device, the COP8720C.

Option List T-49-19-08

The COP820C/COP840C mask programmable options are listed out below. The options are programmed at the same time as the ROM pattern to provide the user with hardware flexibility to use a variety of oscillator configuration.

OPTION 1: CKI INPUT

- = 1 Normal Mode Crystal (CKI/10) CKO for crystal configuration
- = 2 Normal Mode External (CKI/10) CKO available as G7 Input
- = 3 R/C (CKI/10) CKO available as G7 Input
- = 4 High Speed Crystal (CKI/20) CKO for crystal configuration
- = 5 High Speed External (CKI/20) CKO available as G7 Input

OPTION 2: COP820C/COP840C BONDING

- = 1 28 pin package
- = 2 24 pin package
- = 3 20 pin package

The following option information is to be sent to National along with the EPROM.

Option Data

Option 1 Value__is: CKI Input
 Option 2 Value__is: COP Bonding

How to Order

To order a complete development package, select the section for the microcontroller to be developed and order the parts listed.

Development Tools Selection Table

Microcontroller	Order Part Number	Description	Includes	Manual Number
COP820/ COP840	MOLE-BRAIN	Brain Board	Brain Board Users Manual	420408188-001
	MOLE-COP8-PB1	Personality Board	COP820/840 Personality Board Users Manual	420410806-001
	MOLE-COP8-IBM	Assembler Software for IBM	COP800 Software Users Manual and Software Disk PC-DOS Communications Software Users Manual	424410527-001 420040416-001
	420410703-001	Programmer's Manual		420410703-001

COP820C/COP821C/COP822C/COP840C/COP841C/COP842C/COP820C/COP821C/COP822C/COP840C/COP841C/COP842C

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