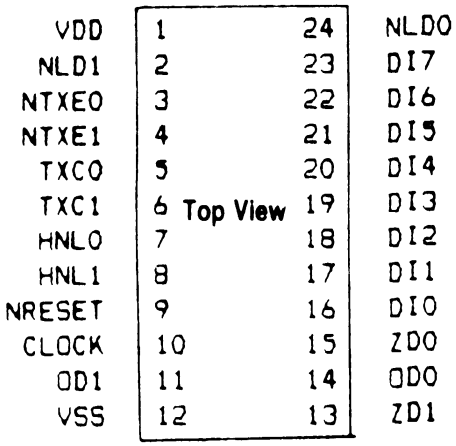
Micro Circuit Engineering

technology applied

TWO CHANNEL ARINC TRANSMITTER

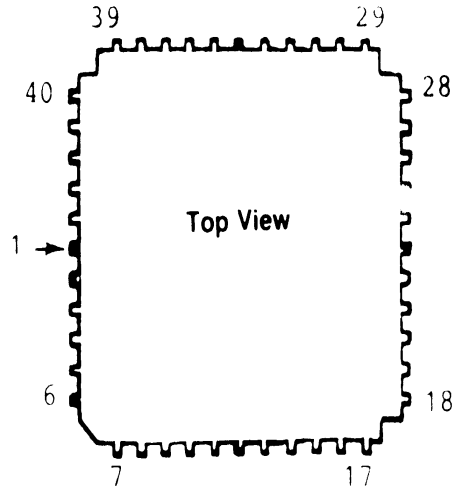
- 8 bit parallel interface
- TTL/CMOS compatible I/P
- Single 5V supply with low power consumption < 50mW
- Full MIL operating range
- Automatic parity generation
- HIGH/LOW speed programmable independently in each channel

PIN CONFIGURATION



NC NOT CONNECTED

24 PIN DIL PACKAGE



1	NC	16	NC	31	DI1
2	VDD	17	NRESET	32	NC
3	NC	18	CLOCK	33	DI2
4	NLD1	19	NC	34	NC
5	NC	20	OD1	35	DI3
6	NTXEO	21	NC	36	NC
7	NTXE1	22	VSS	37	DI4
8	NC	23	NC	38	NC
9	TXCO	24	ZD1	39	DI5
10	NC	25	NC	40	DI6
11	TXC1	26	ODO	41	NC
12	NC	27	NC	42	DI7
13	HNLO	28	ZDO	43	NC
14	NC	29	DIO	44	NLDO
15	HNL1	30	NC		

44 PIN J LEAD
SURFACE MOUNT PACKAGE.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	- 65ºC to +150ºC
Temperature (Ambient) under Bias	- 55ºC to +125ºC
Supply Voltage VDD	-0.3V to + 7V
DC Input Voltage	-0.3 to VDD +0.3V
Output Current (Single O/P)	10mA
Output Current (Total O/P)	20mA

ELECTRICAL CHARACTERISTICS over operating range

PARAMETER	DESCRIPTION	TEST CONDITIONS		MIN	TYP	MAX	UNITS
IOH	Output High Current	VOH=2.8V	VDD= 4.5V	1.0			mA
IOL	Output Low Current	VOL=0.4V		3.2			mA
VIH	Input High Voltage			2.4		VCC	Volts
VIL	Input Low Voltage			-0.3		0.8	Volts
IIL	Input Load Current	VSS				0.45	mA
IOZ	Output Leakage Current	0.4V<VO<VCC Output Disabled		-40		40	uA
CI	Input Capacitance	Test Frequency = 1.0 MHZ			2	2.6	pF
CI/O	I/O Capacitance				7	9	pF
ICC	Supply Current	VCC = MAX. All inputs HIGH, All outputs open.				1.5	mA

3. SWITCHING CHARACTERISTICS (For C_L = 50pF & RL = 3K ohms)

PARAMETER		Min	Max	Units
f_{CLK}	Clock Frequency	-	5	MHz
t_P	(Serial data bit period for HNL input high ((Serial data bit period for HNL input low (((f = f_{CLK}/MHz)	50/f 380/f		uS uS
t_{RES}	NRSET pulse width	200nS	-	
t_{RTC}	Propagation delay, NRESET falling edge to TXC high	-	200nS	
t_{RD}	Propagation delay, NRESET falling edge to data outputs low	-	200nS	
t_{WL}	NLD pulse width	200nS	-	
t_{GL}	Gap between NLD pulses	400nS	-	
t_{SU}	Data set up time	100nS	-	
t_H	Data hold time	100nS	-	
t_{LTC}	Propagation delay, NLD rising edge following last byte load to TXZ low	-	400nS	
t_R	Output rise time	-	50nS	
t_F	Output fall time	-	50nS	
t_{WTE}	NOT Transmit enable pulse width	100nS	-	
t_{TED}	Propagation delay NOT transmit enable falling edge or NOT Transmission complete falling edge to data output	tp	2tp	
t_{DTC}	Last data bit of message to TXC high	-	200nS	
t_M	Time of data pulse output (mark time)	$\frac{tp}{2} \pm 1\%$		

FUNCTIONAL DESCRIPTION

The device consists of two independent channels each of which functions as a parallel to serial data converter. The parallel data is loaded via an 8-bit input highway and the serial output is generated in the ARINC format, i.e. 31 bits of data plus one parity bit.

The input highway (DIO to D17) is common to both channels as are the reset (NRESET) CLOCK 9clock), positive supply (V_{DD}), and ground (VSS) pins. Each channel has 3 control inputs. Channel 0 has a 'load' input (NLDO), a 'transmit enable' input (NTXEO), and a 'high/low speed' (HNLO) control input. There are 3 outputs per channel. Channel 0 has a 'data out zeros' (ZDO) output, a 'data out ones' (ODO) output and a 'transmission complete' (TXCO) output.

Operations for Channel 0 and Channel 1 are identical in all respects.

The data to be transmitted by a particular channel is loaded as four 8-bit bytes via the input highway. The four bytes are stored on chip in the order in which they were loaded. Loading is performed by pulsing the (NLDO) input low. The data must then be changed to the value of the next byte and (NLDO) pulsed low again etc.

The four bytes are transmitted in the order in which they were loaded. The only exception is the most significant bit of the 4th byte. This bit is ignored and a parity bit is transmitted in its place. The parity bit corresponds to an odd parity check on the first 31 bits, i.e. if the number of ones in the first 31 bits is odd, the parity bit is equal to zero.

Data is only accepted if the TXCO output is high. Once byte 4 has been loaded, TXCO is driven low. Data must be valid on the input highway for t_{su} before and to t_H after the (NLDO) rising edge.

The clock (CLOCK) input of 5mhz $\pm$ 1%* is divided down on chip by 50 to give a serial data transmission rate for (HNLO) high or by 380 for (HNLO) low. These rates correspond to the ARINC fast and slow rates respectively. The timing of the two output data lines (ODO) and (ZDO) is shown in Fig.2. A data value of one is signified by a positive pulse output on (ODO) and a zero by a positive pulse on (ZDO). The bit period tp will be $50/f_{CLK}$ for (HNLO) high and $380/f_{CLK}$ for (HNLO) low.

* ARINC recommends that the transmission rate should not be precisely 100KHZ to avoid interference but any rate within $\pm$ 1% of these can be used.

The overall timing diagram for a complete data transfer is shown in Fig.3. When the last byte has been loaded (TXCO) goes low. This signal is combined with the output of an on chip latch which is set by the (NTXEO) signal to initiate the start of transmission. The latch is reset upon start of transmission. If the (NTXEO) signal is left permanently low the on chip latch is always set and transmission will be initiated by TXCO going low, i.e. as soon as the 4 bytes have been loaded. Hence there is an option between auto-start and controlled-start of transmission. At the end of the transmission TXCO goes high and the device is able to accept new data.

The devices can be completely reset by pulsing the (NRESET) line low. This causes both channels to be put into the data load phase of operation. The TXC lines are forced high and all data outputs are forced low. the timing is shown in Fig. 4.

INTERFACE DEFINITIONS

The device is implemented as a monolithic circuit using CMOS compatible with standard TLL circuitry.

A circuit with V_{OH} (min) = 2.7V and V_{OL} (max) = 0.4V will drive all inputs to the device and a standard TTL circuit with I_{IL} (max) = -1.6mA at V_I = 0.4V and I_{IH} (max) = 40 uA at V_I = 2.4V can be driven by all the outputs of the device.

An on-chip resistor of nominal value 25K ohms is connected between the input pin and V_{DD}. This is intended to pull up the input to a sufficiently high voltage to ensure switching when a standard TTL driver is driving the input.

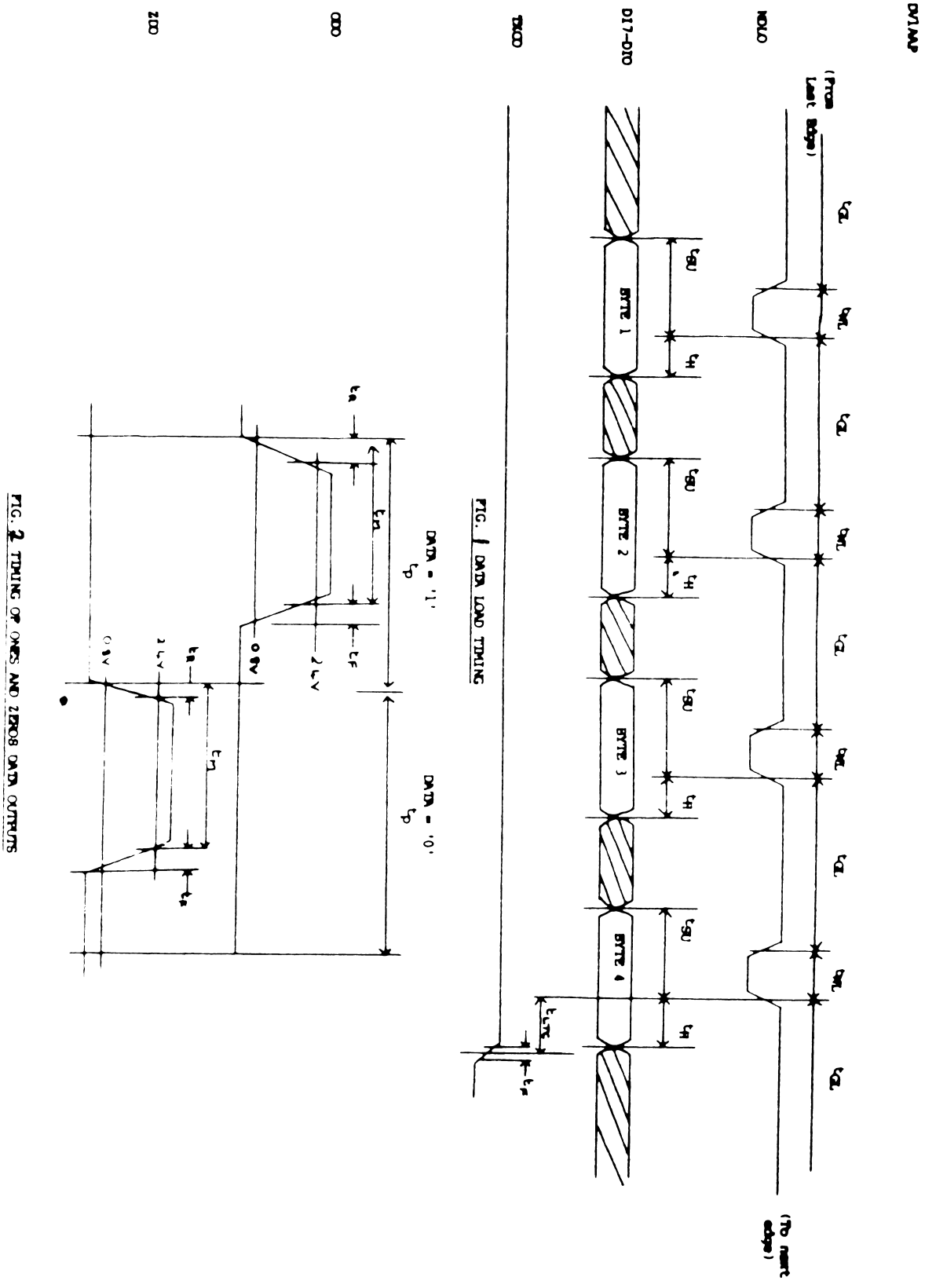


FIG. 2 TIMING OF ONES AND ZEROS DATA OUTPUTS

FIG. 1 DATA LOAD TIMING

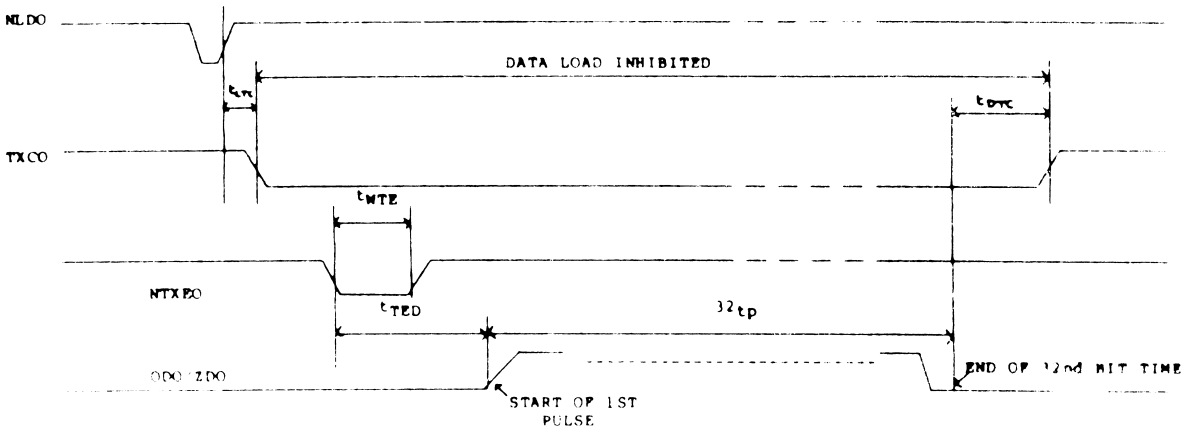
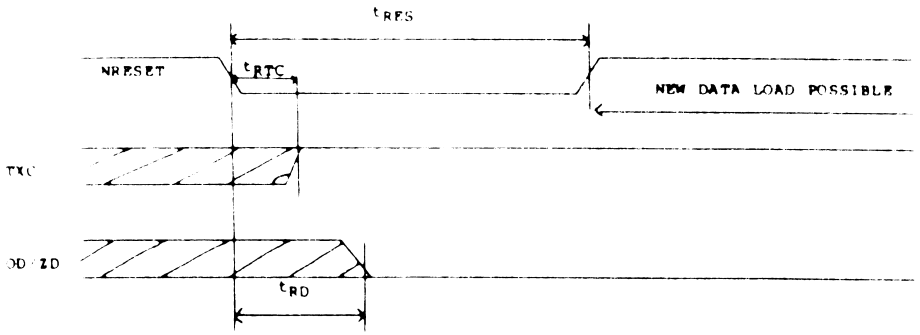


FIG. 3 OVERALL TIMING FOR DATA TRANSFER



DV1AAQ

FIG. 4 RESET TIMING

PHYSICAL DIMENSIONS

24-Pin Side Brazed