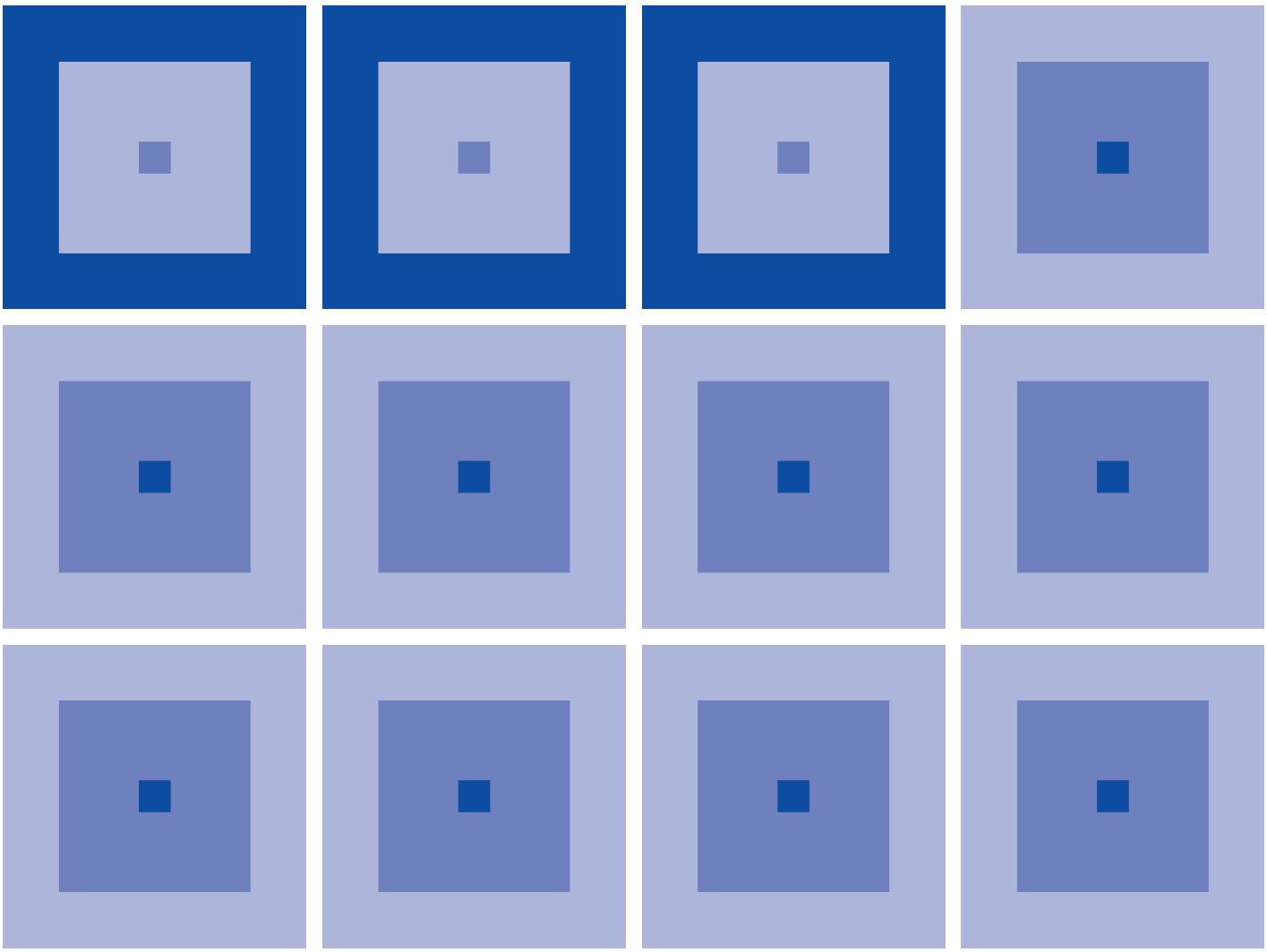
EPSON

IEEE1394 Controller

S1R72803F00A

Technical Manual



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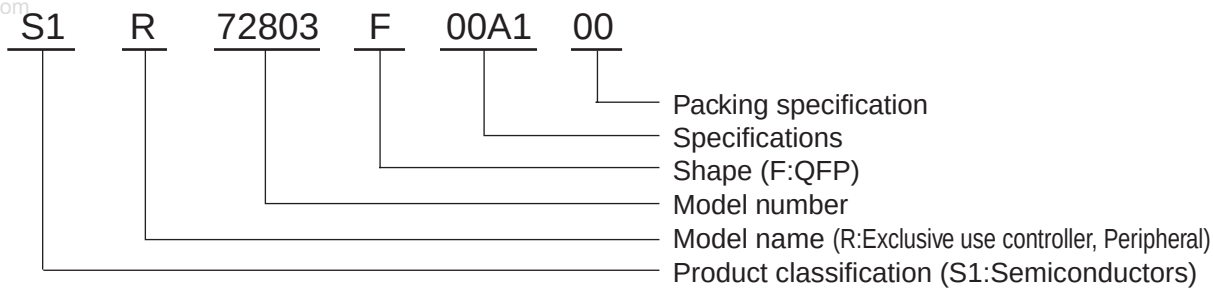
The information of the product number change

Starting April 1, 2001 the product number has been changed as listed below. Please use the new product number when you place an order. For further information, please contact Epson sales representative.

Configuration of product number

●DEVICES



Contents

1. DESCRIPTION

The S1R72801F00A is a LINK/Transaction controller based on the IEEE Std. 1394-1955, P1394a Draft 2.0. It integrates a built-in CPU and Flash ROM, and also integrates a part of transaction functions into hardware. If you set a PageTable address and its size, it can automatically fetch subsequent PageTables and transmit data. It can offer a 1394 interface optimum to computer peripherals in combination with the Cable PHY Transceiver Arbiter based on the above standard.
The IDE interface complies with Ultra DMA mode 4 (ATA 66), offering a high transfer rate.

2. FEATURES

- LINK/Transaction Controller
  LINK Layer
  Ready for all two-way data transfer in Asynchronous and Isochronous modes.
  The built-in SRAM realized stable two-way data transfer up to max. payload of 100Mbps, 200Mbps, and 400Mbps.
  Can automatically detect the Isochronous Resource Manager by hardware.

  Transaction Layer
  Integrates a part of transaction functions into hardware to prevent deterioration of actual data transmission rate due to the overhead of firmware (assure a special area).
  A header area is distinguished from a data area to simplify communications with a higher rank layer. Furthermore, it segments a data area to a stream area and ORB area.
  Adopts a ring buffer to the receive header area, receive data area (receive stream area, receive ORB area) and transmit data area (transmit stream area). Can arbitrarily set the size of each area.
  Automatically controls the Busy when hardware receives data.

- SBP-2 Support
  Can set an PageTable address and its size for the SBP-2 to automatically perform subsequent Page Table fetches and data transfers.

- PHY/LINK Interface
  Ready for the P1394a.
  Ready for the data transfer rate of 100/200/400Mbps.
  Ready for isolation (bus holder integrated)

- IDE Interface
  Ready for the PIO mode 0/1/2/3/4, multi-word DMA mode 0/1/2, Ultra-DMA mode 0/1/2/3/4.
  Voltage level is 3.3V (TTL) level.
  5V level input can be possible (5V Tolerant)

● Built-in CPU

Integration of a CPU eliminated the necessity of an external CPU to control this IC.

CPU core: 32-bit RISC CPU S1C33000
Harvard architecture (Concurrency of a fetch and load/store)

High speed/high performance:
Ready for operation with 25MHz

Command set: 16-bit fixed length, 105 types of basic commands

Execution cycle:
Execution at one cycle/command regarding a main command

AND/OR (MAC) operation:
16 bits × 16 bits + 64 bits, 2 clocks/MAC

CPU Register: 16 32-bit general registers and 5 32-bit special registers

Memory space: Linear space where 256-Mbyte (28-bit) code, data, and I/O can be mapped.

External bus interface:
Directly connects the external memory of the memory area.
Programmable wait cycle (7 cycles, Max.)
Enables handshake through the XWAIT terminal.

Interrupt: Ready for reset, NMI, max. 128 external interrupts, 4 software interrupts, and 2 exceptions

Reset, boot: Cold reset, hot reset

Built-in RAM: 8Kbytes for work

● Flash ROM

Integration of a Flash ROM eliminated the necessity of a ROM to externally store programs.

- Memory structure:
  Memory size 512K (32K × 16) bits
- Sector size: 512 words/sector
- Unit of erase: Per chip or sector
- Unit of write: Writing with words
- Erase/write time:
  Chip erase time 100ms (Standard)
  Sector erase time 20ms (Standard)
  Write time: 15µs (Standard)
- Access time: 90nsec. (Max.)
- Reliability: No. of erase/write 1,000 times
  Data retention: 10 years

● Others

A Boot ROM (4MBbytes, Max.) is connectable to outside of this IC.
Supply voltage, 5.0V ± 10% and 3.3V ± 0.3V
184PinQFP (0.4mm pitch)
Not radiation resistant.

The CPU core built into this IC is an original 32-bit RISC CPU from SEIKO EPSON. Regarding the CPU core, refer to the S1C33208/204/202 Technical Manual and S1C33 Family ASIC Macro Manual. The built-in RAM is 8Kbytes.

Note: In the built-in CPU core, a DMA controller and A/D converter are not integrated; this part is different from the description on the DMA controller and A/D converter given in Technical Manual (and Macro Manual). A low speed oscillation circuit (OSC1) is not available.

3. INTERNAL BLOCK DESCRIPTION

3.1 BLOCK DIAGRAM

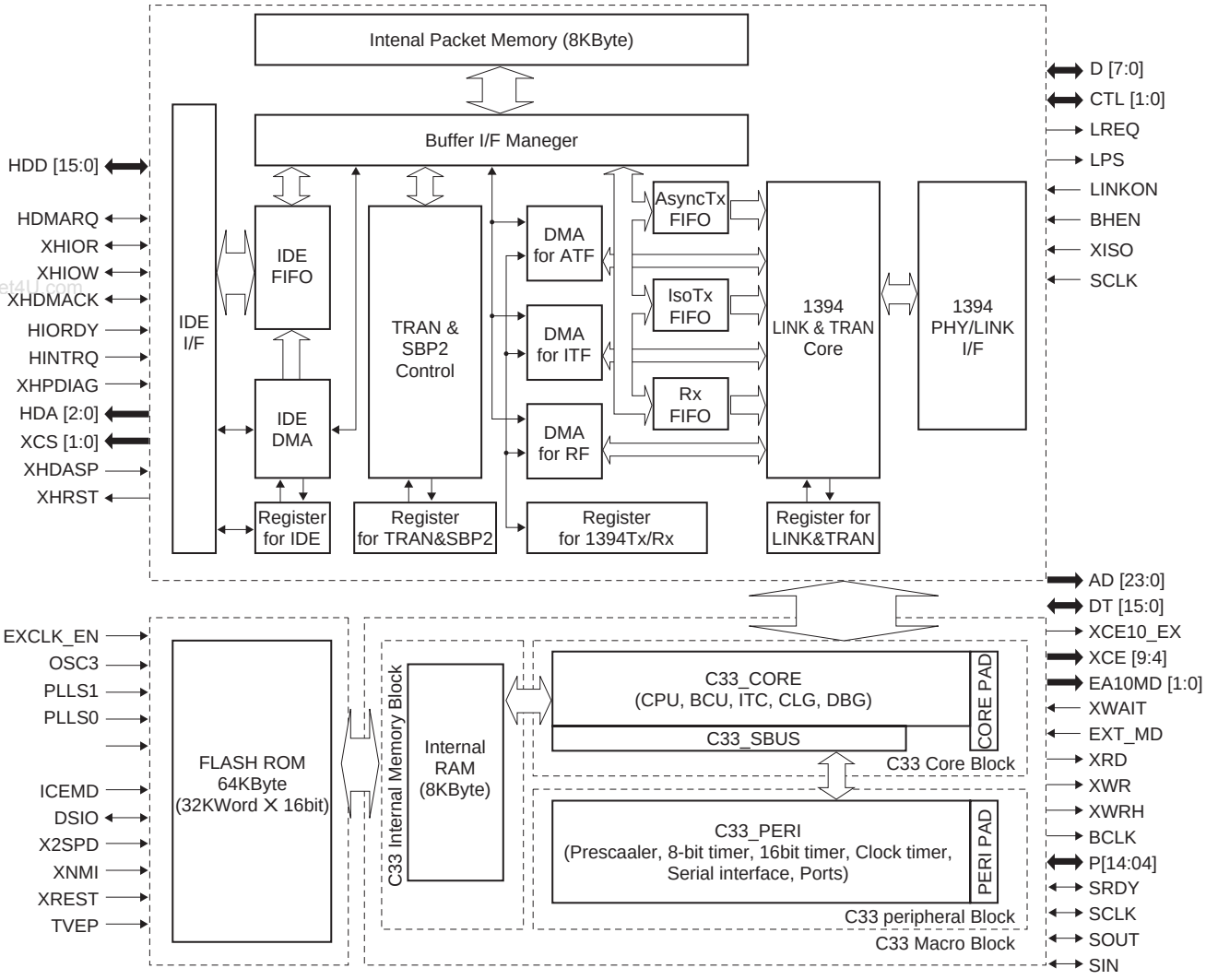


Fig. 3.1 Block diagram

3.2 BLOCK DIAGRAM DESCRIPTION

● C33 CORE Block
The C33 CORE Block consists of the function block-C33_CORE- that includes the CPU, BCU (bus control unit), ITC (interrupt controller), CLG (clock generator), and DBG (debug unit), the external interface I/O pad block-PAD_CORE, PAD_CORE_OPTION-, and the block to interface with the peripheral circuits on the chip -SBUS-.

● C33_PERI Block (C33 peripheral circuit block)
The C33_PERI Block consists of the PSC (prescaler), 6-channel T8 (8-bit programmable timer), WDT (watch dog timer), 6-channel T16 with an event counter (16-bit programmable timer), 4-channel SIO (serial interface), input and I/O ports, and CTM (clock timer).

● Internal RAM Block
SRAM for the built-in memory area (Area 0).

● Internal Flash Block
Flash for the built-in memory area (Area 10).

4. INTERNAL CONNECTION DIAGRAM

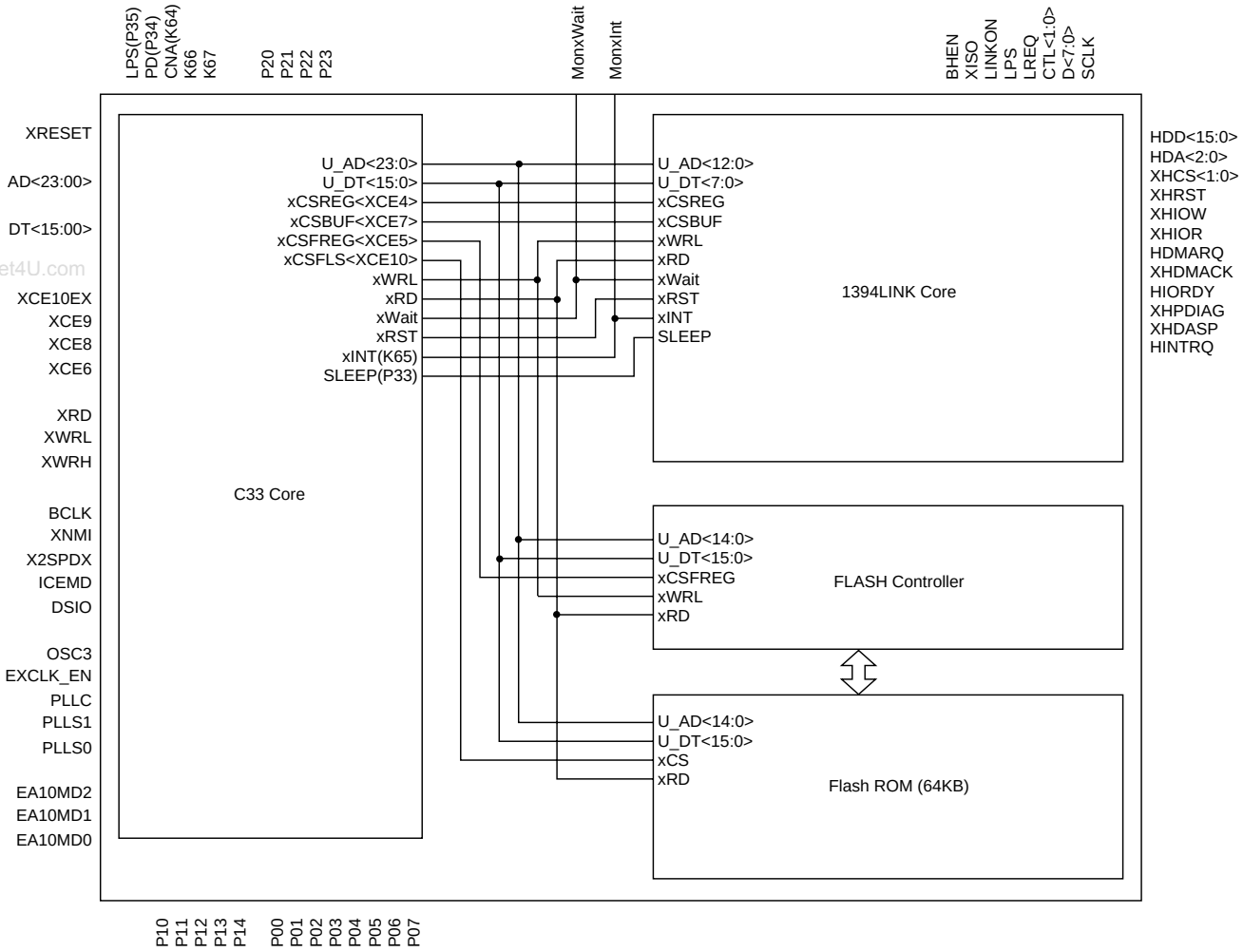
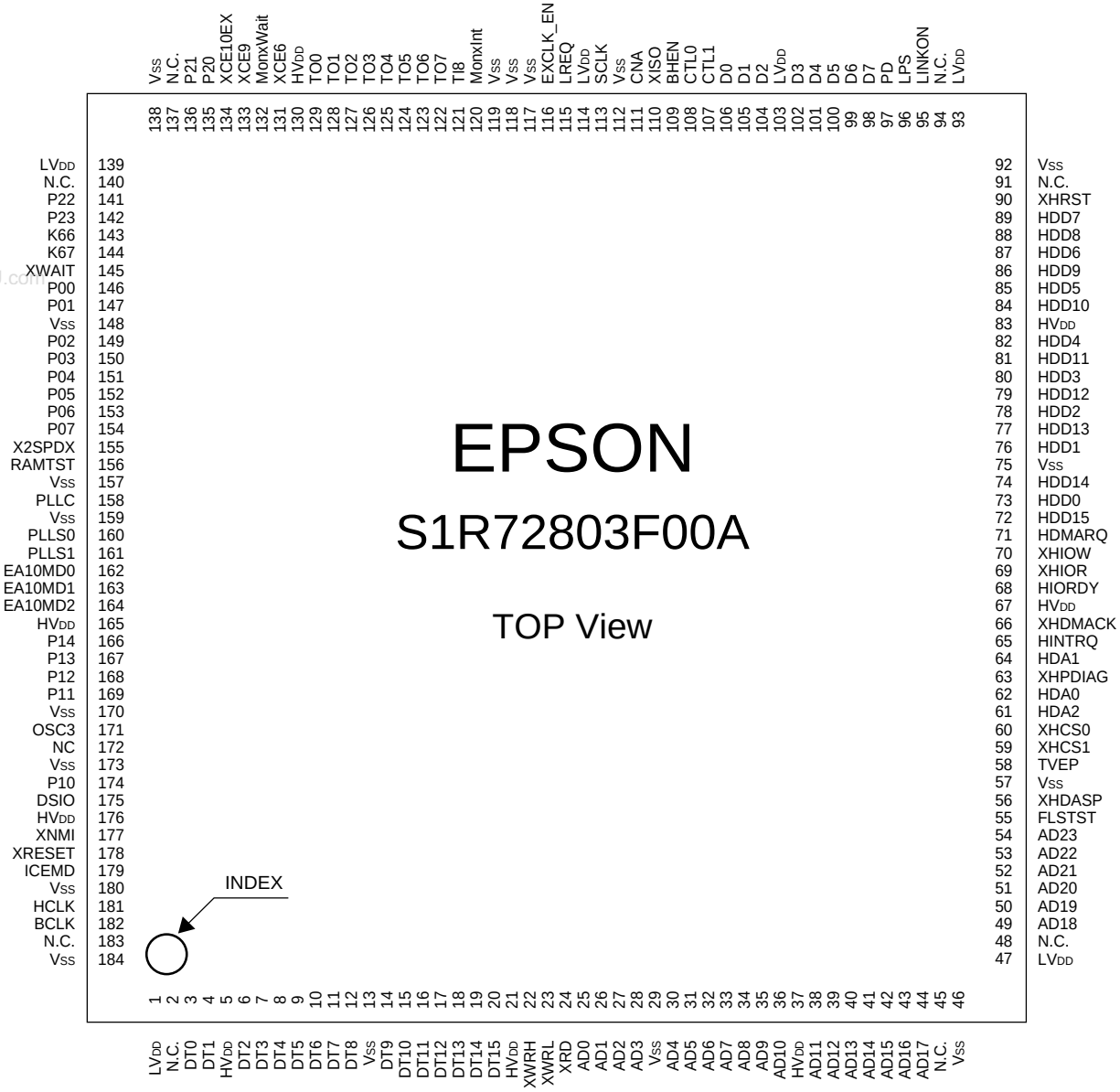


Fig. 4.1 Internal connection diagram

5. PIN ASSIGNMENT DIAGRAM



6. PIN DESCRIPTION

Control signals with an "X" as the first character of a pin name are low active. (Excluding X2SPD)

Pin Name	PIN	I/O	Reset	Pin Function	Remarks
1394PHY interface (LV_{DD})					
D7	98	B	Hi-Z	(MSB)	
D6	99	B	Hi-Z		
D5	100	B	Hi-Z		
D4	101	B	Hi-Z	Data Bus with PHY	Drive Ability 6mA
D3	102	B	Hi-Z		
D2	104	B	Hi-Z		Schmitt Input (Bus Holder)
D1	105	B	Hi-Z		
D0	106	B	Hi-Z	(LSB)	
CTL1	107	B	Hi-Z	Control Signal with PHY	Drive Ability 6mA
CTL0	108	B	Hi-Z		Schmitt Input (Bus Holder)
LREQ	115	O	Lo	LINK Request Signal to PHY	Drive Ability 6mA
LPS	96	O	Hi	LINK Power Status Signal to PHY	Drive Ability 6mA
LINKON	95	I	–	LINK ON Signal from PHY	Schmitt Input (Bus Holder)
XISO	110	I	–	Setting should be made according to the construction of isolation buffer between PAY and LINK Set to H level in case of DC connection and Single capacitor AC connection. And Annex-J Isolation connection cannot be used.	CMOS Input
BHEN	109	I	–	Bus Holder Enable Signal H: Single capacitor AC connection L: DC connection	
CNA	111	I	–	Cabele Not Active	Schmitt Input (Bus Holder)
PD	97	O		Power Down Enable	Drive Ability 6mA
SCLK	113	I	–	Clock Signal from PHY (49.576MHz)	Schmitt Input (Bus Holder)
IDE Interface (LV_{DD})					
HDD15	72	B	Hi-Z	(MSB)	
HDD14	74	B	Hi-Z		
HDD13	77	B	Hi-Z		
HDD12	79	B	Hi-Z		
HDD11	81	B	Hi-Z		
HDD10	84	B	Hi-Z		
HDD9	86	B	Hi-Z		5V Tolerant
HDD8	88	B	Hi-Z	IDE Data Bus	Drive Ability 2mA
HDD7	89	B	Hi-Z		Pull Down HDD7 at 10kΩ
HDD6	87	B	Hi-Z		
HDD5	85	B	Hi-Z		
HDD4	82	B	Hi-Z		
HDD3	80	B	Hi-Z		
HDD2	78	B	Hi-Z		
HDD1	76	B	Hi-Z		
HDD0	73	B	Hi-Z	(LSB)	
HDMARQ	71	B	Hi-Z	IDE DMA Request Signal	5V Tolerant, Drive Ability 2mA, Schmitt Input
XHIOW	70	B	Hi-Z	IDE Write Signal	5V Tolerant, Drive Ability 2mA, Schmitt Input
XHIOR	69	B	Hi-Z	IDE Read Signal	5V Tolerant, Drive Ability 2mA, Schmitt Input
HIORDY	68	I	–	IDE IORDY Signal	5V Tolerant, Drive Ability 2mA, Schmitt Input
XHDMACK	66	B	Hi-Z	IDE DMA Acknowledge Signal	5V Tolerant, Drive Ability 2mA, Schmitt Input
HINTRQ	65	I	–	IDE Interrupt Signal	5V Tolerant, Schmitt Input
XHPDIAG	63	I	–	IDE PDIAG Signal	5V Tolerant, Schmitt Input

Pin Name	PIN	I/O	Reset	Pin Function	Remarks
IDE Interface (LVDD)					
HDA2	61	Otr	Hi-Z	(MSB)	Drive Ability 2mA, Tristate
HDA1	64	Otr	Hi-Z	IDE Address Signal	Drive Ability 2mA, Tristate
HDA0	62	Otr	Hi-Z	(LSB)	Drive Ability 2mA, Tristate
XHCS1	59	Otr	Hi-Z	IDE Chip Select Signal	Drive Ability 2mA, Tristate
XHCS0	60	Otr	Hi-Z	IDE Chip Select Signal	Drive Ability 2mA, Tristate
XHDASP	56	I	–	IDE DASP Signal	5V Tolerant, Schmitt Input
XHRST	90	Otr	Hi-Z	IDE Reset Signal	Drive Ability 2mA, Tristate
C33 External Interface (HVDD)					
AD23	54	O		(MSB)	
AD22	53	O			
AD21	52	O			
AD20	51	O			
AD19	50	O			
AD18	49	O			
AD17	44	O			
AD16	43	O			
AD15	42	O		CPU Address Bus	
AD14	41	O			
AD13	40	O			
AD12	39	O			
AD11	38	O			
AD10	36	O			
AD9	35	O			
AD8	34	O			
AD7	33	O			
AD6	32	O			
AD5	31	O			
AD4	30	O			
AD3	28	O			
AD2	27	O			
AD1	26	O			
AD0	25	O		(LSB)	
DT15	20	B	Hi-Z	(MSB)	
DT14	19	B	Hi-Z		
DT13	18	B	Hi-Z		
DT12	17	B	Hi-Z		
DT11	16	B	Hi-Z		
DT10	15	B	Hi-Z		
DT9	14	B	Hi-Z		
DT8	12	B	Hi-Z		
DT7	11	B	Hi-Z	CPU Data Buss	Pull Up Resistor Intgrated
DT6	10	B	Hi-Z		
DT5	9	B	Hi-Z		
DT4	8	B	Hi-Z		
DT3	7	B	Hi-Z		
DT2	6	B	Hi-Z		
DT1	4	B	Hi-Z		
DT0	3	B	Hi-Z	(LSB)	

Pin Name	PIN	I/O	Reset	Pin Function	Remarks
C33 External Interface (HVDD)					
P07	154	B		General I/O Port 07	Pull Up Resistor Integrated
P06	153	B		General I/O Port 06	Pull Up Resistor Integrated
P05	152	B		General I/O Port 05	Pull Up Resistor Integrated
P04	151	B		General I/O Port 04	Pull Up Resistor Integrated
SRDY(P03)	150	B		Serial I/F Ready Signal Input Pin-cum-General I/O Port 03	Pull Up Resistor Integrated
SCLK(P02)	149	B		Serial I/F Clock Input Pin-cum-General I/O Port 02	Pull Up Resistor Integrated
SOUT(P01)	147	B		Serial I/F Data Output Pin-cum-General I/O Port 01	Pull Up Resistor Integrated
SIN(P00)	146	B		Serial I/F Data Input Pin-cum-General I/O Port 00	Pull Up Resistor Integrated
K67	144	I		Generall Inut Port 67	Pull Up Resistor Integrated
K66	143	I		Generall Inut Port 66	Pull Up Resistor Integrated
P23	142	B		Generall I/O Port 23	Pull Up Resistor Integrated
P22	141	B		Generall I/O Port 22	Pull Up Resistor Integrated
P21	136	B		Generall I/O Port 21	Pull Up Resistor Integrated
P20	135	B		Generall I/O Port 20	Pull Up Resistor Integrated
XCE10_EX	134	O	Hi	External Memory Area 10 Chip Enable	
XCE9	133	O	Hi	Area 9 Chip Enable	
XCE6	131	O	Hi	Area 6 Chip Enable	
EA10M2	164	I		Area 10 Boot Mode Select 2	
EA10M1	163	I		Area 10 Boot Mode Select 1	Pull Up Resistor Integrated
EA10M0	162	I		Area 10 Boot Mode Select 0	Pull Up Resistor Integrated
XWAIT	145	I		Wait Cycle Input	
XRD	24	O	Hi	Read Signal	
XWRH	22	O	Hi	Higher Order Byte Write Signal	
XWRL	23	O	Hi	Lower Order Byte Write Signal	
BCLK	182	O		Bus Clock Signal	
C33 External Interface (LVDD)					
P14	166	B		General I/O Port 14 (For ICD)	
P13	167	B		General I/O Port 13 (For ICD)	
P12	168	B		General I/O Port 12 (For ICD)	
P11	169	B		General I/O Port 11 (For ICD)	
P10	174	B		General I/O Port 10 (For ICD)	
DSIO	175	B		Serial I/O Pin for Debug: Use for communication with ICD33.	Pull Up Resister Integrated
Clock Generator Pin					
OSC3	171	I		MCU Clock Input Crystal Oscillator	LVDD Input
PLLS1	161	I		PLL Set Pin 1	HVDD Input
PLLS0	160	I		PLL Set Pin 0	HVDD Input
PLLC	158	–		Capacitor Connection Pin for PLL	

Pin Name	PIN	I/O	Reset	Pin Function	Remarks
Other Pins					
ICEMD	179	I		Hi-Impedance Control: Set Hi-Z for all outputs.	Pull Down Resistor Integrated
X2PSDX	155	I		Double-speed mode setting pin HIGH : BCLK = CPU Clock LOW : BCLK = Half CPU Clock	HVDD Input
XNMI	177	I		NMIInput Pin	HVDD Input, Pull Up Resistor Integrated
XRESET	178	I		Initial Reset	HVDD Input, Pull Up Resistor Integrated
HCLK	181	O		Half SCLK Frequency Division Output	LVDD Output
EXCLK_EN	116	I		MCU clock switch pin HIGH:Internal CLK LOW:OSC3 Input	LVDD Input
TVEP	58	–		Flash Test Pin	Connect to HVDDwhen it is mounted.
Test Pin					
TI8	121	I			Schmitt Input (Bus Holder)
TO7	122	O	–	(MSB)	
TO6	123	O	–		
TO5	124	O	–		
TO4	125	O	–	Test Output Pin	Drive Ability 1mA
TO3	126	O	–		
TO2	127	O	–		
TO1	128	O	–		
TO0	129	O	–	(LSB)	
FLSTST	55	I	–	Built-in Flash Test Pin	Pull Down Resistor Integrated
RAMTST	156	I	–	Built-in SRAM Test Pin	Pull Down Resistor Integrated
MonxWait	132	O	–	Internal Logic xWait Monitor Pin	
MonxInt	120	O	–	Internal Logic xINT Monitor Pin	
Power Pin					
HVDD	–	P		HIGH Power (5V) 5,21,37,67,83,130,165,176 (8 Pins)	
LVDD	–	P		LOW Power (3.3V) 1,47,93,103,114,139 (6 Pins)	
VSS	–	P		GND 13,29,46,57,75,92,112,117,118,119,138, 148,157,159,170,173,180,184 (18 Pins)	
N.C. Pin					
N.C.	–	–		2,45,48,91,94,137,140,172,183 (9 Pins)	

Table 6.1 Settings of EA10M2, EA10M1, and EA10M0 (Area 10 Boot Mode)

P_EA10M2	P_EA10M1	P_EA10M0	Function
1	1	1	Built-in Flash Boot Mode
0	1	1	External ROM Mode

Note) Other settings are not available on this IC.

7. FUNCTIONAL DESCRIPTION

7.1 MEMORY MAP

7.1.1 All Memory Space

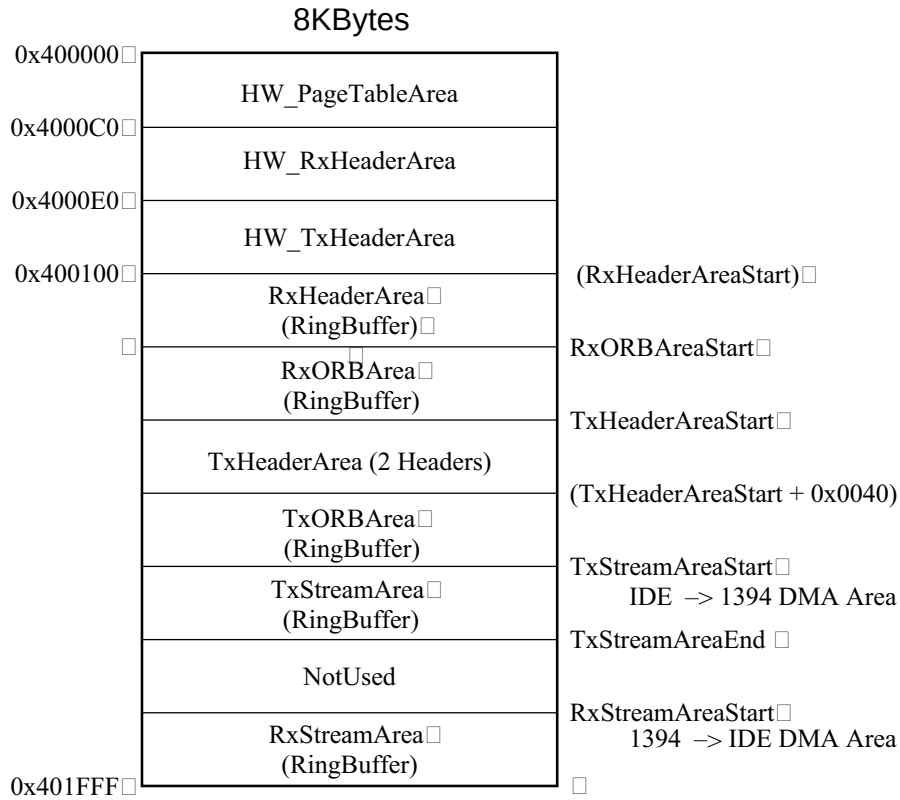
<table>
<tr><th>Area</th><th>Address</th><th colspan="2"></th></tr>
<tr><td rowspan="2">Area 0</td><td rowspan="2">0x000000
0x002000</td><td colspan="2">CPU-integrated RAM (8KB)</td></tr>
<tr><td colspan="2">(Mirror of CPU-integrated RAM)</td></tr>
<tr><td rowspan="3">Area 1</td><td rowspan="3">0x030000
0x040000
0x050000</td><td colspan="2">(Mirror of CPU-integrated Peripheral Circuit Control Register)</td></tr>
<tr><td colspan="2">CPU-integrated Peripheral Circuit Control Register</td></tr>
<tr><td colspan="2">(Mirror of CPU-integrated Peripheral Circuit Control Register)</td></tr>
<tr><td>Area 2</td><td>0x060000</td><td colspan="2">Reserved</td></tr>
<tr><td>Area 3</td><td>0x080000</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="2">Area 4</td><td rowspan="2">0x100000

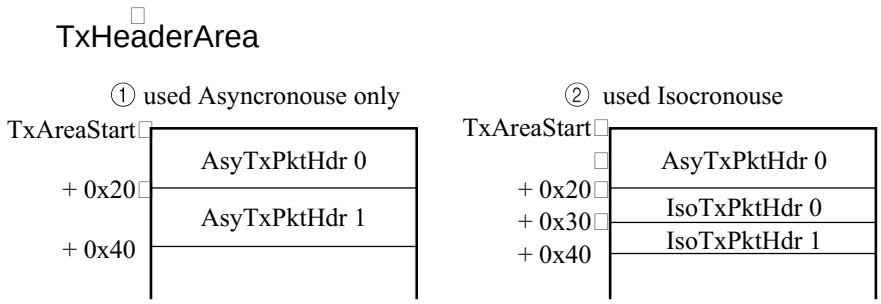
0x100080</td><td colspan="2">IEEE1394LINK/Transaction Controller
x CSREG Area (Control Register)</td></tr>
<tr><td colspan="2">Reserved</td></tr>
<tr><td rowspan="2">Area 5</td><td rowspan="2">0x200000
0x200008</td><td colspan="2">Flash ROM Control Register</td></tr>
<tr><td colspan="2">Reserved</td></tr>
<tr><td>Area 6</td><td>0x300000</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="2">Area 7</td><td rowspan="2">0x400000

0x402000</td><td colspan="2">IEEE1394LINK/Transaction Controller
xCSBUF Area (SRAM: 8KB)</td></tr>
<tr><td colspan="2">Reserved</td></tr>
<tr><td>Area 8</td><td>0x600000</td><td colspan="2">Reserved</td></tr>
<tr><td>Area 9</td><td>0x800000</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="2">Area 10</td><td rowspan="2">0xC00000
0xC10000

0xFFFFFF</td><td>Internal Flash ROM (64KB)</td><td rowspan="2">External ROM
(4MB)</td></tr>
<tr><td>Reserved</td></tr>
</table>

7.1.2 IEEE1394LINK/Transaction Controller xCSBUF Area (SRAM)



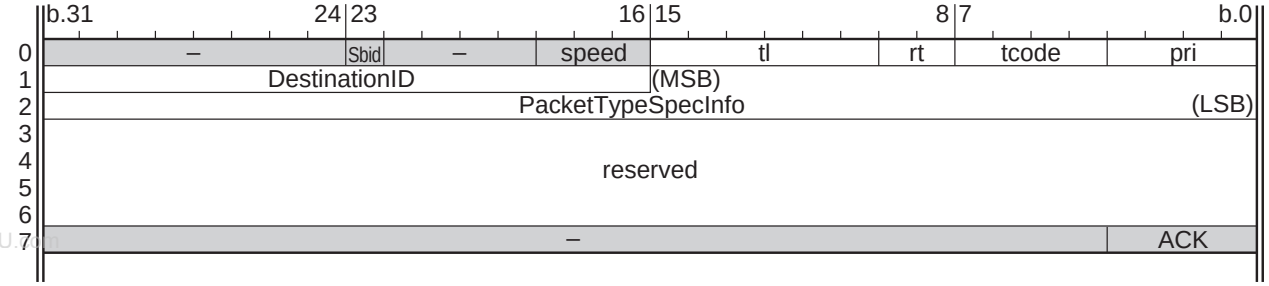


- All RAM areas are accessible from the CPU by direct addressing.
- Hardware DMA is possible to the IDE I/F for the RxStreamArea and TXStreamArea.
- HW_PageTableArea (the equivalent of 24 pages) and HW_RxHeaderArea and HW_TXHeaderArea (the equivalent of 1 header, respectively) are assured. The RxORB and TxORB areas are usable by firmware alone.
- The RxHeaderArea, RxORBArea, TxORB, TXStreamArea and RxStreamArea are RingBuffers. Even at the time of execution of data transmission/ reception according to 1394 or IDE DMA, data among the areas are guaranteed by hardware . (The size of each RingBuffer is variable by settings on the TxStreamAreaStart, TxStreamAreaEnd, and RxStreamAreaStart.)
- The TxStreamArea and RxStreamArea is usable as one StreamArea by overlaying them.
- The Post**Ptr and Used**Ptr of the RxHeaderArea, RxORBArea, TxStreamArea, and RxStreamArea monitor the used condition in each Area. (In the case of the Rx of 1394, the free space of the above two is monitored and the busy_A, B, X is controlled by hardware.)
- By controlling the above functions from the TRAN & SBP2 Control Block, a PageTable fetch and data transfer according to SBP-2 are executable by hardware.

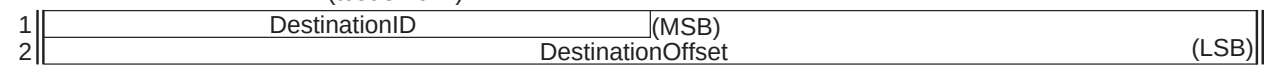
7.2 IEEE1394 PACKET FORMAT

7.2.1 Transmit Packet Format

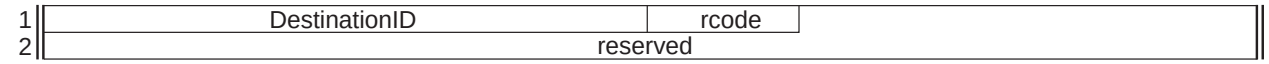
(1) TxAsyncronousePacket <3> QuadReadReq, WriteResp



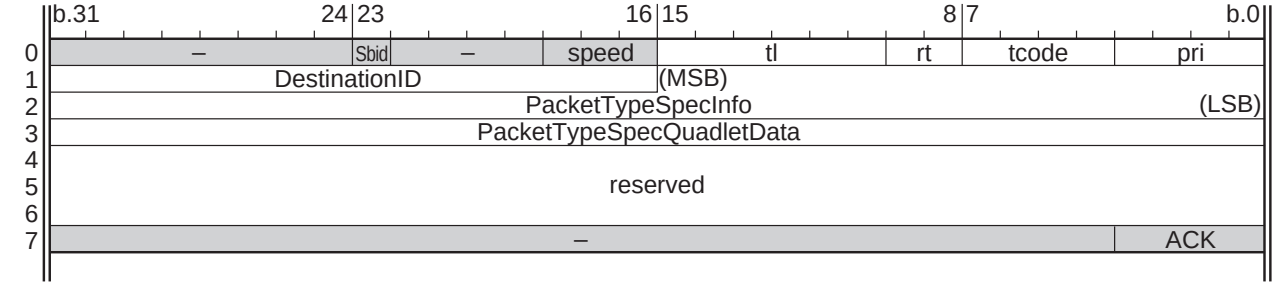
① QuadReadReq (tcode : 0x4)



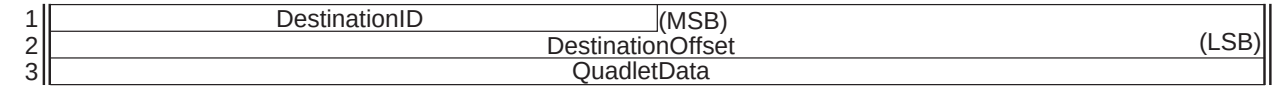
② WriteResp (tcode : 0x2)



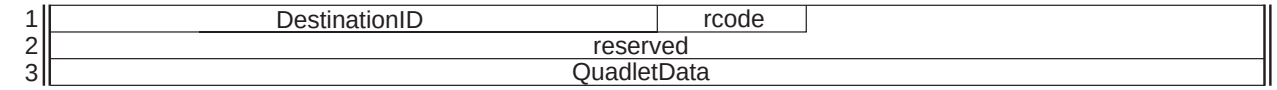
(2) TxAsyncronousePacket <4> QuadWriteReq, QuadReadResp, BlockReadReq



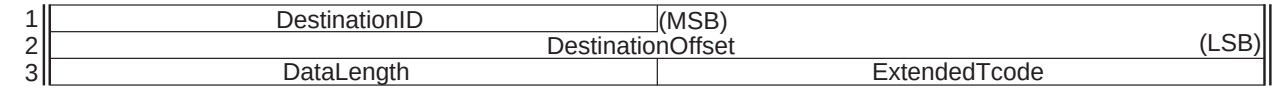
① QuadWriteReq (tcode : 0x0)



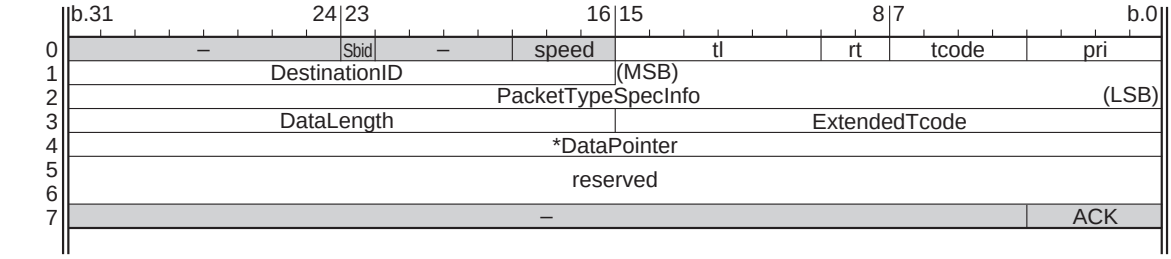
② QuadReadResp (tcode : 0x6)



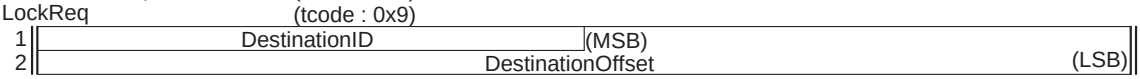
③ BlockReadReq (tcode : 0x5)



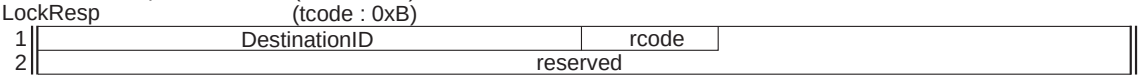
(3) TxAsyncronousePacket <5> BlockWriteReq, BlockReadResp, LockReq, LockResp



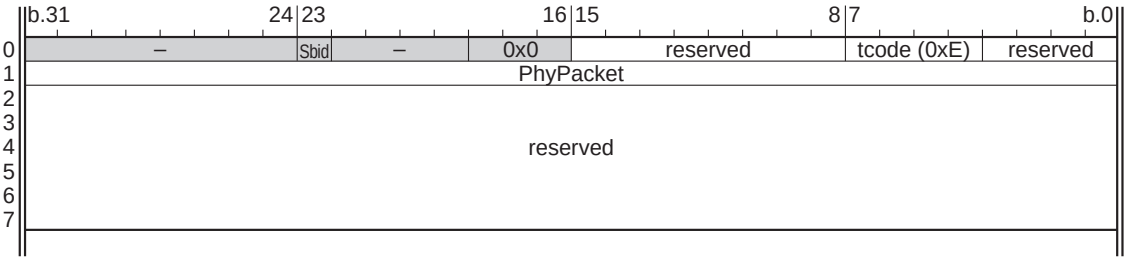
① BlockWriteReq (tcode : 0x1)
LockReq (tcode : 0x9)



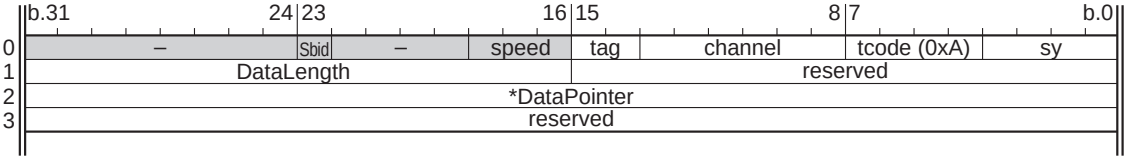
② BlockReadResp (tcode : 0x7)
LockResp (tcode : 0xB)



(4) TxAsyncronousePhyPacket (tcode : 0xE)



(5) TxIsocoronousePacket (tcode : 0xA)



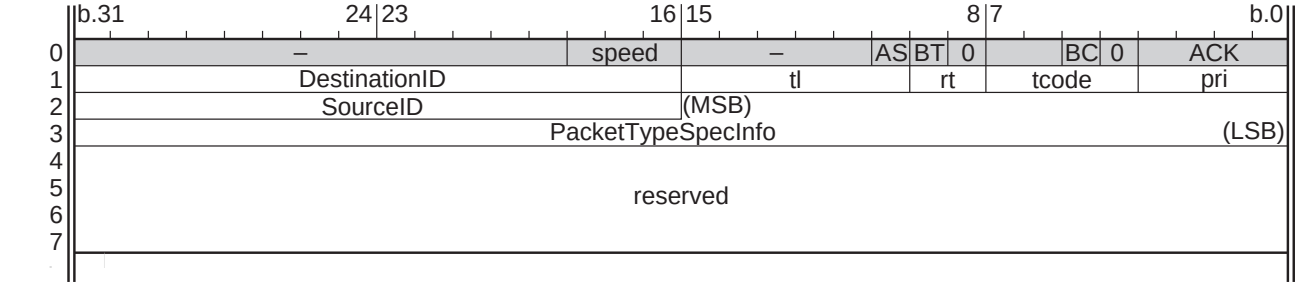
Transmit Packet Common Format

Name	Bit count	Description
speed	3	Speed Code 3'b000 S100 3'b001 S200 3'b010 S400 All Other Value Reserved
Sbid	1	Souce Bus ID 0:3FFh, 1:Source ID

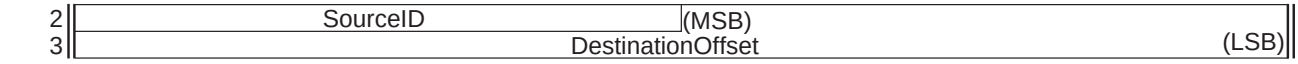
Name	Bit count	Description
ACK	4	Received AckCode 4'h1 ask_complete 4'h2 ask_pending 4'h4 ask_busy_X 4'h5 ask_busy_A 4'h6 ask_busy_B 4'hB ask_tardy 4'hC ask_confilict_error 4'hD ask_data_error 4'hE ask_type_error 4'hF ask_address_error All Other Value Reserved

7.2.2 Receive Packet Format

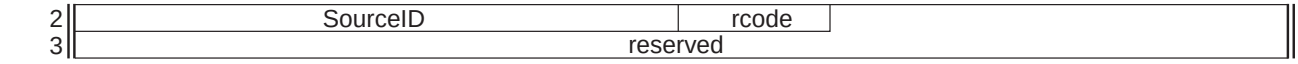
(1) RxAsyncronousePacket <4> QuadReadReq, WriteResp



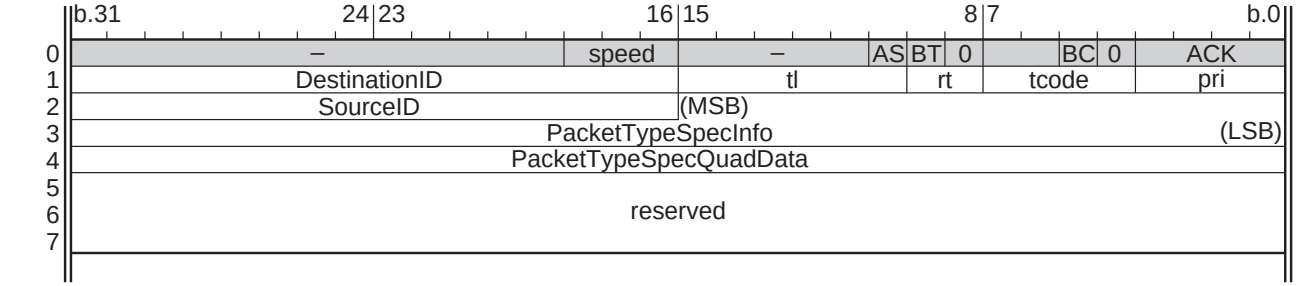
① QuadReadReq (tcode : 0x4)



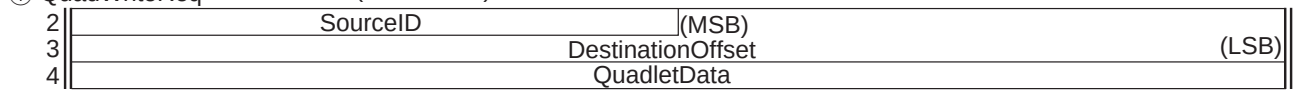
② WriteResp (tcode : 0x2)



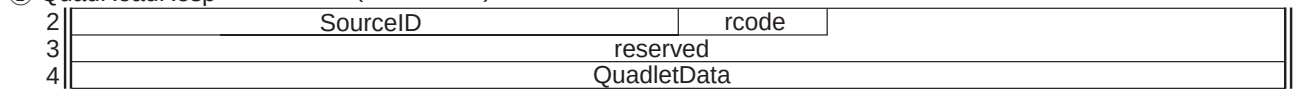
(2) RxAsyncronousePacket <5> QuadWriteReq, QuadReadResp, BlockReadReq



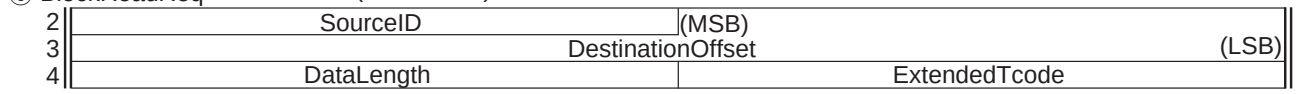
① QuadWriteReq (tcode : 0x0)



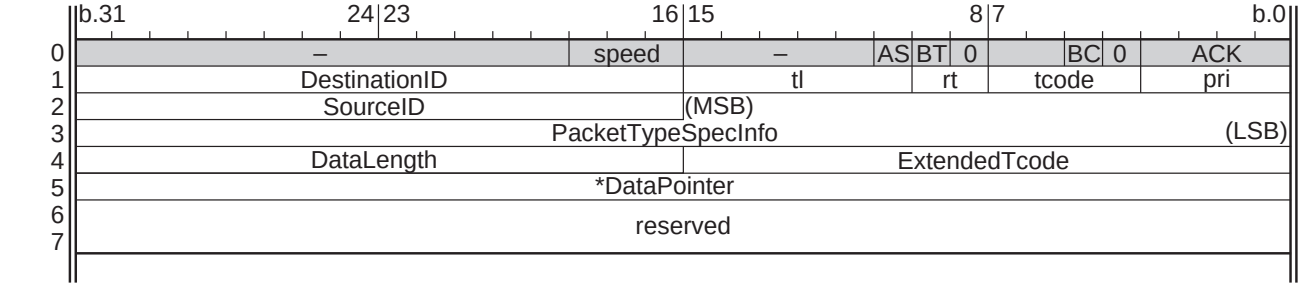
② QuadReadResp (tcode : 0x6)



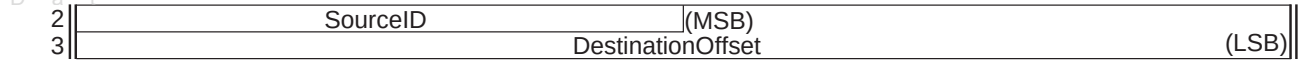
③ BlockReadReq (tcode : 0x5)



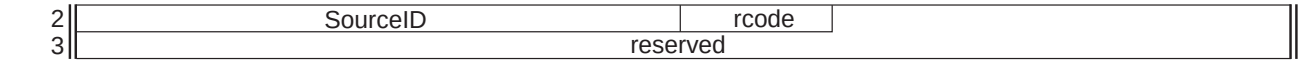
(3) RxAsyncronousePacket <6> BlockWriteReq, BlockReadResp, LockReq, LockResp



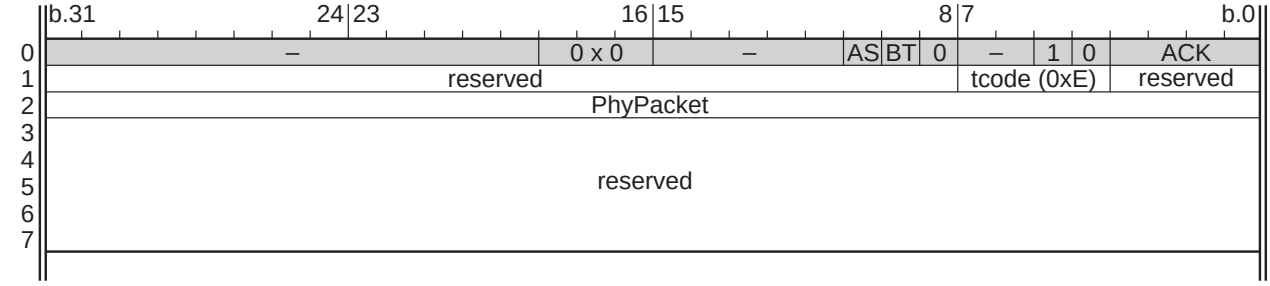
① BlockWriteReq (tcode : 0x1)
LockReq (tcode : 0x9)



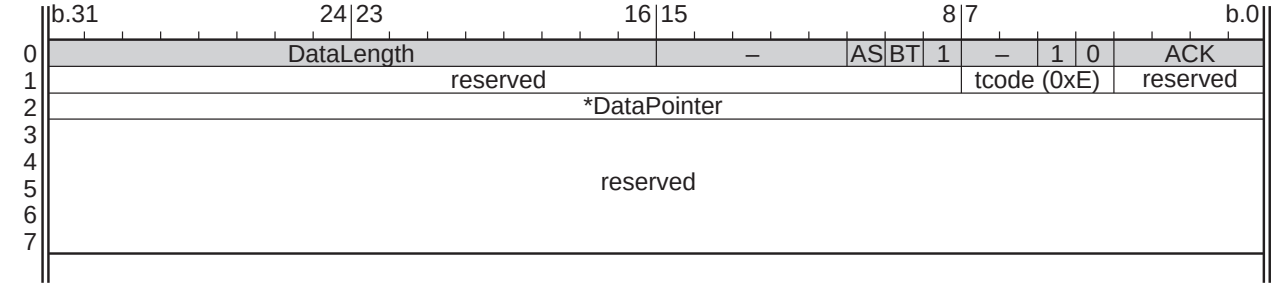
② BlockReadResp (tcode : 0x7)
LockResp (tcode : 0xB)



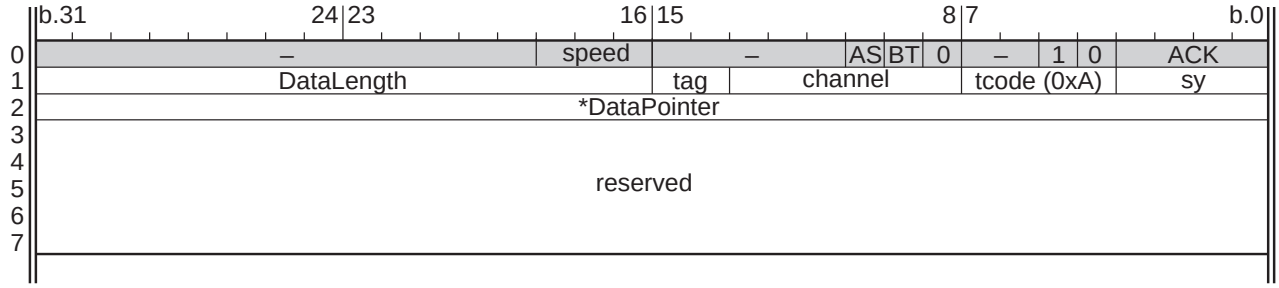
(4) RxAsyncronousePhyPacket Normal (tcode : 0xE)



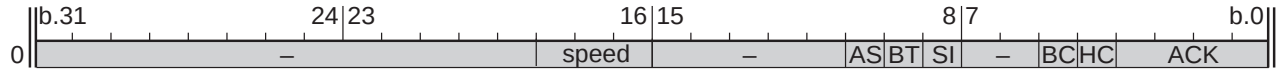
(5) SelfIDPacket Received SelfID packets between BusReset and 1st-ArbRstGap (tcode : 0xE)



(6) RxIsocronousePacket (tcode : 0xA)



Receive Packet Common Format



Name	Bit count	Description
speed	3	Speed Code (Note 1)
AS	1	AreaStatus bit (1: StreamArea, 0: ORBArea)
BT	1	Bit which toggles during the BusReset period.
SI	1	Whether the received packet is a Self ID packet
BC	1	Whether the received packet is a Broadcast packet.
HC	1	Presence/absence of the Header CRC error (1: Packet disabled)
ACK	4	Transmitted AckCode (Note 2)
PSTS	4	AckCode which was scheduled to be transmitted (Note 2)

(Note 1) Refer to the Transmit Packet Common spd (speed code).
(Note 2) Refer to the Transmit Packet Common Ack (AckCode).

7.3 IEEE1394 HARDWARE SBP-2 CONTROL

The hardware SBP2 of this IC automatically executes a PageTable fetch and data transfer according to the Serial Bus Protocol 2 after receiving specifications of its PageTable Size and Address. The control of the SBP2 is performed by accessing the internal register. Data transfer is controlled by the transmission and reception of signals to and from the PHY-LINK interface and the transmission/reception of a series of packets are automatically executed by having access to the internal SRAM area. The functions of this block are as follows.

This Block,

(1) Receives specifications of a Page Table Size, Page Table Address, Speed Code, and Max Payload Size, etc. to automatically execute a PageTable fetch and data transfer according to the Serial Bus Protocol 2.

(2) Can transfer data the equivalent of max. 24-page elements at one time. If no PageTable exists, you can transfer data by directly specifying a data length as a Page Table Size.

(3) Allows you to perform the pause, resume, or reset during data transfer. Though the register value is retained even after the reset, the state machine is restored to the initial state. You can check transfer condition through the register any time.

(4) Immediately enters the error pause when an error arises during data transfer by which you can check an error cause through the register. The resume from the error pause will pick up the transaction where the error arose.

(5) Allows you to transfer data if you specify the omission of the PageTable fetch or Page Element No. to start data.

7.4 IDE INTERFACE CONTROL

This IC contains a block to control the IDE interface. Its functions are as follows.

This block,

(1) Accesses the IDE bus by having access to the Program mode of the CPU.
The access to the data port of the CPU is available only in PIO mode.

(2) Can monitor various kinds of signals of the IDE interface.

(3) Controls the link-up of function blocks in accordance with the control signals and operation end signal from the DMA control circuit.

(4) Manages the condition of data transfer in DMA mode of the IDE by the HDMARQ/XHDMACK signal.

(5) Reads and writes the data of data bus DD15-0 of IDE from and to the FIFO in the 1394LINKCORE by the XHIOR/XHIOW signal.
If the FIFO becomes full or empty to disable data transfer, this block suspends data transfer with specified timing.

7.5 BUILT-IN CPU

Regarding the built-in CPU, refer to the S1C33208/204/202 TECHNICAL MANUAL (and S1C33 Family ASIC Macro Manual).

In the built-in CPU core, however, a DMA controller and A/D converter are not integrated; this part is different from the description on the DMA controller and A/D converter given in TECHNICAL MANUAL (and Macro Manual). A low speed oscillation circuit (OSC1) is not available.

7.6 FLASH CONTROLLER

This IC is provided with a function to perform Erase and Write to the Flash ROM.

(1) Chip Erase
According to a specified sequence, you can erase all memory cells in the built-in Flash ROM to put them in "1" status.
After erasing the chip, check that the data of all memory cells is "1".

(2) Sector Erase
This IC is ready for the Sector Erase in the unit of 512 words/sector.
According to a specified sequence, you can erase all memory cells in the built-in Flash ROM to put them in "1" status.
After erasing the chip, check that the data of all memory cells is "1".

(3) Write
Write is complete if you continue writing Write data in the unit of word until writing of all sectors (512 words) finishes.
On completion of the Sector Write, compare all data in the sectors with original data for confirmation.
You cannot change the data of the memory cell from "0" to "1" by writing.

8. INTERNAL REGISTER

8.1 IEEE1394 LINK CONTROLLER REGISTER MAPPING

8.1.1 Register Table

(The base address of this register is 0x100000.)

Address	Register Name	R/W	Function	Relation
0x00	MainIntStat	R(W)	Main Interrupt Status Register	
0x01	SubIntStat	R(W)	Sub-Interrupt Status Register	
0x02	(Reserved)			
0x03	DmaIntStat	R(W)	DMA Interrupt Status Register	
0x04	LinkIntStat1	R(W)	LINK Core Interrupt Status Register 1	
0x05	LinkIntStat0	R(W)	LINK Core Interrupt Status Register 0	
0x06	PhyIntStat	R(W)	PHY Interrupt Status Register	
0x07	(Reserved)			
0x08	MainIntEnb	R/W	Main Interrupt Enable Flag Register	
0x09	SubIntEnb	R/W	Sub-Interrupt Enable Flag Register	
0x0A	(Reserved)			
0x0B	DmaIntEnb	R/W	DMA Interrupt Enable Flag Register	
0x0C	LinkIntEnb1	R/W	LINK Core Interrupt Enable Flag Register 1	
0x0D	LinkIntEnb0	R/W	LINK Core Interrupt Enable Flag Register 0	
0x0E	PhyIntEnb	R/W	PHY Interrupt Enable Flag Register	
0x0F	(Reserved)			
0x10	ChipCtl	R/W	Chip Control Register	
0x11	HW_Revision	R/W	Hardware Revision Register	
0x12	(Reserved)			
0x13	(Reserved)			
0x14	(Reserved)			
0x15	(Reserved)			
0x16	(Reserved)			
0x17	(Reserved)			
0x18	LinkCtl_H	R/W	LINK Core Control Register	Higher Rank
0x19	LinkCtl_L	R/W	LINK Core Control Register	Lower Rank
0x1A	LinkStat	R	LINK Core Status Read Register	
0x1B	PriReqCnt	R	Priority Request Count Register	
0x1C	RetryLimit_H	R/W	Dual Retry Time Set Register	Higher Rank
0x1D	RetryLimit_L	R/W	Dual Retry Time Set Register	Lower Rank
0x1E	MaxRetry	R/W	Single Retry Number Set Register	
0x1F	IRM_Stat	R/W	IRM Status Register	
0x20	NODE_IDS_H	R/W	Node IDS Status Register	Higher Rank
0x21	NODE_IDS_L	R/W	Node IDS Status Register	Lower Rank
0x22	(Reserved)			
0x23	(Reserved)			
0x24	PhyAccCtl_H	R/W	LINK Core Control Register	Middle Rank
0x25	PhyAccCtl_L	R/W	LINK Core Control Register	Lower Rank
0x26	PhyRdstat_H	R	LINK Core Status Read Register	
0x27	PhyRdstat_L	R/W	Priority Request Count Register	
0x28	ChnlIndex	R/W	ISO Async Stream Channel Index Register	
0x29	ChnlWindow	R/W	ISO Async Stream Channel Window Register	
0x2A	CmprIndex	R/W	Compare Offset Address Index Register	
0x2B	CmpRW indow	R/W	Compare Offset Address Window Register	
0x2C	CYCLE_TIME_H	R/W	Cycle Time Register	Higher Rank

Address	Register Name	R/W	Function	Relation
0x2D	CYCLE_TIME_MH	R/W	Cycle Time Register	
0x2E	CYCLE_TIME_ML	R/W	Cycle Time Register	
0x2F	CYCLE_TIME_L	R/W	Cycle Time Register	Lower Rank
0x30	HwSBP2Ctl	R/W	Hardware SBP2 Control Register	
0x31	HwSBP2Stat	R/W	Hardware SBP2 Status Read Register	
0x32	HwSBP2IntStat	R(W)	Hardware SBP2 Interrupt Status Register	
0x33	HwSBP2Index	R/W	Hardware SBP2 Index Register	
0x34	HwSBP2Window_H	R/W	Hardware SBP2 Window Register	Higher Rank
0x35	HwSBP2Window_L	R/W	Hardware SBP2 Window Register	Lower Rank
0x36	PayloadSize_H	R/W	Hardware SBP2 Payload Size Set Register	Higher Rank
0x37	PayloadSize_L	R/W	Hardware SBP2 Payload Size Set Register	Lower Rank
0x38	PageTableSize_H	R/W	Hardware PageTable Size Set Register	Higher Rank
0x39	PageTableSize_L	R/W	Hardware PageTable Size Set Register	Lower Rank
0x3A	PageTableAdrs0	R/W	Hardware SBP2 PageTable Address Set Register	Higher Rank
0x3B	PageTableAdrs1	R/W	Hardware SBP2 PageTable Address Set Register	
0x3C	PageTableAdrs2	R/W	Hardware SBP2 PageTable Address Set Register	
0x3D	PaqeTableAdrs3	R/W	Hardware SBP2 PageTable Address Set Register	
0x3E	PageTableAdrs4	R/W	Hardware SBP2 PageTable Address Set Register	
0x3F	PageTableAdrs5	R/W	Hardware SBP2 PageTable Address Set Register	Lower Rank
0x40	LinkRxHdrPtr_H	R/W	Receive Header LINK Pointer Register	Higher Rank
0x41	LinkRxHdrPtr_L	R/W	Receive Header LINK Pointer Register	Lower Rank
0x42	LinkRxORBPtr_H	R/W	Receive ORB Data LINK Pointer Register	Higher Rank
0x43	LinkRxORBPtr_L	R/W	Receive ORB Data LINK Pointer Register	Lower Rank
0x44	LinkRxStreamPtr_H	R/W	Receive Stream Data LINK Pointer Register	Higher Rank
0x45	LinkRxStreamPtr_L	R/W	Receive Stream Data LINK Pointer Register	Lower Rank
0x46	LinkTxStreamPtr_H	R	Receive Stream Data LINK Pointer Register	Higher Rank
0x47	LinkTxStreamPtr_L	R	Receive Stream Data LINK Pointer Register	Lower Rank
0x48	UsedRxHdrPtr_H	R/W	Used Receive Header Pointer Register	Higher Rank
0x49	UsedRxHdrPtr_L	R/W	Used Receive Header Pointer Register	Lower Rank
0x4A	UsedRxORBPtr_H	R/W	Used Receive ORB Data Pointer Register	Higher Rank
0x4B	UsedRxORBPtr_L	R/W	Used Receive ORB Data Pointer Register	Lower Rank
0x4C	IDE_RxStreamPtr_H	R/W	Receive Stream Data IDE Pointer Register	Higher Rank
0x4D	IDE_RxStreamPtr_L	R/W	Receive Stream Data IDE Pointer Register	Lower Rank
0x4E	IDE_TxStreamPtr_H	R/W	Receive Stream Data IDE Pointer Register	Higher Rank
0x4F	IDE_TxStreamPtr_L	R/W	Receive Stream Data IDE Pointer Register	Lower Rank
0x50	BufControl	R/W	Buffer Control Register	
0x51	BufMonitor	R	Buffer Monitor Register	
0x52	AsyDmaCtl	R/W	Async TxDMA Control Register	
0x53	IsoDmaCtl	R/W	ISO TxDMA Control Register	
0x54	RxDmaCtl	R/W	RxDMA Control Register	
0x55	AreaIndex	R/W	Memory Map Area Set Index Register	
0x56	AreaWindow_H	R/W	Memory Map Area Set Window Register	Higher Rank
0x57	AreaWindow_L	R/W	Memory Map Area Set Window Register	Lower Rank
0x58	BRstHdrPtr_H	R	Bus Reset Header Pointer Register	Higher Rank
0x59	BRstHdrPtr_L	R	Bus Reset Header Pointer Register	Lower Rank
0x5A	BRstORBPtr_H	R	Bus Reset ORB Pointer Register	Higher Rank
0x5B	BRstORBPtr_L	R	Bus Reset ORB Pointer Register	Lower Rank
0x5C	(Reserved)			
0x5D	(Reserved)			
0x5E	MaintCtl_H	R/W	Maintenance Control Register	Higher Rank
0x5F	MaintCtl_L	R/W	Maintenance Control Register	Lower Rank

Address	Register Name	R/W	Function	Relation
0x60	IDE_Config0	R/W	IDE Configuration Register	
0x61	IDE_Config1	R/W	IDE Configuration Register	
0x62	IDE_RegAccCyc	R/W	IDE Register Access Cycle Register	
0x63	IDE_PioDmaCyc	R/W	IDE PIO/DMA Cycle Register	
0x64	IDE_UltraDmaCyc	R/W	IDE Ultra DMA Cycle Register	
0x65	IDE_DmaCtl	R/W	IDE DMA Control Register	
0x66	IDE_BusStat	R/W	IDE Bus Status Read Register	
0x67	IDE_DmaStat	R/W	IDE DMA Status Register	
0x68	IDE_ByteCount0	R/W	IDE Byte Count Set Register	Higher Rank
0x69	IDE_ByteCount1	R/W	IDE Byte Count Set Register	
0x6A	IDE_ByteCount2	R/W	IDE Byte Count Set Register	
0x6B	IDE_ByteCount3	R/W	IDE Byte Count Set Register	Lower Rank
0x6C	IDE_CRC0	R	CRC Read Register	Higher Rank
0x6D	IDE_CRC1	R	CRC Read Register	Lower Rank
0x6E	(Reserved)			
0x6F	(Reserved)			
0x70	IDE_CS00	R/W	IDE Command Block Register	
0x71	IDE_CS01	R/W	IDE Command Block Register	
0x72	IDE_CS02	R/W	IDE Command Block Register	
0x73	IDE_CS03	R/W	IDE Command Block Register	
0x74	IDE_CS04	R/W	IDE Command Block Register	
0x75	IDE_CS05	R/W	IDE Command Block Register	
0x76	IDE_CS06	R/W	IDE Command Block Register	
0x77	IDE_CS07	R/W	IDE Command Block Register	
0x78	IDE_CS10	R/W	IDE Command Control Register	
0x79	IDE_CS11	R/W	IDE Command Control Register	
0x7A	IDE_CS12	R/W	IDE Command Control Register	
0x7B	IDE_CS13	R/W	IDE Command Control Register	
0x7C	IDE_CS14	R/W	IDE Command Control Register	
0x7D	IDE_CS15	R/W	IDE Command Control Register	
0x7E	IDE_CS16	R/W	IDE Command Control Register	
0x7F	IDE_CS17	R/W	IDE Command Control Register	

8.1.2 Register/Bit Table

The base address of this register is 0x100000.

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	MainIntStat	SubIntStat	TxIsoCmp	RxDmaCmp	TxAsyCmp	HwSBP2Cmp	IDE_DmaCm	IDE_INTRQ	BusReset
0x01	SubIntStat	SelfIDdone	SelfIDerr	HwSBP2Err	HwSBP2BRs	LinkIntStat1	LinkIntStat0	PhyIntStat	DmaIntStat
0x02	(Reserved)								
0x03	DmaIntStat		TxAsyRtyGo	TxAsyBCSent	RxDmaFaild	TxAsyFaild	TxIsoFaild	TxAsyBRAbort	TxAsyMiss
0x04	LinkIntStat1					RxOnTardy	RxHcrcErr	RxUnkTcode	TxRtyExced
0x05	LinkIntStat0	UnExpCh	DupliCh	IsoArbFaild	CycTooLong	CycOverFlw	CycEvent	CycLost	CycArbFail
0x06	PhyIntStat	SubGap	ArbGap				Phy_int	PhyWrDone	PhyRdDone
0x07	(Reserved)								
0x08	MainIntEnb	EnSubIntStat	EnTxIsoCmp	EnRxDmaCmp	EnTxAsyCmp	EnHwSBP2Cm	EnIDE_DmaC	EnIDE_INTRQ	EnBusReset
0x09	SubIntEnb	EnSelfIDdone	EnSelfIDerr	EnHwSBP2Err	EnHwSBP2BRst	EnLinkIntStat1	EnLinkIntStat0	EnPhyIntStat	EnDmaIntStat
0x0A	(Reserved)								
0x0B	DmaIntEnb		EnTxAsyRtyGo	EnTxAsyBCSe	EnRxDmaFaild	EnTxAsyFaild	EnTxIsoFaild	EnTxAsyBRAb	EnTxAsyMiss
0x0C	LinkIntEnb1					EnRxOnTardy	EnRxHcrcErr	EnRxUnkTcod	EnTxRtyExced
0x0D	UltraDmaMode	EnUnExpCh	EnDupliCh	EnIsoArbFaild	EnCycTooLon	EnCycOverFlw	EnCycEvent	EnCycLost	EnCycArbFail
0x0E	PhyIntEnb	EnSubGap	EnArbGap				EnPhy_int	EnPhyWrDone	EnPhyRdDone
0x0F	(Reserved)								
0x10	ChipCtl	Suspend					IDE_MdlRst	SendTardy	SoftReset
0x11	HW_Revision	HW_Revision[7:0]							
0x12	ApetusTestOutPut_H	Chip Test Register							
0x13	ApetusTestOutPut_L								
0x14	LCTestIndex								
0x15	LCTestWindow								
0x16	SBP2TestIndex								
0x17	SBP2TestWindow								
0x18	LinkCtl_H	PassSelfID	PassPhyPkt	PassBrPkt	EnPosWB	EnPosWQ	APHY	EnAcc	Cmstr
0x19	LinkCtl_L	EnLink		PLIFrst	IgnrBChdr	IgnrBCdata	RxBusyMode	DualRtyEnb	SinglRtyEnb
0x1A	LinkStat						ID_Valid	Root	CablPwSts
0x1B	PriReqCnt			Priority Budget Request Count [5:0]					
0x1C	RetryLimit_H	SecLimit[2:0]			CycLimit[12:8]				
0x1D	RetryLimit_L	CycLimit[7:0]							
0x1E	MaxRetry					MaxRetry[3:0]			
0x1F	IRM_Stat	NoIRM	WonIRM	IRM_ID[5:0]					
0x20	NODE_IDS_H	BusID[9:2]							
0x21	NODE_IDS_L	BusID[1:0]		Physical ID[5:0]					
0x22	(Reserved)								
0x23	(Reserved)								
0x24	PhyAccCtl_H	RdReq	WrReq			Request Address[3:0]			
0x25	PhyAccCtl_L	Write Data[7:0]							
0x26	PhyRdstat_H					Read Address[3:0]			
0x27	PhyRdstat_L	Read Data[7:0]							
0x28	ChnlIndex					Channel Index			
0x29	ChnlWindow	Channel Window							
0x2A	CmprIndex					Compare Address Index			
0x2B	CmprWindow	Compare Address Window							
0x2C	CYCLE_TIME_H	Cycle Second[6:0]							CycCnt[12]
0x2D	CYCLE_TIME_MH	Cycle Count[11:4]							
0x2E	CYCLE_TIME_ML	Cycle Count[3:0]				Cycle Offset[11:8]			
0x2F	CYCLE_TIME_L	Cycle Offset[7:0]							

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x30	HwSBP2Ctl	PtNotPresen	HOSTtoDev	FromStream	LastPT	HwSBP2Rst	HwSBP2Rsu	HwSBP2Pau	HwSBP2Star
0x31	HwSBP2Stat	FwPause	ErrPause	NotQuadEnb	WaitPLRead	HwSBP2Exe	PTaskExec	StTaskExec	TranExec
0x32	HwSBP2IntStat	SplitTimeOut	TxAckedIlleg	TxAckMiss	BRAbort	NotQuad	RxNotRespCm	RxBroadCast	RxAckDataErr
0x33	HwSBP2Index					HwSBP2 Index			
0x34	HwSBP2Window_H	(MSB)			HwSBP2 Window				
0x35	HwSBP2Window_L								(LSB)
0x36	PayloadSize_H	(MSB)			Payload Size				
0x37	PayloadSize_L								(LSB)
0x38	PageTableSize_H	(MSB)			Page Table Size				
0x39	PageTableSize_L								(LSB)
0x3A	PageTableAdrs0	(MSB)							
0x3B	PageTableAdrs1								
0x3C	PageTableAdrs2				Page Table Offset Address				
0x3D	PaqeTableAdrs3								
0x3E	PageTableAdrs4								
0x3F	PageTableAdrs5								(LSB)
0x40	LinkRxHdrPtr_H				LinkRxHdrPtr[12:8]				
0x41	LinkRxHdrPtr_L	LinkRxHdrPtr[7:5]							
0x42	LinkRxORBPtr_H				LinkORBPointer[12:8]				
0x43	LinkRxORBPtr_L	LinkRxORBPtr[7:2]							
0x44	LinkRxStreamPtr_H				LinkRxStreamPtr[12:8]				
0x45	LinkRxStreamPtr_L	LinkRxStreamPtr[7:2]							
0x46	LinkTxStreamPtr_H				LinkTxStreamPtr[12:8]				
0x47	LinkTxStreamPtr_L	LinkTxStreamPtr[7:2]							
0x48	UsedRxHdrPtr_H				UsedRxHdrPtr[12]				
0x49	UsedRxHdrPtr_L	UsedRxHdrPtr[7:5]							
0x4A	UsedRxORBPtr_H				UsedRxORBPtr[12:8]				
0x4B	UsedRxORBPtr_L	UsedRxORBPtr[7:2]							
0x4C	IDE_RxStreamPtr_H				IDE_RxStreamPtr[12:8]				
0x4D	IDE_RxStreamPtr_L	IDE_RxStreamPtr[7:2]							
0x4E	IDE_TxStreamPtr_H				IDE_TxStreamPtr[12:8]				
0x4F	IDE_TxStreamPtr_L	IDE_TxStreamPtr[7:2]							
0x50	BufControl	TxStreamClr	RxStreamClr	RxORBClr	RxHdrClr				UpdLinkTxStrm
0x51	BufMonitor	RxPayldRdy	TxPayldRdy			RxHdrRemain	RxORBFull	RxStreamFull	RxHdrFull
0x52	AsyDmaCtl	AsyChnlSel			BlkWrAreaSel	AsyFIFOEpty	AsyFIFOClr	AsyTxMon	AsyStart
0x53	IsoDmaCtl	IsoChnlSel			SelTxPtr	IsoFIFOEpty	IsoFIFOClr	IsoTxMon	IsoStart
0x54	RxDmaCtl					RxFIFOEpty	RxFIFOClr	RxMon	ForceBusy
0x55	AreaIndex					Memory Map Area Index			
0x56	AreaWindow_H	(MSB)			Memory Map Area Window				
0x57	AreaWindow_L								(LSB)
0x58	BRstHdrPtr_H				BusReset Header Pointer[12:8]				
0x59	BRstHdrPtr_L	BusResetHeaderPointer[7:5]							
0x5A	BRstORBPtr_H				BusResetORBPointer[12:8]				
0x5B	BRstORBPtr_L	BusResetORBPointer[7:2]							
0x5C	(Reserved)								
0x5D	(Reserved)								
0x5E	MaintCtl_H	E_Hcrc	E_Dcrc	No_Pkt	F_Ack	N_ack			
0x5F	MaintCtl_L	Ack[7:0]							

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x60	IDE_Config0	UltraDmaMode	DmaMode	ActPort	IDE_Slave	DMARQ_Leve	Swap		
0x61	IDE_Config1	IDE_Reset					XDIOW_DLYen		
0x62	IDE_RegAccCyc	Assert Pulse[3:0]				Negate Pulse[3:0]			
0x63	IDE_PioDmaCyc	Assert Pulse[3:0]				Negate Pulse[3:0]			
0x64	IDE_UltraDmaCyc					Cycle Time[3:0]			
0x65	IDE_DmaCtl			IncFIFOCnt	CRC_Clear	FIFO_Clear	IDE_Abort	IDE_Directio	DmaStart
0x66	IDE_BusStat	DMARQ	DMACK	INTRQ	IORDY			DIAG	DASP
0x67	IDE_DmaStat		FIFOCnt[2:0]					DmaPause	DmaRun
0x68	IDE_ByteCount0	(MSB)	IDE DMA xfer Byte Count						
0x69	IDE_ByteCount1								
0x6A	IDE_ByteCount2								
0x6B	IDE_ByteCount3								(LSB)
0x6C	IDE_CRC0	(MSB)	Ultra DMA CRC Value						
0x6D	IDE_CRC1								(LSB)
0x6E	IDE_TestIndex	Chip Test Register							
0x6F	IDE_TestWindow								
0x70	IDE_CS00	Command Block register			R- Data			W- Data	
0x71	IDE_CS01	Command Block register			R- Error			W- Features	
0x72	IDE_CS02	Command Block register			R- Sector Count			W- Sector Count	
0x73	IDE_CS03	Command Block register			R- Sector Number/LBA[bit0-7]			W- Sector Number/LBA[bit0-7]	
0x74	IDE_CS04	Command Block register			R- Cylinder Low/LBA[bit8-15]			W- Cylinder Low/LBA[bit8-15]	
0x75	IDE_CS05	Command Block register			R- Cylinder High/LBA[bit[16-23]			W- Cylinder High/LBA[bit[16-23]	
0x76	IDE_CS06	Command Block register			R- Device/Head,LBA[bit24-27]			W- Device/Head,LBA[bit24-27]	
0x77	IDE_CS07	Command Block register			R- Status			W- Command	
0x78	IDE_CS10	Control Block Register			R- Data Bus Hi-Impedence			W- Not Used	
0x79	IDE_CS11	Control Block Register			R- Data Bus Hi-Impedence			W- Not Used	
0x7A	IDE_CS12	Control Block Register			R- Data Bus Hi-Impedence			W- Not Used	
0x7B	IDE_CS13	Control Block Register			R- Data Bus Hi-Impedence			W- Not Used	
0x7C	IDE_CS14	Control Block Register			R- Data Bus Hi-Impedence			W- Not Used	
0x7D	IDE_CS15	Control Block Register			R- Data Bus Hi-Impedence			W- Not Used	
0x7E	IDE_CS16	Control Block Register			R- Alternate Status			W- Device Control	
0x7F	IDE_CS17	Control Block Register			R- (obsolete)			W- Not Used	

LinkChnnel Index/Window Register

ChnlIndex									
	ChnlWindow	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	ChannelAvailableH0		ch01	ch02	ch03	ch04	ch05	ch06	ch07
0x01	ChannelAvailableH1	ch08	ch09	ch10	ch11	ch12	ch13	ch14	ch15
0x02	ChannelAvailableH2	ch16	ch17	ch18	ch19	ch20	ch21	ch22	ch23
0x03	ChannelAvailableH3	ch24	ch25	ch26	ch27	ch28	ch29	ch30	ch31
0x04	ChannelAvailableL0	ch32	ch33	ch34	ch35	ch36	ch37	ch38	ch39
0x05	ChannelAvailableL1	ch40	ch41	ch42	ch43	ch44	ch45	ch46	ch47
0x06	ChannelAvailableL2	ch48	ch49	ch50	ch51	ch52	ch53	ch54	ch55
0x07	ChannelAvailableL3	ch56	ch57	ch58	ch59	ch60	ch61	ch62	ch63
0x08	ReceiveChannel0	ch00	ch01	ch02	ch03	ch04	ch05	ch06	ch07
0x09	ReceiveChannel1	ch08	ch09	ch10	ch11	ch12	ch13	ch14	ch15
0x0A	ReceiveChannel2	ch16	ch17	ch18	ch19	ch20	ch21	ch22	ch23
0x0B	ReceiveChannel3	ch24	ch25	ch26	ch27	ch28	ch29	ch30	ch31
0x0C	ReceiveChannel4	ch32	ch33	ch34	ch35	ch36	ch37	ch38	ch39
0x0D	ReceiveChannel5	ch40	ch41	ch42	ch43	ch44	ch45	ch46	ch47
0x0E	ReceiveChannel6	ch48	ch49	ch50	ch51	ch52	ch53	ch54	ch55
0x0F	ReceiveChannel7	ch56	ch57	ch58	ch59	ch60	ch61	ch62	ch63

Compare Address Index/Window Register

CmprIndex									
	ChnlWindow	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
0x00	CompareDOffset0	(MSB)							
0x01	CompareDOffset1								
0x02	CompareDOffset2				Compare Destination Offset Address[47:0]				
0x03	CompareDOffset3								
0x04	CompareDOffset4								
0x05	CompareDOffset5								(LSB)
0x06	(Reserved)								
:	(Reserved)								
0x0F	(Reserved)								

H/W SBP2 Index Chnnel/Window Register

SBP2Index									
	SBP2Window_H/L	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
0x00	PageBoundary						PageBoundary[2:0]		
	PageElementNunber				PageElementNumber[4:0]				
0x01	PgElmentRemain_H	(MSB)			Page Element Remain Length (Bytes)				
	PgElmentRemain_L								(LSB)
0x02	SpeedCode						SpeedCode[2:0]		
	MaxPayload					MaxPayload[3:0]			
0x03	DestinationID_H	(MSB)							
	DestinationID_L				Destination_ID Value				(LSB)
0x04	SplitTime_H		Second[2:0]			Cycle Count[12:8]			
	SplitTime_L				Cycle Count[7:0]				
0x05	(Reserved)								
:	(Reserved)								
0x0F	(Reserved)								

Memory Map Area Index/Window Register

AreaIndex									
	AreaWindow_H/L	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
0x00	RxORBAreaStart_H				(MSB)		RxORBAreaStart[12:8]		
	RxORBAreaStart_L			RxORBAreaStart[7:2]			(LSB)		
0x01	TxHdrAreaStart_H				(MSB)		TxHdrAreaStart[12:8]		
	TxHdrAreaStart_L			TxHdrAreaStart[7:2]			(LSB)		
0x02	TxStreamAreaStart_H				(MSB)		TxStreamAreaStart[12:8]		
	TxStreamAreaStart_L			TxStreamAreaStart[7:2]			(LSB)		
0x03	TxStreamAreaEnd_H				(MSB)		TxStreamAreaEnd[12:8]		
	TxStreamAreaEnd_L			TxStreamAreaEnd[7:2]			(LSB)		
0x04	RxStreamAreaStart_H				(MSB)		RxStreamAreaStart[12:8]		
	RxStreamAreaStart_L			RxStreamAreaStart[7:2]			(LSB)		
0x05	(Reserved)								
:	(Reserved)								
0x0F	(Reserved)								

8.1.3 Register Map

(The base address of this register is 0x100000.)

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x00	MainIntStat	7:SubIntStat 6: TxIsoCmp 5: RxDmaCmp 4: TxAsyCmp 3: HwSBP2Cmp 2: IDE_DmaCmp 1: IDE_INTRQ 0: BusReset	R(W) R(W) R(W) R(W) R(W) R(W) R(W) R(W)	0: None 0: None 0: None 0: None 0: None 0: None 0: None 0: None	1: Sub Interrupt Occurred 1: ISO Pkt Transmit Done 1: Packet Reception 1: AckCode Reception 1: HwSBP2 Process Complete 1: IDE DMA Transmit Complete 1: IDE Interface Interrupt 1: Bas Reset Detected	0x00	0x00	–
0x01	SubIntStat	7: SelfIDdone 6: SelfIDerr 5: HwSBP2Err 4: HwSBP2BRst 3: LinkIntStat1 2: LinkIntStat0 1: PhyIntStat 0: DmaIntStat	R(W) R(W) R(W) R(W) R(W) R(W) R(W) R(W)	0: None 0: None 0: None 0: None 0: None 0: None 0: None 0: None	1: Self-ID Phase Done 1: Self-ID Packet Error 1: Hw SBP2 Error 1: BusReset in process HwSBP 1: Link1 Interrupt Occurred 1: Link0 Interrupt Occurred 1: PHY Interrupt Occurred 1: Dma Interrupt Occurred	0x00	0x00	–
0x02	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x03	DmaIntStat	7: 6: TxAsyRtyGo 5: TxAsyBCSent 4: RxDmaFaild 3: TxAsyFaild 2: TxIsoFaild 1: TxAsyBRAbort 0: TxAsyMiss	 R(W) R(W) R(W) R(W) R(W) R(W) R(W)	0: 0: None 0: None 0: None 0: None 0: None 0: None 0: None	1: 1: Async Tx Retry Go 1: AsyncTxBroadcast Sent 1: Rx DMA Failed 1: Async Tx Failed 1: ISO Tx Failed 1: Async Tx BusReset Abort 1: AsyncTxAckCodeMissing	0x00	0x00	–
0x04	LinkIntStat1	7: 6: 5: 4: 3: RxOnTardy 2: RxHcrcErr 1: RxUnkTcode 0: TxRtyExced	 R(W) R(W) R(W) R(W)	0: 0: 0: 0: None 0: None 0: None 0: None	1: 1: 1: 1: 1: Ack_tardy Sent 1: Rx Packet Header CRC Err 1: Rx Packet Tcode Unknown 1: Tx Retry Exceeded	0x00	0x00	–
0x05	LinkIntStat0	7: UnExpCh 6: DupliCh 5: IsoArbFaild 4: CycTooLong 3: CycOverFlw 2: CycEvent 1: CycLost 0: CycArbFail	R(W) R(W) R(W) R(W) R(W) R(W) R(W) R(W)	0: None 0: None 0: None 0: None 0: None 0: None 0: None 0: None	1: Unknown Expected Channel 1: DuplicateChannelDetected 1: Iso Arbtration Failed 1: ISO Arbitration Failed 1: Cycle Timer Over Fullow 1: Local Cycle Event Occured 1: Cycle Start Packet Lost 1: CycleStartPkt Arbtration Fail	0x00	0x00	–
0x06	PhyIntStat	7: SubGap 6: ArbGap 5: 4: 3: 2: Phy_int 1: PhyWrDone 0: PhyRdDone	R(W) R(W) R(W) R(W) R(W)	0: None 0: None 0: 0: 0: 0: None 0: None 0: None	1: Sub Action Gap Detected 1: ArbtrationResetGapDetected 1: 1: 1: 1: PHY Interrupt Detected 1: PHY Register Write Done 1: PHY Register Read Done	0x00	0x00	–
0x07	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x08	MainIntEnb	7: EnSubIntStat	R/W	0: Disable	1: Enable	0x00	0x00	–
		6: EnTxIsoCmp	R/W	0: Disable	1: Enable			
		5: EnRxDmaCmp	R/W	0: Disable	1: Enable			
		4: EnTxAsyCmp	R/W	0: Disable	1: Enable			
		3: EnHwSBP2Cmp	R/W	0: Disable	1: Enable			
		2: EnIDE_DmaCmp	R/W	0: Disable	1: Enable			
		1: EnIDE_INTRQ	R/W	0: Disable	1: Enable			
		0: EnBusReset	R/W	0: Disable	1: Enable			
0x09	SubIntEnb	7: EnSelfIDdone	R/W	0: Disable	1: Enable	0x00	0x00	–
		6: EnSelfIDerr	R/W	0: Disable	1: Enable			
		5: EnHwSBP2Err	R/W	0: Disable	1: Enable			
		4: EnHwSBP2BRst	R/W	0: Disable	1: Enable			
		3: EnLinkIntStat1	R/W	0: Disable	1: Enable			
		2: EnLinkIntStat0	R/W	0: Disable	1: Enable			
		1: EnPhyIntStat	R/W	0: Disable	1: Enable			
		0: EnDmaIntStat	R/W	0: Disable	1: Enable			
0x0A	(Reserved)	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0:		0:	1:			
0x0B	DmaIntEnb	7:		0:	1:	0x00	0x00	–
		6: EnTxAsyRtyGo	R/W	0: Disable	1: Enable			
		5: EnTxAsyBCSent	R/W	0: Disable	1: Enable			
		4: EnRxDmaFaild	R/W	0: Disable	1: Enable			
		3: EnTxAsyFaild	R/W	0: Disable	1: Enable			
		2: EnTxIsoFaild	R/W	0: Disable	1: Enable			
		1: EnTxAsyBRAbort	R/W	0: Disable	1: Enable			
		0: EnTxAsyMiss	R/W	0: Disable	1: Enable			
0x0C	LinkIntEnb1	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3: EnRxOnTardy	R/W	0: Disable	1: Enable			
		2: EnRxHcrcErr	R/W	0: Disable	1: Enable			
		1: EnRxUnkTcode	R/W	0: Disable	1: Enable			
		0: EnTxRtyExced	R/W	0: Disable	1: Enable			
0x0D	LinkIntEnb0	7: EnUnExpCh	R/W	0: Disable	1: Enable	0x00	0x00	–
		6: EnDupliCh	R/W	0: Disable	1: Enable			
		5: EnIsoArbFaild	R/W	0: Disable	1: Enable			
		4: EnCycTooLong	R/W	0: Disable	1: Enable			
		3: EnCycOverFlw	R/W	0: Disable	1: Enable			
		2: EnCycEvent	R/W	0: Disable	1: Enable			
		1: EnCycLost	R/W	0: Disable	1: Enable			
		0: EnCycArbFail	R/W	0: Disable	1: Enable			
0x0E	PhyIntEnb	7: EnSubGap	R/W	0: Disable	1: Enable	0x00	0x00	–
		6: EnArbGap	R/W	0: Disable	1: Enable			
		5:		0:	1:			
		4:		0:	1:			
		3:		0:	1:			
		2: EnPhy_int	R/W	0: Disable	1: Enable			
		1: EnPhyWrDone	R/W	0: Disable	1: Enable			
		0: EnPhyRdDone	R/W	0: Disable	1: Enable			
0x0F	(Reserved)	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0:		0:	1:			

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x10	ChipCtl	7: Suspend 6: 5: 4: 3: 2: IDE_MdlRst 1: SendTardy 0: SoftReset	R/W W R/W W	0: Resume 0: 0: 0: 0: 0: None 0: None 0: None	1: Suspend 1: 1: 1: 1: 1: IDE_Module Reset 1: Send Ack_tardy 1: Reset Start	0x00	0x00	–
0x11	HW_Revision	7: HW_Revision[7] 6: HW_Revision[6] 5: HW_Revision[5] 4: HW_Revision[4] 3: HW_Revision[3] 2: HW_Revision[2] 1: HW_Revision[1] 0: HW_Revision[0]	R	Indicate Hard Ware Revison Number		0x03	0x03	0x03
0x12	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x13	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x14	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x15	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x16	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x17	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x18	LinkCtl_H	7: PassSelfID		0: Non PassSelfID	1: Self–ID to DMA FIFO			
		6: PassPhyPkt		0: Non Pass PHY Packet	1: PHY Pkt to DMA FIFO			
		5: PassBrPkt		0: Non Pass BusRst Packet	1: BusRst Pkt to DMA FIFO			
		4: EnPosWB	R/W	0: Disable Posted WB	1: Enable Posted WB	0x00	0x00	–
		3: EnPosWQ		0: Disable Poosted WQ	1: Enable Posted WQ			
		2: APHY		0: PHY 1394.a uncorrespond	1: PHY 1394.a correspond			
		1: EnAcc		0: Ack Acceleration Disable	1: Ack Acceleration Enable			
		0: Cmstr		0: Cycle Master Not Capabl	1: Cycle Master Capable			
0x19	LinkCtl_L	7: EnLink	R/W	0: Disable Link	1: Enable Link		–	–
		6:		0:	1:			
		5: PLIFrst	W	0: NONE	1: Reset PHY/Link I/F		0	–
		4: IgnrBChdr	R/W	0: BC Pkt to DMA FIFO	1: Ignore BC Packet	0x00	0	–
		3: IgnrBCdata	R/W	0: BC Data to DMA FIFO	1: Ignore BC–Data		0	–
		2: RxBusyMode	R/W	0: Dual	1: Single		0	–
		1: DualRtyEnb	R/W	0: Dual Retry Disable	1: Dual Retry Enable		0	–
		0: SinglRtyEnb	R/W	0: Single Retry Disable	1: Single Retry Enable		0	–
0x1A	LinkStat	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	–	–
		3:		0:	1:			
		2: ID_Valid	R	0: PhyID Invalid	1: PhyID Valid			
		1: Root	R	0: Self Node = Not Root	1: Self Node = Root			
		0: CablPwSts	R	0: Cable Power Status NG	1: Cable Power Status OK			
0x1B	PriReqCnt	7:		0:	1:			
		6:		0:	1:			
		5: PriReq[5]						
		4: PriReq[4]						
		3: PriReq[3]	R/W	Maximum Number of certain Priority Arb Request		0x00	0x00	0x00
		2: PriReq[2]						
		1: PriReq[1]						
		0: PriReq[0]						
0x1C	RetryLimit_H	7: SecLimit[2]		Dual Phase Retry Limit				
		6: SecLimit[1]	R/W	Second Limit				
		5: SecLimit[0]						
		4: CycLimt[12]						
		3: CycLimt[11]						
		2: CycLimt[10]				0x00	0x00	–
		1: CycLimt[9]						
		0: CycLimt[8]						
0x1D	RetryLimit_L	7: CycLimt[7]	R/W	Cycle Limit				
		6: CycLimt[6]						
		5: CycLimt[5]		If (SecLimit == 0 and CycLimit==0)				
		4: CycLimt[4]		Dual Phase is ignore		0x00	0x00	–
		3: CycLimt[3]						
		2: CycLimt[2]						
		1: CycLimt[1]						
		0: CycLimt[0]						
0x1E	MaxRetry	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3: maxRty[3]		Single Phase Retry Limit				
		2: maxRty[2]	R/W	Max Retry Count Value				
		1: maxRty[1]		If maxRty == 0, Single Phase Retry is ignore				
		0: maxRty[0]						
0x1F	IRM_Stat	7: NoIRM	R	0: Exist IRM Node	1: None IRM Node			
		6: WonIRM	R(W)	0: Other Node	1: Self Node			
		5: IRMID[5]						
		4: IRMID[4]						
		3: IRMID[3]	R	Physical ID of IRM Node		0x3F	–	0x3F
		2: IRMID[2]		No exist IRM Node then IRMID= 0x3F				
		1: IRMID[1]						
		0: IRMID[0]						

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x20	NODE_IDS_H	7: BusID[9] 6: BusID[8] 5: BusID[7] 4: BusID[6] 3: BusID[5] 2: BusID[4] 1: BusID[3] 0: BusID[2]	R/W	Serial Bus ID Number Single Bus, Bus ID = 0x3FF Multiple Bus, Bus ID is uniquely specifying		0xFF	–	–
0x21	NODE_IDS_L	7: BusID[1] 6: BusID[0]						– –
		5: PhyID[5] 4: PhyID[4] 3: PhyID[3] 2: PhyID[2] 1: PhyID[1] 0: PhyID[0]	R	Self Node's Physical ID Number		0xFF	–	1 1 1 1 1 1
0x22	(Reserved)	7: 6: 5: 4: 2: 1: 0:	3:	0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x23	(Reserved)	7: 6: 5: 4: 2: 1: 0:	3:	0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x24	PhyAccCtl_H	7: RdReq 6: WrReq 5: 4:	R/W R/W	0: Normal 0: Normal 0: 0:	1: PHY Reg Rd Request 1: PHY Reg Wr Request 1: 1:	0x00	0x00	–
		3: ReqAdd[3] 2: ReqAdd[2] 1: ReqAdd[1] 0: ReqAdd[0]	R/W	PHY Register Read/Write Request Address				
0x25	PhyAccCtl_L	7: WrDat[7] 6: WrDAt[6] 5: WrDat[5] 4: WrDat[4] 3: WrDat[3] 2: WrDat[2] 1: WrDat[1] 0: WrDat[0]	R/W	PHY Register Write Data		0x00	0x00	–
0x26	PhyRdstat_H	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: RdAdd[3] 2: RdAdd[2] 1: RdAdd[1] 0: RdAdd[0]	R	PHY Register Read Address				
0x27	PhyRdstat_L	7: RdDat[7] 6: RdDat[6] 5: RdDat[5] 4: RdDat[4] 3: RdDat[3] 2: RdDat[2] 1: RdDat[1] 0: RdDat[0]	R	PHY Register Read Data		0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x28	ChnlIndex	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: Channel Index[3] 2: Channel Index[2] 1: Channel Index[1] 0: Channel Index[0]	R/W	ISO (Async Stream) Channel Index				
0x29	ChnlWindow	7: Channel Window[7] 6: Channel Window[6] 5: Channel Window[5] 4: Channel Window[4] 3: Channel Window[3] 2: Channel Window[2] 1: Channel Window[1] 0: Channel Window[0]	R/W	ISO (Async Stream) Cahnnel Window		0x00	0x00	–
0x2A	CmprIndex	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: Compare Index[3] 2: Compare Index[2] 1: Compare Index[1] 0: Compare Index[0]	R/W	Compare Address Index				
0x2B	CmprWindow	7: Compare Window[7] 6: Compare Window[6] 5: Compare Window[5] 4: Compare Window[4] 3: Compare Window[3] 2: Compare Window[2] 1: Compare Window[1] 0: Compare Window[0]	R/W	Compare Address Window		0x00	0x00	–
0x2C	CYCLE_TIME_H	7: Cycle Second[6] 6: Cycle Second[5] 5: Cycle Second[4] 4: Cycle Second[3] 3: Cycle Second[2] 2: Cycle Second[1] 1: Cycle Second[0]	R/W	CYCLE_TIME.second_count		0x00	–	–
		0: Cycle Count[12]	R/W	CYCLE_TIME.cycle_count				
0x2D	CYCLE_TIME_MH	7: Cycle Count[11] 6: Cycle Count[10] 5: Cycle Count[9] 4: Cycle Count[8] 3: Cycle Count[7] 2: Cycle Count[6] 1: Cycle Count[5] 0: Cycle Count[4]				0x00	–	–
0x2E	CYCLE_TIME_ML	7: Cycle Count[3] 6: Cycle Count[2] 5: Cycle Count[1] 4: Cycle Count[0]				0x00	–	–
		3: Cycle Offset[11] 2: Cycle Offset[10] 1: Cycle Offset[9] 0: Cycle Offset[8]	R/W	CYCLE_TIME.cycle_offset				
0x2F	CYCLE_TIME_L	7: Cycle Offset[7] 6: Cycle Offset[6] 5: Cycle Offset[5] 4: Cycle Offset[4] 3: Cycle Offset[3] 2: Cycle Offset[2] 1: Cycle Offset[1] 0: Cycle Offset[0]				0x00	–	–

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x30	HwSBP2Ctl	7: PtNotPresent 6: HOSTtoDev 5: FromStream 4: LastPT 3: HwSBP2Rst 2: HwSBP2Rsum 1: HwSBP2Pause 0: HwSBP2Start	R/W R/W R/W R/W W W W W	0: Present 0: Host <– Device 0: From PageTable 0: None 0: None 0: None 0: None 0: None	1: Not Present 1: Host –> Device 1: FromStream 1: Ignore 1: Reset 1: Resume 1: Pause 1: Start	0x00	0x00	–
0x31	HwSBP2Stat	7: FwPause 6: ErrPause 5: NotQuadEnable 4: WaitPLReady 3: HwSBP2Exec 2: PTaskExec 1: StTaskExec 0: TranExec	R R R/W R R R R R	0: Not Firmware Pause 0: Not Error Pause 0: Disable 0: Not Ready 0: Stop 0: Stop 0: Stop 0: Stop	1: FirmWre Pause 1: Error Pause 1: Enable 1: Ready 1: Execute 1: Execute 1: Execute 1: Execute	0x00	0x00	–
0x32	HwSBP2IntStat	7: SplitTimeOut 6: TxAckedIllegal 5: TxAckMiss 4: BrAbort 3: NotQuad 2: RxNotRespCmp 1: RxBroadCast 0: RxAckDataErr	R(W) R(W) R(W) R(W) R/W R(W) R(W) R(W)	0: None 0: None 0: None 0: None 0: None 0: None 0: None 0: None	1: SplitTimeOut 1: TxAckedIllegal 1: TxAsyMiss 1: BrAbort 1: NotQuad 1: RxNotRespCmp 1: RxBroadCast 1: RxAckDataErr	0x00	0x00	–
0x33	HwSBP2Index	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: HwSBP2 Index[3] 2: HwSBP2 Index[2] 1: HwSBP2 Index[1] 0: HwSBP2 Index[0]	R/W	HwSBP2 Index				
0x34	HwSBP2Window_H	7: HwSBP2 Window[15] 6: HwSBP2 Window[14] 5: HwSBP2 Window[13] 4: HwSBP2 Window[12] 3: HwSBP2 Window[11] 2: HwSBP2 Window[10] 1: HwSBP2 Window[9] 0: HwSBP2 Window[8]	R/W	HwSBP2 Window		0x00	0x00	–
0x35	HwSBP2Window_L	7: HwSBP2 Window[7] 6: HwSBP2 Window[6] 5: HwSBP2 Window[5] 4: HwSBP2 Window[4] 3: HwSBP2 Window[3] 2: HwSBP2 Window[2] 1: HwSBP2 Window[1] 0: HwSBP2 Window[0]				0x00	0x00	–

0x36	PayloadSize_H	7: Payload Size[15]
		6: Payload Size[14]
		5: Payload Size[13]
		4: Payload Size[12]
		3: Payload Size[11]
		2: Payload Size[10]
		1: Payload Size[9]
		0: Payload Size[8]
			R/W	Set Payload Size (Bytes)
				If (HwSBP2Ctl.HwSBP2Exec ==0) {
				Write is valid.
				} else {
				Write is invalid.
				}
						0x00	0x00	–

0x37	PayloadSize_L	7: Payload Size[7] 6: Payload Size[6] 5: Payload Size[5] 4: Payload Size[4] 3: Payload Size[3] 2: Payload Size[2] 1: Payload Size[1] 0: Payload Size[0]				0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst

0x38	PageTableSize_H	7: Page Table Size[15]
		6: Page Table Size[14]
		5: Page Table Size[13]
		4: Page Table Size[12]
		3: Page Table Size[11]
		2: Page Table Size[10]
		1: Page Table Size[9]
		0: Page Table Size[8]
			R/W	If (HwSBP2Ctl.PtNotPresent == 0) {
				Write:Set PageElement *8 (bytes)
				Read :Indicate Page Table Size
				} else {
				Write:Set Data Length (bytes)
				Read :Indicate Create PageElement *8 (bytes)
				}
					0x00	0x00	–

0x39	PageTableSize_L	7: Page Table Size[7] 6: Page Table Size[6] 5: Page Table Size[5] 4: Page Table Size[4] 3: Page Table Size[3] 2: Page Table Size[2] 1: Page Table Size[1] 0: Page Table Size[0]			0x00	0x00	–
0x3A	PageTableAdrs0	7: PtAdress[47] 6: PtAdress[46] 5: PtAdress[45] 4: PtAdress[44] 3: PtAdress[43] 2: PtAdress[42] 1: PtAdress[41] 0: PtAdress[40]	R/W	Write: Set PageTable Offset Address Read: Indicate NextPageTable Offset Address	0x00	0x00	–
0x3B	PageTableAdrs1	7: PtAdress[39] 6: PtAdress[38] 5: PtAdress[37] 4: PtAdress[36] 3: PtAdress[35] 2: PtAdress[34] 1: PtAdress[33] 0: PtAdress[32]			0x00	0x00	–
0x3C	PageTableAdrs2	7: PtAdress[31] 6: PtAdress[30] 5: PtAdress[29] 4: PtAdress[28] 3: PtAdress[27] 2: PtAdress[26] 1: PtAdress[25] 0: PtAdress[24]			0x00	0x00	–
0x3D	PaqeTableAdrs3	7: PtAdress[23] 6: PtAdress[22] 5: PtAdress[21] 4: PtAdress[20] 3: PtAdress[19] 2: PtAdress[18] 1: PtAdress[17] 0: PtAdress[16]			0x00	0x00	–
0x3E	PageTableAdrs4	7: PtAdress[15] 6: PtAdress[14] 5: PtAdress[13] 4: PtAdress[12] 3: PtAdress[11] 2: PtAdress[10] 1: PtAdress[9] 0: PtAdress[8]			0x00	0x00	–
0x3F	PageTableAdrs5	7: PtAdress[7] 6: PtAdress[6] 5: PtAdress[5] 4: PtAdress[4] 3: PtAdress[3] 2: PtAdress[2] 1: PtAdress[1] 0: PtAdress[0]			0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x40	LinkRxHdrPtr_H	7: 6:		Write is ignore Read is always zero	0x00	0x00	–
		5: 4: LRHP[12] 3: LRHP[11] 2: LRHP[10] 1: LRHP[9] 0: LRHP[8]	R/W	Current Received Packet Header Area Pointer			
0x41	LinkRxHdrPtr_L	7: LRHP[7] 6: LRHP[6] 5: LRHP[5]			0x00	0x00	–
		4: 3: 2: 1: 0:		Write is ignore Read is always zero			
0x42	LinkRxORBPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: POP[12] 3: POP[11] 2: POP[10] 1: POP[9] 0: POP[8]	R/W	Current Received Packet ORB Data Area Pointer			
0x43	LinkRxORBPtr_L	7: POP[7] 6: POP[6] 5: POP[5] 4: POP[4] 3: POP[3] 2: POP[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			
0x44	LinkRxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: PSP[12] 3: PSP[11] 2: PSP[10] 1: PSP[9] 0: PSP[8]	R/W	Current Received Packet Stream Data Area Pointer			
0x45	LinkRxStreamPtr_L	7: PSP[7] 6: PSP[6] 5: PSP[5] 4: PSP[4] 3: PSP[3] 2: PSP[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			
0x46	LinkTxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	
		4: PTDP[12] 3: PTDP[11] 2: PTDP[10] 1: PTDP[9] 0: PTDP[8]	R	Current Transmit Packet Data Area Pointer			
0x47	LinkTxStreamPtr_L	7: PTDP[7] 6: PTDP[6] 5: PTDP[5] 4: PTDP[4] 3: PTDP[3] 2: PTDP[2]			0x00	0x00	
		1: 0:		Write is ignore Read is always zero			

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x48	UsedRxHdrPtr_H	7: 6: 5:		Write is ignore Read always zero	0x00	0x00	–
		4: URHP[12] 3: URHP[11] 2: URHP[10] 1: URHP[9] 0: URHP[8]	R/W	Received Packet Header Area Used Pointer			
0x49	UsedRxHdrPtr_L	7: URHP[7] 6: URHP[6] 5: URHP[5]					
		4: 3: 2: 1: 0:		Write is ignore Read is always zero	0x00	0x00	–
0x4A	UsedRxORBPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: UOP[12] 3: UOP[11] 2: UOP[10] 1: UOP[9] 0: UOP[8]	R/W	Received Packet ORB Data Area Used Pointer			
0x4B	UsedRxORBPtr_L	7: UOP[7] 6: UOP[6] 5: UOP[5] 4: UOP[4] 3: UOP[3] 2: UOP[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			
0x4C	IDE_RxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: IRSP[12] 3: IRSP[11] 2: IRSP[10] 1: IRSP[9] 0: IRSP[8]	R/W	Received Packet Stream Data Area IDE Pointer			
0x4D	IDE_RxStreamPtr_L	7: IRSP[7] 6: IRSP[6] 5: IRSP[5] 4: IRSP[4] 3: IRSP[3] 2: IRSP[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			
0x4E	IDE_TxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: ITSP[12] 3: ITSP[11] 2: ITSP[10] 1: ITSP[9] 0: ITSP[8]	R/W	Transmit Packet Stream Data Area IDE Pointer			
0x4F	IDE_TxStreamPtr_L	7: ITSP[7] 6: ITSP[6] 5: ITSP[5] 4: ITSP[4] 3: ITSP[3] 2: ITSP[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x50	BufControl	7: TxStreamClr	W	0: None Affect	1: Tx Stream Data Clear	0x00	0x00	–
		6: RxStreamClr	W	0: None Affect	1: Rx Stream Data Clear			
		5: RxORBClr	W	0: None Affect	1: Rx ORB Dat Clear			
		4: RxHdrClr	W	0: None Affect	1: Rx Header Clear			
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0: UpdLinkTxStrm	W	0: None Affect	1: Update Link Tx Stream Ptr			
0x51	BufMonitor	7: RxPayldRdy	R	0: Rx Payld Capa not Ready	1: Rx Payload Capa Ready	0x00	0x00	–
		6: TxPayldRdy	R	0: Tx Payld Capa not Ready	1: Tx Payload Capa Ready			
		5:		0:	1:			
		4: TxStreamFull	R	0: Not Full	1: Full			
		3: RxHdrRemain	R	0: Rx Header Area Empty	1: Rx Header not Empty			
		2: RxORBFull	R	0: Rx ORB Area not Full	1: Rx ORB Data Area Full			
		1: RxStreamFull	R	0: Rx Stream Area not Full	1: Rx Stream Data Area Full			
		0: RxHdrFull	R	0: Rx Header Area not Full	1: Rx Header Area Full			
0x52	AsyDmaCtl	7: AsyChnlSel	R/W	0: AsyTxPktHdr0	1: AsyTxPktHdr1	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4: BlkWrAreaSel	R/W	0: Rx ORB Area	1: Rx Stream Area			
		3: AsyFIFOEpty	R	0: AsyFIFO Empty	1: Non Empty			
		2: AsyFIFOClr	W	0: Normal	1: AsyFIFO Clear			
		1: AsyTxMon	R	0: Async Tx Stop	1: Async Tx Run			
		0: AsyStart	W	0: normal	1: Async Start			
0x53	IsoDmaCtl	7: IsoChnlSel	R/W	0: IsoTxPktHdr0	1: IsoTxPktHdr1	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4: SelTxPtr	R/W	0: Async Tx Pointer Select	1: ISO Tx Pointer Select			
		3: IsoFIFOEpty	R	0: IsoFIFO Empty	1: Non Empty			
		2: IsoFIFOClr	W	0: Normal	1: IsoFIFO Clear			
		1: IsoTxMon	R	0: Iso Tx Stop	1: Iso Tx Run			
		0: IsoStart	W	0: normal	1: Start			
0x54	RxDmaCtl	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3: RxFIFOEpty	R	0: Rx FIFO Empty	1: Non Empty			
		2: RxFIFOClr	W	0: Normal	1: Rx FIFO Clear			
		1: RxMon	R	0: Rx Stop	1: Rx Run			
		0: ForceBusy	R/W	0: Normal	1: Busy			
0x55	AreaIndex	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3: MemMapIndex[3]	R/W	Memory Map Area Index				
		2: MemMapIndex[2]						
		1: MemMapIndex[1]						
		0: MemMapIndex[0]						
0x56	AreaWindow_H	7: MemMapWindow[15]	R/W	Memory Map Area Window		0x00	0x00	–
		6: MemMapWindow[14]						
		5: MemMapWindow[13]						
		4: MemMapWindow[12]						
		3: MemMapWindow[11]						
		2: MemMapWindow[10]						
		1: MemMapWindow[9]						
		0: MemMapWindow[8]						
0x57	AreaWindow_L	7: MemMapWindow[7]				0x00	0x00	–
		6: MemMapWindow[6]						
		5: MemMapWindow[5]						
		4: MemMapWindow[4]						
		3: MemMapWindow[3]						
		2: MemMapWindow[2]						
		1: MemMapWindow[1]						
		0: MemMapWindow[0]						

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x58	BRstHdrPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: BusResetPtr[12] 3: BusResetPtr[11] 2: BusResetPtr[10] 1: BusResetPtr[9] 0: BusResetPtr[8]	R	Bus Reset Header Area Pointer This register indicates Address in Rx Header Area when BusRest detected.			
0x59	BRstHdrPtr_L	7: BusResetPtr[7] 6: BusResetPtr[6] 5: BusResetPtr[5]			0x00	0x00	–
		4: 3: 2: 1: 0:		Write is ignore Read is always zero			
0x5A	BRstORBPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: BusRstORBPtr[12] 3: BusRstORBPtr[11] 2: BusRstORBPtr[10] 1: BusRstORBPtr[9] 0: BusRstORBPtr[8]	R	Bus Reset ORB-Data Area Pointer This register indicates Address in Rx ORB Data Area when BusRest detected.			
0x5B	BRstORBPtr_L	7: BusRstORBPtr[7] 6: BusRstORBPtr[6] 5: BusRstORBPtr[5] 4: BusRstORBPtr[4] 3: BusRstORBPtr[3] 2: BusRstORBPtr[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			
0x5C	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x5D	(Reserved)	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0:	1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x5E	MaintCtl_H	7: E_Hcrc 6: E_Dcrc 5: No_Pkt 4: F_Ack 3: N_ack	R/W R/W R/W R/W R/W	0: 0: 0: 0: 0:	1: Add Header CRC Error 1: Add Data CRC Error 1: No Transmit Next Packet 1: Tx Optional AckCode 1: No Transmit AckPacket	0x00	0x00	–
		2: 1: 0:		0: 0: 0:	1: 1: 1:			
0x5F	MaintCtl_L	7: Ack[7] 6: Ack[6] 5: Ack[5] 4: Ack[4] 3: Ack[3] 2: Ack[2] 1: Ack[1] 0: Ack[0]	R/W	Optional AckCode		0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x60	IDE_Config0	7: UltraDmaMode 6: DmaMode 5: ActPort 4: IDE_Slave 3: DMARQ_Level 2: Swap	R/W	0: DMA Mode 0: PIO Mode 0: None 0: Master 0: Positive Logic 0: Nomal	1: Ultra DMA Mode 1: DMA Mode 1: Active 1: Slave 1: Negative Logic 1: Swap IDE Port Hi & Lo	0x00	0x00	–
		1: 0:		0: 0:	1: 1:			
0x61	IDE_Config1	7: IDE_Reset	R/W	0: None	1: IDE Reset	0x00	0x00	–
		6: 5: 4: 3: 2: XDIOW_DLYen 1: 0:	R/W	0: 0: 0: 0: 0: None 0: 0:	1: 1: 1: 1: 1: Delay XDIOW 1: 1:			
0x62	IDE_RegAccCyc	7: Assert Pulse[3] 6: Assert Pulse[2] 5: Assert Pulse[1] 4: Assert Pulse[0]	R/W	IDE Register Access Strobe Signal Assert Pulse Width Minimum Value		0x00	0x00	–
		3: Negate Pulse[3] 2: Negate Pulse[2] 1: Negate Pulse[1] 0: Negate Pulse[0]	R/W	IDE Register Access Strobe Signal Negate Pulse Width Minimum Value				
0x63	IDE_PioDmaCyc	7: Assert Pulse[3] 6: Assert Pulse[2] 5: Assert Pulse[1] 4: Assert Pulse[0]	R/W	IDE Transfer Mode Strobe Signal Assert Pulse Width Minimum Value		0x00	0x00	–
		3: Negate Pulse[3] 2: Negate Pulse[2] 1: Negate Pulse[1] 0: Negate Pulse[0]	R/W	IDE Transfer Mode Strobe Signal Negate Pulse Width Minimum Value				
0x64	IDE_UltraDmaCyc	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: Cycle Time[3] 2: Cycle Time[2] 1: Cycle Time[1] 0: Cycle Time[0]	R/W	IDE Ultra DMA Transfer Mode Strobe Signal Minimum Cycle Time				
0x65	IDE_DmaCtl	7: 6: 5: IncFIFOCnt	 W	0: 0: 0: None	1: 1: 1: Push FIFO Data	0x00	0x00	–
		4: CRC_Clear 3: FIFO_Clear 2: IDE_Abort 1: IDE_Direction 0: DmaStart	W W W R/W W	0: None 0: None 0: None 0: SRAM –> IDE 0: None	1: CRC Clear 1: FIFO Clear 1: IDE Transfer Abort 1: IDE –> SRAM 1: IDE DMA Start			
0x66	IDE_BusStat	7: DMARQ 6: DMACK 5: INTRQ 4: IORDY 3: 2: 1: DIAG 0: DASP	R	Indicate IDE I/F Signals State		0x00	0x00	–
0x67	IDE_DmaStat	7: FIFOCnt[2] 6: FIFOCnt[1] 5: FIFOCnt[0]	R R R	Indicate word count in FIFO		0x00	0x00	–
		4: 3: 2:		0: 0: 0:	1: 1: 1:			
		1: DmaPause 0: DmaRun	R W	0: IDE DMA not Pause 0: Not DMA	1: IDE DMA Pause 1: IDE DMA Running			

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x68	IDE_ByteCount0	7: ByteCount[31] 6: ByteCount[30] 5: ByteCount[29] 4: ByteCount[28] 3: ByteCount[27] 2: ByteCount[26] 1: ByteCount[25] 0: ByteCount[24]	R/W	IDE Data Transfer Byte Count Register Read: Indicate Remain Byte Count Write: Set Total Transfer Byte Count	0x00	0x00	–
0x69	IDE_ByteCount1	7: ByteCount[23] 6: ByteCount[22] 5: ByteCount[21] 4: ByteCount[20] 3: ByteCount[19] 2: ByteCount[18] 1: ByteCount[17] 0: ByteCount[16]			0x00	0x00	–
0x6A	IDE_ByteCount2	7: ByteCount[15] 6: ByteCount[14] 5: ByteCount[13] 4: ByteCount[12] 3: ByteCount[11] 2: ByteCount[10] 1: ByteCount[9] 0: ByteCount[8]			0x00	0x00	–
0x6B	IDE_ByteCount3	7: ByteCount[7] 6: ByteCount[6] 5: ByteCount[5] 4: ByteCount[4] 3: ByteCount[3] 2: ByteCount[2] 1: ByteCount[1] 0: ByteCount[0]			0x00	0x00	–
0x6C	IDE_CRC0	7: CRC[15] 6: CRC[14] 5: CRC[13] 4: CRC[12] 3: CRC[11] 2: CRC[10] 1: CRC[9] 0: CRC[8]	R	IDE CRC Data Register	0x00	0x00	–
0x6D	IDE_CRC1	7: CRC[7] 6: CRC[6] 5: CRC[5] 4: CRC[4] 3: CRC[3] 2: CRC[2] 1: CRC[1] 0: CRC[0]			0x00	0x00	–
0x6E	IDE_TestIndex	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0: / 1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–
0x6F	IDE_TestWindow	7: 6: 5: 4: 3: 2: 1: 0:		0: 0: 0: 0: 0: 0: 0: 0: / 1: 1: 1: 1: 1: 1: 1: 1:	0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x70	IDE_CS00	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Data Register	0x00	0x00	–
0x71	IDE_CS01	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Read : Error Register Write: Features Register	0x00	0x00	–
0x72	IDE_CS02	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Sector Count Register	0x00	0x00	–
0x73	IDE_CS03	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Sector Number Register or Logical Block Address(LBA) bit 0 – 7	0x00	0x00	–
0x74	IDE_CS04	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Cylinder Low Register or Logical Block Address(LBA) bit 8 – 15	0x00	0x00	–
0x75	IDE_CS05	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Cylinder High Register or Logical Block Address(LBA) bit 16 – 23	0x00	0x00	–
0x76	IDE_CS06	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Device/Head Register 0x00 Logical Block Address(LBA) bit 24 – 27	0x00	0x00	–
0x77	IDE_CS07	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Read : Status Register 0x00 Write: Command Register	0x00	0x00	–

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x78	IDE_CS10	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x79	IDE_CS11	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7A	IDE_CS12	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7B	IDE_CS13	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7C	IDE_CS14	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7D	IDE_CS15	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7E	IDE_CS16	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Alternate Status Write: Device Control	0x00	0x00	–
0x7F	IDE_CS17	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : (obsolete) Write: Not Used	0x00	0x00	–

8.1.4 Detail Description of Register

(The base address of this register is 0x100000.)

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x00	MainIntStat	7:SubIntStat	R(W)	0: None	1: Sub Interrupt Occurred	0x00	0x00	–
		6: TxIsoCmp	R(W)	0: None	1: ISO Pkt Transmit Done			
		5: RxDmaCmp	R(W)	0: None	1: Packet Reception			
		4: TxAsyCmp	R(W)	0: None	1: AckCode Reception			
		3: HwSBP2Cmp	R(W)	0: None	1: HwSBP2 Process Complete			
		2: IDE_DmaCmp	R(W)	0: None	1: IDE DMA Transmit Complete			
		1: IDE_INTRQ	R(W)	0: None	1: IDE Interface Interrupt			
		0: BusReset	R(W)	0: None	1: Bas Reset Detected			

Main Interrupt Status Register

When this IC interrupts the CPU, the CPU first reads this register to handle it, indicating which Interrupt Status Register is a factor of this interrupt.

Subsequent to reading this register, the SubIntStat (Bit 7) reads an Interrupt Status Register associated with each bit to confirm which bit is an interrupt source and appropriately handle it. After that, it writes the read value to the Interrupt Status Register to clear the bit. In the case the interrupt factor still remains, however, the bit is not cleared.

When one of 7 bits of the TxIsoCmp, RxDmaCmp, TxAsyCmp, HwSBP2Cmp, IDE_DmaCmp, IDE_INTRQ, and BusReset other than above is an interrupt source, this register clears the bit by writing the read value.

Note) The bits of this register control the XInt of output pin. Writing to this register negates the XInt once even if the interrupt factor remains, asserting the XInt after a certain period. (Ready for a timer or edge interrupt).

Bit7 Sub Interrupt Status

When an interrupt factor exists at each bit shown at the SubIntStat Register, this bit becomes “1”.

Bit 6 Isochronous Packet Transmit Complete

When an ISO Packet Transmit is complete, this bit becomes “1”.

Bit5 Receive Packet DMA Complete

When a received packet is written to the Receive Buffer Area, this bit becomes “1”.

Bit4 Asynchronous Packet Transmit Complete

When an Ack packet to an Async Transmit packet is received, this bit becomes “1”.

The Ack code is written to the footer area of the Transmit Packet Header.

Bit 3 HwSBP2 Process Complete

When a HwSBP2 processing is complete, this bit becomes “1”.

Bit2 IDE DMA Transmit Complete

When an IDE I/F DMA Transmit is complete, this bit becomes “1”.

Bit1 IDE Interface Interrupt

When the INTRQ signal is asserted to the IDE I/F, this bit becomes “1”.

Bit0 BusReset Detected

When a BusReset signal is detected on the 1394 Serial Bus, this bit becomes “1”.

When it issues a BusReset, this bit becomes “1” as well.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x01	SubIntStat	7: SelfIDdone	R(W)	0: None	1: Self-ID Phase Done			
		6: SelfIDerr	R(W)	0: None	1: Self-ID Packet Error			
		5: HwSBP2Err	R(W)	0: None	1: Hw SBP2 Error			
		4: HwSBP2BRst	R(W)	0: None	1: BusReset in process HwSBP	0x00	0x00	–
		3: LinkIntStat1	R(W)	0: None	1: Link1 Interrupt Occurred			
		2: LinkIntStat0	R(W)	0: None	1: Link0 Interrupt Occurred			
		1: PhyIntStat	R(W)	0: None	1: PHY Interrupt Occurred			
		0: DmaIntStat	R(W)	0: None	1: Dma Interrupt Occurred			

Sub-Interrupt Status Register

The value of each bit of this register indicates the status of a corresponding interrupt source. If these bits become "1" when the associated bit of the SubIntEnb Register is "1", this register asserts an interrupt signal to the CPU. The CPU reads this register after receiving the interrupt signal to locate an interrupt source. By writing the read value again, it clears these bits.

Subsequent to reading this register, the lower order 4 bits reads the Interrupt Status Register associated with each bit to confirm which bit is an interrupt source and appropriately handle it. After that, it writes the read value to the Interrupt Status Register to clear the bit. In the case that the interrupt factor still remains, however, the bit is not cleared.

Bit7 Self Identify Period Complete

When a Self ID period finishes, this bit becomes "1".

Bit6 Self Identify Packet Error

When a Self-ID packet with an error is received during the Self-ID period or when the Self-ID period finishes due to an error, this bit becomes "1".

Bit5 HwSBP2Err

When an interrupt factor from the HwSBP2 indicated on the HwSBP2IntStat Register exists, this bit becomes "1".

Bit4 BusReset in process HwSBP2

When a BusReset occurs in the HwSBP2 processing, this bit becomes "1".

Bit3 LINK Core Interrupt Status1

When an interrupt factor from the LINK core indicated on the LinkIntStat1 Register exists, this bit becomes "1".

Bit2 LINK Core Interrupt Status0

When an interrupt factor from the LINK core indicated on the LinkIntStat0 Register exists, this bit becomes "1".

Bit1 PHY/LINK Interrupt Status

When an interrupt factor from the PHY status indicated on the PHYIntStat Register exists, this bit becomes "1".

Bit0 LINK DMA Interrupt Status

When an interrupt factor exists in the internal DMA operation indicated on the DmaIntStat Register, this bit becomes "1".

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x02	(Reserved)	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0:		0:	1:			

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x03	DmaIntStat	7:		0:	1:			
		6: TxAsyRtyGo	R(W)	0: None	1: Async Tx Retry Go			
		5: TxAsyBCSent	R(W)	0: None	1: AsyncTxBroadcast Sent			
		4: RxDmaFaild	R(W)	0: None	1: Rx DMA Failed	0x00	0x00	–
		3: TxAsyFaild	R(W)	0: None	1: Async Tx Failed			
		2: TxIsoFaild	R(W)	0: None	1: ISO Tx Failed			
		1: TxAsyBRAbort	R(W)	0: None	1: Async Tx BusReset Abort			
		0: TxAsyMiss	R(W)	0: None	1: AsyncTxAckCodeMissing			

DMA Interrupt Status Register

The value of each bit of this register indicates the status of a corresponding interrupt source. If these bits become "H" when the associated bit of the DMAIntEnb Register is "1", this register asserts the interrupt signal to the CPU.

The CPU reads this register after receiving the interrupt signal to locate an interrupt source. By writing the read value again, it clears these bits.

Bit7 Reserved

When a Sub Action Gap is detected in PHY status of PHY/LINK interface, this bit becomes "1".

Bit6 Transmit Async Packet Retry Go

When an auto retry is performed after transmitting an Async packet and receiving an Ack_busy, this bit becomes "1".

Bit5 Transmit Async Broadcast Packet Sent

After a transmission of a Broadcast packet of Async or a PHY packet finishes, this bit becomes "1".

Bit4 Receive Packet LINK DMA Failed

When a received packet cannot be written to the buffer due to the following reasons, this bit becomes "1".

1) DMA was too late.
2) A packet was received when the ForceBusy bit is on.

Bit3 Transmit Async Packet LINKDMA Failed

When data cannot be transferred from the buffer to the LINK core at the time of Async packet transmission (DMA FIFO is Under Flow), this bit becomes "1".

Bit2 Transmit ISO Packet LINKDMA Failed

When data cannot be transferred from the buffer to the LINK core at the time of ISO packet transmission (DMA FIFO is Under Flow), this bit becomes "1".

Bit 1 Transmit Async Packet BusReset Abort

When a Transmit packet is disabled by a BusReset before an Ack packet is returned at the time of Async packet transmission, this bit becomes "1".

Bit0 Transmit Async Packet Ack-code Missing

When a Ack packet is not returned at the time of Async packet transmission, this bit becomes "1".

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x04	LinkIntStat1	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3: RxOnTardy	R(W)	0: None	1: Ack_tardy Sent			
		2: RxHcrcErr	R(W)	0: None	1: Rx Packet Header CRC Err			
		1: RxUnkTcode	R(W)	0: None	1: Rx Packet Tcode Unknown			
		0: TxRtyExced	R(W)	0: None	1: Tx Retry Exceeded			

LINK Core Interrupt Status Register 1

The value of each bit of this register indicates the status of a corresponding interrupt source. If these bits become "1" when the associated bit of the LINKIntEnb1 Register is "1", this register asserts the interrupt signal to the CPU.

The CPU reads this register after receiving the interrupt signal to locate an interrupt source. By writing the read value again, it clears these bits.

Bit7 Reserved

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 RxOnTardy

When a packet is received when the ChipCtl. SendTardy bit is "1", an Ack_tardy is returned to the party of the other end and this bit becomes "1".

Bit2 Receive Packet Header CRC Error

When an error exists in the header CRC of a received packet, this bit becomes "1".

Bit1 Receive Packet Tcode Unknown

When the Tcode in a received packet is invalid, this bit becomes "1".

Bit0 transmit Retry Exceeded

If a transmit retry fails since the set value of the MaxRetry Register is exceeded when the RetryLimit Register is not zero or the MaxRetry Register is not 0 and this bit becomes "1".

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x05	LinkIntStat0	7: UnExpCh	R(W)	0: None	1: Unknown Expected Channel			
		6: DupliCh	R(W)	0: None	1: DuplicateChannelDetected			
		5: IsoArbFaild	R(W)	0: None	1: Iso Arbtration Failed			
		4: CycTooLong	R(W)	0: None	1: ISO Arbitration Failed	0x00	0x00	–
		3: CycOverFlw	R(W)	0: None	1: Cycle Timer Over Fullow			
		2: CycEvent	R(W)	0: None	1: Local Cycle Event Occured			
		1: CycLost	R(W)	0: None	1: Cycle Start Packet Lost			
		0: CycArbFail	R(W)	0: None	1: CycleStartPkt Arbtration Fail			

LINK Core Interrupt Status Register 0

The value of each bit of this register indicates the status of a corresponding interrupt source. If these bits become "1" when the associated bit of the LINKIntEnb0 Register is "1", this register asserts the interrupt signal to the CPU.

The CPU reads this register after receiving the interrupt signal to locate an interrupt source. By writing the read value again, it clears these bits.

Bit7 Unknown Expected Channel

When a packet of ISO channel not set in the CHANNEL_AVAILABLE Register is detected, this bit becomes "1".

It is enabled when the WonIRM = "1" of IRM IDStat Register (the self node is IRM).

Bit6 DuplicateChannelDetected

When a packet of a same channel is detected in the ISO period of 1 cycle, this bit becomes "1".

It is enabled when the WonIRM = "1" of IRM IDStat Register (the self node is IRM).

Bit5 ISO Arbitration Failed

When an ISO packet transmit request is received but a SubAction Gap is detected before it is transmitted, this bit becomes "1".

Bit4 ISO Arbitration Failed

When a Cycle_START packet is received but a SubAction Gap cannot be detected even after the ISOCHRONOUS_CYCLE_TIME has passed, this bit becomes "1".

Bit3 Cycle Timer Over Flow

When the CYCLE_TIMER overflows, this bit becomes "1".

Bit2 Local Cycle Event Occurred

When an local cycle event occurs, this bit becomes "1".

Bit1 Cycle Start Packet Lost

When the CYCLE_START_PACKET does not exist over two local cycle events, this bit becomes "1".

Bit0 CycleStartPkt Arbitration Failed

When a CYCLE_START_PACKET cannot be transmitted before the SubActionGap after a local cycle event occurs, this bit becomes "1". This bit is enabled when cmstr = "1".

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x06	PhyIntStat	7: SubGap	R(W)	0: None	1: Sub Action Gap Detected			
		6: ArbGap	R(W)	0: None	1: ArbtrationResetGapDetected			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2: Phy_int	R(W)	0: None	1: PHY Interrupt Detected			
		1: PhyWrDone	R(W)	0: None	1: PHY Register Write Done			
		0: PhyRdDone	R(W)	0: None	1: PHY Register Read Done			

PHY Interrupt Status Register

The value of each bit of this register indicates the status of a corresponding interrupt source. If these bits become "1" when the associated bit of the PHYIntEnb Register is "1", this register asserts the interrupt signal to the CPU. The CPU reads this register after receiving the interrupt signal to locate an interrupt source. By writing the read value again, it clears these bits.

Bit 7 Sub Action Gap Detected

When a Transmit Action Gap is detected in the PHY status of the PHY/LINK interface, this bit becomes "1".

Bit6 Arbitration Reset Gap Detected

When an Arbitration Reset Gap is detected in the PHY status of the PHY/LINK interface, this bit becomes "1".

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 PHY/LINK Interface Interrupt Detected

When a PHY_Interrupt is detected in the PHY status of the PHY/LINK interface, this bit becomes "1". This status indicates the PHY is put under one of the following.

1) In most instances, a loop is created in the cable topology.
2) Cable power is insufficient.
3) A bias change is detected.

Bit1 PHY Register Write Done

When the write access of the PHY Register is complete, this bit becomes "1".

Bit0 PHY Register Read Done

When read data is stored in the PHYRdStat Register at the time of read access of the PHY Register, this bit becomes "1".

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x07	(Reserved)	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0:		0:	1:			

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x08	MainIntEnb	7: EnSubIntStat	R/W	0: Disable	1: Enable			
		6: EnTxIsoCmp	R/W	0: Disable	1: Enable			
		5: EnRxDmaCmp	R/W	0: Disable	1: Enable			
		4: EnTxAsyCmp	R/W	0: Disable	1: Enable	0x00	0x00	–
		3: EnHwSBP2Cmp	R/W	0: Disable	1: Enable			
		2: EnIDE_DmaCmp	R/W	0: Disable	1: Enable			
		1: EnIDE_INTRQ	R/W	0: Disable	1: Enable			
		0: EnBusReset	R/W	0: Disable	1: Enable			

Main Interrupt Enable Flag Register

This register enables/disables an interrupt factor of the MainIntStat Register.
Setting the corresponding bit to “1” enables an interrupt to the CPU.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x09	SubIntEnb	7: EnSelfIDdone	R/W	0: Disable	1: Enable			
		6: EnSelfIDerr	R/W	0: Disable	1: Enable			
		5: EnHwSBP2Err	R/W	0: Disable	1: Enable			
		4: EnHwSBP2BRst	R/W	0: Disable	1: Enable	0x00	0x00	–
		3: EnLinkIntStat1	R/W	0: Disable	1: Enable			
		2: EnLinkIntStat0	R/W	0: Disable	1: Enable			
		1: EnPhyIntStat	R/W	0: Disable	1: Enable			
		0: EnDmaIntStat	R/W	0: Disable	1: Enable			

Sub-Interrupt Enable Flag Register

This register enables/disables an interrupt factor of the SubIntStat Register.
Setting the corresponding bit to “1” enables an interrupt to the CPU.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x0A	(Reserved)	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0:		0:	1:			

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x0B	DmaIntEnb	7:		0:	1:			
		6: EnTxAsyRtyGo	R/W	0: Disable	1: Enable			
		5: EnTxAsyBCSent	R/W	0: Disable	1: Enable			
		4: EnRxDmaFaild	R/W	0: Disable	1: Enable	0x00	0x00	–
		3: EnTxAsyFaild	R/W	0: Disable	1: Enable			
		2: EnTxIsoFaild	R/W	0: Disable	1: Enable			
		1: EnTxAsyBRAbort	R/W	0: Disable	1: Enable			
		0: EnTxAsyMiss	R/W	0: Disable	1: Enable			

DMA Interrupt Enable Flag Register

This register enables/disables an interrupt factor of the DMAIntStat Register.
Setting the corresponding bit to “1” enables an interrupt to the CPU.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x0C	LinkIntEnb1	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3: EnRxOnTardy	R/W	0: Disable	1: Enable			
		2: EnRxHcrcErr	R/W	0: Disable	1: Enable			
		1: EnRxUnkTcode	R/W	0: Disable	1: Enable			
		0: EnTxRtyExced	R/W	0: Disable	1: Enable			

LINK Core Interrupt Enable Flag Register 1

This register enables/disables an interrupt factor of the LINKIntStat1 Register.
Setting the corresponding bit to “1” enables an interrupt to the CPU.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x0D	LinkIntEnb0	7: EnUnExpCh	R/W	0: Disable	1: Enable			
		6: EnDupliCh	R/W	0: Disable	1: Enable			
		5: EnIsoArbFaild	R/W	0: Disable	1: Enable			
		4: EnCycTooLong	R/W	0: Disable	1: Enable	0x00	0x00	–
		3: EnCycOverFlw	R/W	0: Disable	1: Enable			
		2: EnCycEvent	R/W	0: Disable	1: Enable			
		1: EnCycLost	R/W	0: Disable	1: Enable			
		0: EnCycArbFail	R/W	0: Disable	1: Enable			

LINK Core Interrupt Enable Flag Register 0

This register enables/disables an interrupt factor of the LINKIntStat0 Register.
Setting the corresponding bit to “1” enables an interrupt to the CPU.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x0E	PhyIntEnb	7: EnSubGap	R/W	0: Disable	1: Enable			
		6: EnArbGap	R/W	0: Disable	1: Enable			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2: EnPhy_int	R/W	0: Disable	1: Enable			
		1: EnPhyWrDone	R/W	0: Disable	1: Enable			
		0: EnPhyRdDone	R/W	0: Disable	1: Enable			

PHY Core Interrupt Enable Flag Register

This register enables/disables an interrupt factor of the PHYIntStat Register.
Setting the corresponding bit to “1” enables an interrupt to the CPU.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x0F	(Reserved)	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0:		0:	1:			

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x10	ChipCtl	7: Suspend	R/W	0: Resume	1: Suspend			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3:		0:	1:			
		2: IDE_MdlRst	W	0: None	1: IDE_Module Reset			
		1: SendTardy	R/W	0: None	1: Send Ack_tardy			
		0: SoftReset	W	0: None	1: Reset Start			

Chip Control Register

The Chip Ctl Register controls the internal circuit of a chip.

Bit7 Suspend

Setting this bit to “1” stops the Sclk supplied from the PHY to this IC. At that time, the LPS signal must be negated as well.

When a LINKOn packet is received, the CPU asserts the xINT. After asserting it, the firmware asserts the LPS signal to the PHY and resume it by the Sclk supplied from the PHY. At that time, this bit must be set to “0”.

Bit6 Reserved

Bit5 Reserved

Bit4 Reserved

Bit3 Reserved

Bit2 IDE_MdlRst

Setting this bit to “1” resets IDE-related registers (0x60 - 0x7F) to restore them to the initial state.

Bit1 Send Ack_tardy Enable

Makes setting to return an Ack_tardy as a Ack code when receiving an Async packet.

0: Usual Ack code

1: ack_tardy

Bit0 Soft Reset

Setting this bit to “1” initializes the interiors of the circuit. After initializing it, it is restored to “0”.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x11	HW_Revision	7: HW_Revision[7] 6: HW_Revision[6] 5: HW_Revision[5] 4: HW_Revision[4] 3: HW_Revision[3] 2: HW_Revision[2] 1: HW_Revision[1] 0: HW_Revision[0]	R	Indicate Hard Ware Revison Number	0x03	0x03	0x03

Hardware Revision Register

The HW_Revision Register indicates the revision number of a chip.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x18	LinkCtl_H	7: PassSelfID	R/W	0: Non PassSelfID	1: Self–ID to DMA FIFO	0x00	0x00	–
		6: PassPhyPkt		0: Non Pass PHY Packet	1: PHY Pkt to DMA FIFO			
		5: PassBrPkt		0: Non Pass BusRst Packet	1: BusRst Pkt to DMA FIFO			
		4: EnPosWB		0: Disable Posted WB	1: Enable Posted WB			
		3: EnPosWQ		0: Disable Poosted WQ	1: Enable Posted WQ			
		2: APHY		0: PHY 1394.a uncorrespond	1: PHY 1394.a correspond			
		1: EnAcc		0: Ack Acceleration Disable	1: Ack Acceleration Enable			
		0: Cmstr		0: Cycle Master Not Capabl	1: Cycle Master Capable			

LINK Core Control Register Higher Rank

This register controls the functions of the LINK core.

Bit7 Pass Self-ID Packet

Setting this bit to “1” captures a Self-ID packet received by the LINK core into the buffer.

Bit6 Pass PHY Packet

When requesting the PHY Register for a register write, this bit is set to “1”. After the execution, this bit is cleared.

Bit5 Pass BusReset Packet

Setting this bit to “1” captures a BusReset packet received by the LINK core into the buffer.

Bit4 Enable Posted Block Write

Setting this bit to “1” enables the Posted Write function for a Block Write Request.

Bit3 Enable Posted Quadlet Write

Setting this bit to “1” enables the Posted Write function for a Quadlet Write Request.

Bit2 APHY

Indicates whether the PHY conforms to 1394.a or not.

1: Conforms to PHY 1394.a

0: Does not conform to PHY 1394.a

Bit1 Enable Ack Acceleration

Indicates the setting of Ack Acceleration.

1: Ack Acceleration enable

0: Ack Acceleration disable

Bit0 cmstr

When the self node is Cycle Master capable and a root, this bit becomes “1”.

If the self node does not become a root in the Self-ID processing when this bit is set after the Bus Reset, this bit is cleared.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x19	LinkCtl_L	7: EnLink	R/W	0: Disable Link	1: Enable Link		–	–
		6:		0:	1:		–	–
		5: PLIFrst	W	0: None	1: Reset PHY/Link I/F		0	–
		4: IgnrBChdr	R/W	0: BC Pkt to DMA FIFO	1: Ignore BC Packet	0x00	0	–
		3: IgnrBCdata	R/W	0: BC Data to DMA FIFO	1: Ignore BC – Data		0	–
		2: RxBusyMode	R/W	0: Dual	1: Single		0	–
		1: DualRtyEnb	R/W	0: Dual Retry Disable	1: Dual Retry Enable		0	–
		0: SinglRtyEnb	R/W	0: Single Retry Disable	1: Single Retry Enable		0	–

LINK Core Control Register Lower Rank

This register controls the functions of the LINK core.

Bit7 Enable LINK

Controls whether communications with other nodes are enabled.
When this bit is “0”, no response is given to a received packet. When it is “1”, the transmission/reception of a packet becomes possible. Even if you set the EnLINK to “1” when the LPS bit is “0”, it is ignored. Before setting it to “1”, set the LPS bit to “1” and wait 10ms.

Bit6 Reserved

Bit5 PHY/LINK Interface Reset

Writing “1” to this bit resets the PHY/LINK interface. After resetting it, this bit is automatically restored to “0”.

Bit4 Ignore Broadcast Packet

Setting this bit to “1” abandons a Broadcast packet received by the LINK core.

Bit3 Ignore Broadcast Packet Data

Setting this bit to “1” abandons a Broadcast data received by he LINK core.

Bit2 Rx Busy Mode

Sets a Busy type, the Dual Phase mode or Single Phase mode, for a received packet when returning a Busy. When this is “1”, an ack_busy_X is returned. When it is “0”, an ack_busy_A or ack_busy_B is returned.

Bit1 Dual Phase Retry Enable

Controls whether the Dual Phase retry protocol is enabled.
When this bit is “1”, a retry processing is done until a time set on the Retry Limit Register is exceeded. When it is “0”, no retry is done. When the value of the Retry Limit Register is “0”, a retry processing is ignored.

Bit0 Single Phase Retry Enable

Controls whether the Single Phase retry protocol is enabled.
When this bit is “1”, a retry processing is done until the number set on the Retry Limit Register is exceeded. When it is “0”, a retry processing is disabled. When the value of the MaxRetry Register is “0”, a retry processing is ignored.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x1A	LinkStart	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	–	–
		3:		0:	1:			
		2: ID_Valid	R	0: PhyID Invalid	1: PhyID Valid			
		1: Root	R	0: Self Node =Not Root	1: Self Node =Root			
		0: CablPwSts	R	0: Cable Power Status NG	1: Cable Power Status OK			

Link Core Status Read Register

Bit 7..3 Reserved

Bit2 ID_Valid

When this bit is set to “1,” the Physical_ID of the NodeID register becomes valid, and when this bit is set to “0,” the Physical_ID becomes invalid.

Bit1 Root

This bit is set to “1” when the self node comes to Root in the Self-ID process after the bus is reset.

Bit 0 Cable Power Status

This bit indicates the status of Cable Power, which is updated in the PHY Status.
“1” : Cable Power Status OK
“0” : Cable Power Status NG

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x1B	PriReqCnt	7: 6:		0: 0: 1:	0x00	0x00	0x00
		5: PriReq[5] 4: PriReq[4] 3: PriReq[3] 2: PriReq[2] 1: PriReq[1] 0: PriReq[0]	R/W	Maximum Number of certain Priority Arb Request			

Priority Request Count Register

This register shows registers in the pri-req field shown in the PRIORITY_BUDGET(CSR) register. This register can precede the Priority Request as often as it is set to PriReq in a uniform section. But this register can only be set by the node suitable for the bus manager.

Bit7..6 Reserved

Bit5..0 pri_req[9:0]

This bit is for setting the value of pri_req designated by the bus manager. Any value exceeding the value of pri_max to be packaged with the firmware cannot be set. The value is cleared to zero when a uniform section ends.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x1C	RetryLimit_H	7: SecLimit[2] 6: SecLimit[1] 5: SecLimit[0]	R/W	Dual Phase Retry Limit Second Limit	0x00	0x00	–
		4: CycLimt[12] 3: CycLimt[11] 2: CycLimt[10] 1: CycLimt[9] 0: CycLimt[8]					
0x1D	RetryLimit_L	7: CycLimt[7] 6: CycLimt[6] 5: CycLimt[5] 4: CycLimt[4] 3: CycLimt[3] 2: CycLimt[2] 1: CycLimt[1] 0: CycLimt[0]	R/W	Cycle Limit If (SecLimit == 0 and CycLimit==0) Dual Phase is ignore	0x00	0x00	–

Dual Retry Time Set Register (Higher Rank, Lower Rank)

This register is used for the Dual Phase Retry protocol to set a retransmit retry time limit when an Async Transmit packet is transmitted and a Busy is returned. When this register is “0”, the Dual Phase retry is ignored.

0x1C

Bit7..5 Second_Limit[2:0]

Set a Dual Phase Retry Time (Unit: second).

0x1C, 0x1D

Cycle Limit[12:0]

Sets a retry time at Cycle Limit [12:0] (Unit: 125µs).

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x1E	MaxRetry	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3: maxRty[3]	R/W	Single Phase Retry Limit				
		2: maxRty[2]		Max Retry Count Value				
		1: maxRty[1]		If maxRty == 0, Single Phase Retry is ignore				
		0: maxRty[0]						

Single Retry Limit Set Register

This register sets the number of retries of the Single Phase Retry protocol.
When its value is “0”, the Single Phase Retry is ignored.

Bit7..4 Reserved

Bit3..0 Single Retry Limit[3:0]

Sets the number of retries in the Single Phase at maxRtry[3:0]

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x1F	IRM_Stat	7: NoIRM	R	0: Exist IRM Node	1: None IRM Node	0x3F	–	0x3F
		6: WonIRM	R(W)	0: Other Node	1: Self Node			
		5: IRMID[5]	R	Physical ID of IRM Node No exist IRM Node then IRMID=0x3F				
		4: IRMID[4]						
		3: IRMID[3]						
		2: IRMID[2]						
		1: IRMID[1]						
		0: IRMID[0]						

IRM Status Register

This IRM Status Register controls detection of the Isochronous Resource Manager.

Bit7 No IRM

Sets whether an Isochronous Resource Manager exists on the serial bus. “1” indicates the IRM node does not exist and “0” indicates the IRM node exists.

Bit6 WonIRM

Sets whether the Isochronous Resource Manager is self node or other node.
“1” indicates it is the self node and “0” indicates it is other node.
Usually, this bit is read-only. When a valid IRM is not detectable due to hardware bugs, however, the firmware sets this bit through a Self-ID packet or topology map.

Bit5..0 IRM ID[5:0]

When the EnLrmDetect bit is “1”, the node ID of the Isochronous Resource Manager detected in the Self-ID period is set. When no node corresponding to the IRM exists, it indicates the 0x3F value.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x20	NODE_IDS_H	7: BusID[9]	R/W	Serial Bus ID Number Single Bus, Bus ID = 0x3FF Multiple Bus, Bus ID is uniquely specifying	0xFF	–	–
		6: BusID[8]					
		5: BusID[7]					
		4: BusID[6]					
		3: BusID[5]					
		2: BusID[4]					
		1: BusID[3]					
		0: BusID[2]					
0x21	NODE_IDS_L	7: BusID[1]					–
		6: BusID[0]					–
		5: PhyID[5]	R	Self Node's Physical ID Number	0xFF	–	1
		4: PhyID[4]					1
		3: PhyID[3]					1
		2: PhyID[2]					1
		1: PhyID[1]					1
		0: PhyID[0]					1

Node IDS Status Register (Higher Rank, Lower Rank)

This register indicates the bus ID of topology connected through the serial bus.

At the time of BusReset, the BusID does not change. When the self node is a bus manager, this register is writable. If you write when it is not a bus manager, the bus goes out of control. Never write when it is not a bus manager.

The PHY ID becomes a value of the 0x3F at the time of BusReset and is automatically stored on completion of the Self-ID processing.

0x20, 0x21 .Bit7..6 Bus ID

These bits are areas to store the Bus_ID value of the serial bus.

0x21 Bit5:0 PHY ID

Indicates the Physical ID of a node established by the PHY in the Self-ID phase.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x24	PhyAccCtl_H	7: RdReq	R/W	0: Normal	1: PHY Reg Rd Request	0x00	0x00	–
		6: WrReq	R/W	0: Normal	1: PHY Reg Wr Request			
		5:		0:	1:			
		4:		0:	1:			
		3: ReqAdd[3]	R/W	PHY Register Read/Write Request Address				
		2: ReqAdd[2]						
		1: ReqAdd[1]						
		0: ReqAdd[0]						

PHY Register Access Control Register (Higher Rank)

Bit7 PHY Register Read Request

When requesting the PHY Register for a register read, this bit is set to “1”. After the execution, it is automatically cleared.

Bit6 PHY Register Write Request

When requesting the PHY Register for a register write, this bit is set to “1”. After the execution, it is automatically cleared.

Bit5 Reserved

Bit4 Reserved

Bit3..0 PHY Access Register

Set a register address to access the PHY Register.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x25	PhyAccCtl_L	7: WrDat[7] 6: WrDAt[6] 5: WrDat[5] 4: WrDat[4] 3: WrDat[3] 2: WrDat[2] 1: WrDat[1] 0: WrDat[0]	R/W	PHY Register Write Data	0x00	0x00	–

PHY Register Access Control Register (Lower Rank)
Bit7..0 PHY Write Data
Set data to write to the PHY Register.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x26	PhyRdstat_H	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: RdAdd[3] 2: RdAdd[2] 1: RdAdd[1] 0: RdAdd[0]	R	PHY Register Read Address				

PHY Register Read Status Register (Higher Rank)
Bit7 Reserved
Bit6 Reserved
Bit5 Reserved
Bit4 Reserved
Bit3..0 PHY Read Address
Indicate a register address indicated in the PHY status.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x27	PhyRdstat_L	7: RdDat[7] 6: RdDat[6] 5: RdDat[5] 4: RdDat[4] 3: RdDat[3] 2: RdDat[2] 1: RdDat[1] 0: RdDat[0]	R	PHY Register Read Data	0x00	0x00	–

PHY Register Read Status Register (Lower Rank)
Bit7..0 PHY Read Data
Indicate register data indicated in the PHY status.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x28	ChnlIndex	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: Channel Index[3] 2: Channel Index[2] 1: Channel Index[1] 0: Channel Index[0]	R/W	ISO (Async Stream) Channel Index				
0x29	ChnlWindow	7: Channel Window[7] 6: Channel Window[6] 5: Channel Window[5] 4: Channel Window[4] 3: Channel Window[3] 2: Channel Window[2] 1: Channel Window[1] 0: Channel Window[0]	R/W	ISO (Async Stream) Cahnnel Window		0x00	0x00	–

ISO-Asyno Stream Channel Index Window Register

This register selects an ISO channel and Async Stream channel. The Channel Available Register is available when the Isochronous Resource Manager is used.

0x28 Channel Index

Sets an index number to select a channel.

0x29 Channel Window

Indicates a window specified by the Channel Index.

ChnlIndex									
	ChnlWindow	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	ChannelAvailableH0		ch01	ch02	ch03	ch04	ch05	ch06	ch07
0x01	ChannelAvailableH1	ch08	ch09	ch10	ch11	ch12	ch13	ch14	ch15
0x02	ChannelAvailableH2	ch16	ch17	ch18	ch19	ch20	ch21	ch22	ch23
0x03	ChannelAvailableH3	ch24	ch25	ch26	ch27	ch28	ch29	ch30	ch31
0x04	ChannelAvailableL0	ch32	ch33	ch34	ch35	ch36	ch37	ch38	ch39
0x05	ChannelAvailableL1	ch40	ch41	ch42	ch43	ch44	ch45	ch46	ch47
0x06	ChannelAvailableL2	ch48	ch49	ch50	ch51	ch52	ch53	ch54	ch55
0x07	ChannelAvailableL3	ch56	ch57	ch58	ch59	ch60	ch61	ch62	ch63
0x08	ReceiveChannel0	ch00	ch01	ch02	ch03	ch04	ch05	ch06	ch07
0x09	ReceiveChannel1	ch08	ch09	ch10	ch11	ch12	ch13	ch14	ch15
0x0A	ReceiveChannel2	ch16	ch17	ch18	ch19	ch20	ch21	ch22	ch23
0x0B	ReceiveChannel3	ch24	ch25	ch26	ch27	ch28	ch29	ch30	ch31
0x0C	ReceiveChannel4	ch32	ch33	ch34	ch35	ch36	ch37	ch38	ch39
0x0D	ReceiveChannel5	ch40	ch41	ch42	ch43	ch44	ch45	ch46	ch47
0x0E	ReceiveChannel6	ch48	ch49	ch50	ch51	ch52	ch53	ch54	ch55
0x0F	ReceiveChannel7	ch56	ch57	ch58	ch59	ch60	ch61	ch62	ch63

ChannelAvailable

This is a register to provide a channel number resource to be used when transferring isochronous and asynchronous stream.

ReceiveChannel

This is a register to set an ISO channel number to be received by this IC.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x2A	CmprIndex	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: Compare Index[3] 2: Compare Index[2] 1: Compare Index[1] 0: Compare Index[0]	R/W	Compare Address Index				
0x2B	CmprWindow	7: Compare Window[7] 6: Compare Window[6] 5: Compare Window[5] 4: Compare Window[4] 3: Compare Window[3] 2: Compare Window[2] 1: Compare Window[1] 0: Compare Window[0]	R/W	Compare Address Window		0x00	0x00	–

Compare Offset Address Index Window Register

This register sets a compare offset address.

When the BlkWrAreaSet bit is "1" and a BlockWriteRequest packet having an Destination_Offset address same as a value set to this register is received, the received data of payload is received by the RxStreamArea.

0x2A Compare Index

This is a register to set an index number to select a channel.

0x2B Compare Window

This is a register to view a window specified by the Compare Index.

Compare Address Index/Window Register									
ChnlIndex									
	ChnlWindow	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	CompareDOffset0	(MSB)							
0x01	CompareDOffset1								
0x02	CompareDOffset2				Compare Destination Offset Address[47:0]				
0x03	CompareDOffset3								
0x04	CompareDOffset4								
0x05	CompareDOffset5								(LSB)
0x06	(Reserved)								
:	(Reserved)								
0x0F	(Reserved)								

Compare Destination Offset Address

When the BlkWrAreaSet bit is "1" and a BlockWriteRequest packet having an Destination_Offset address same as a value set to this register is received, the received data of payload is received by the RxStreamArea. This address is valid when the BlkWrAreaSel bit of the AsyDmaCtl Register is "1".

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x2C	CYCLE_TIME_H	7: Cycle Second[6] 6: Cycle Second[5] 5: Cycle Second[4] 4: Cycle Second[3] 3: Cycle Second[2] 2: Cycle Second[1] 1: Cycle Second[0]	R/W	CYCLE_TIME.second_count	0x00	–	–
		0: Cycle Count[12]	R/W	CYCLE_TIME.cycle_count			
0x2D	CYCLE_TIME_MH	7: Cycle Count[11] 6: Cycle Count[10] 5: Cycle Count[9] 4: Cycle Count[8] 3: Cycle Count[7] 2: Cycle Count[6] 1: Cycle Count[5] 0: Cycle Count[4]			0x00	–	–
0x2E	CYCLE_TIME_ML	7: Cycle Count[3] 6: Cycle Count[2] 5: Cycle Count[1] 4: Cycle Count[0]			0x00	–	–
		3: Cycle Offset[11] 2: Cycle Offset[10] 1: Cycle Offset[9] 0: Cycle Offset8[]	R/W	CYCLE_TIME.cycle_offset			
0x2F	CYCLE_TIME_L	7: Cycle Offset[7] 6: Cycle Offset[6] 5: Cycle Offset[5] 4: Cycle Offset[4] 3: Cycle Offset[3] 2: Cycle Offset[2] 1: Cycle Offset[1] 0: Cycle Offset[0]			0x00	–	–

Cycle Time Register

Each of CycSecond, CycCount, and CycOffset Registers updates the timer by updating the current value of the cycle timer used for isochronous transfer.
When the self node is a CYCLE MASTER, set the value of each register in the CYCLE START PACKET.
When the self node is not a CYCLE MASTER, set the cycle_time_data of a received CYCLE START PACKET on each register.
This register is enabled when LINKCtl(Hi). DisCycTimer="0".
Reserve this register as a CycSecond(Hi) for WORD access.

CYCLE_TIME.second_count

This bit field indicates an integer at the place of Second of the cycle timer.
It is enabled when the LINKCtl(H).DisCycTimer= "0" and the Cycle Second is incremented every time the CycleCount reaches 8000. When the Cycle Second exceeds 127, it is restored to 0.

CYCLE_TIME.cycle_count

When the self node is a CYCLE MASTER and the DisCycTimer="0", it is incremented every time the Cycle Offset reached 3072. When the Cycle Count reaches 8000, it is restored to 0.

CYCLE_TIME. cycle.offset

When the self node is a CYCLE TIMER and the DisCycTimer="0", it is incremented in a cycle of 24.576MHz. When the Cycle Offset reaches 3072, it is restored to 0 and then the Cycle Count is incremented.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x30	HwSBP2Ctl	7: PtNotPresent	R/W	0: Present	1: Not Present			
		6: HOSTtoDev	R/W	0: Host <– Device	1: Host –> Device			
		5: FromStream	R/W	0: From PageTable	1: FromStream			
		4: LastPT	R/W	0: None	1: Ignore	0x00	0x00	–
		3: HwSBP2Rst	W	0: None	1: Reset			
		2: HwSBP2Rsum	W	0: None	1: Resume			
		1: HwSBP2Pause	W	0: None	1: Pause			
		0: HwSBP2Start	W	0: None	1: Start			

Hardware SBP2 Control Register

This register controls the SBP2 processing of this IC.

Bit7 UltraDmaMode

PtNotPresent:0 (Present) Set => PageTable exists.

PtNotPresent:1 (Not Present) Set => PageTable does not exist.

Bit6 HOSTtoDev

HOSTtoDev:0 (Host<-Device) Set => Transfers data from Device to Host.

HOSTtoDev:1 (Host->Device) Set => Transfers data from Host to Device.

Bit5 FromStream

FromStream:0 (FromPt) Set => Starts with the PageTable Processing.

FromStream:1 (FromStream) Set => Starts with the Stream processing.

Bit4 LastPT

This bit indicates the 0x32 bit 3 NotQuad status and specifies whether to generate an interrupt if SegmentLength of the last PageTableElement on PageTable is not the Quad unit during the HwSBP2 process.

LastPT: 0 (None) Set => The NotQuad status is indicated for the last PageTableElement and an interrupt is generated.

LastPT: 1 (Ignore) Set => The NotQuad status is not indicated for the last PageTableElement and an interrupt is not generated.

Bit3 HwSBP2Rst

SBP2Reset:1 (Reset) Set => Resets the hwSBP2.

If you read it, it indicates 0.

Bit2 HwSBP2Rsum

SBP2Resume:1 (Reset) Set => Resumes the hwSBP2 processing in pause.

If you read it, it indicates 0.

Bit1 HwSBP2Pause

SBP2Pause:1 (Pause) Set => Pauses the hwSBP2 processing in execution.

If you read it, it indicates 0.

Bit0 HwSBP2Start

SBP2Start:1 (Start) Set => Starts the hwSBP2 processing.

If you read it, it indicates 0.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x31	SBP2Stat	7: FwPause	R	0: Not Firmware Pause	1: FirmWre Pause			
		6: ErrPause	R	0: Not Error Pause	1: Error Pause			
		5: NotQuadEnable	R/W	0: Disable	1: Enable			
		4: WaitPLReady	R	0: Not Ready	1: Ready	0x00	0x00	–
		3: HwSBP2Exec	R	0: Stop	1: Execute			
		2: PTaskExec	R	0: Stop	1: Execute			
		1: StTaskExec	R	0: Stop	1: Execute			
		0: TranExec	R	0: Stop	1: Execute			

Hardware SBP2 Status Read Register

This register indicates the execution condition of the hardware SBP2.

Bit7 F/W Pause

When the firmware writes “1” at the HwSBP2Ctl. HwSBP2Pause bit during the execution of the HwSBP2Pause:1 (Pause) HwSBP2, this bit becomes “1”. When the firmware writes “1” at the HwSBP2Ctl.HwSBP2Rsum bit or resets it, it is cleared. Writing to this bit is ignored.

Bit6 Error Pause

When firmware enters the pause state without writing “1” at the HwSBP2Ctl.HwSBP2Pause bit during the execution of the HwSBP2Pause:1 (Pause) HwSBP2, this bit becomes “1”. It is cleared at the time of Reset. Writing to this bit is ignored.

Bit5 NotQuadEnable

This bit specifies whether to generate a 0x32 bit 3 NotQuad interrupt by if SegmentLength of PageTableElement is not the Quad unit during the HwSBP2 process.

NotQuadEnable: 0 (Disable) Set => A NotQuad interrupt is not generated.

NotQuadEnable: 1 (Enable) Set => A NotQuad interrupt is generated.

* Note that this bit does not indicate the status of HwSBP2.

Bit4 Wait Payload Ready

- WaitPLReady:0 (Not Ready) => Payload Domain Not Ready
- WaitPLReady:1 (Ready) => Payload Domain Ready

When the IDE interface has a problem, the payload may not be ready. At that time, perform a recovery processing by the firmware.

Bit3 HwSBP2Exec

- HwSBP2Exec:0 (Stop) => Indicates the HwSBP2 processing is completed.
- HwSBP2Exec:1 (Execute) => Indicates the HwSBP2 processing is in execution.

It is cleared at the time of Reset. Writing to this bit is ignored..

Bit2 PageTaskExec

- PageTaskExec:0 (Stop) => Indicates a PageTask is completed.
- PageTaskExec:1 (Execute) => Indicates a PageTask is in execution.

It is cleared at the time of Reset. Writing to this bit is ignored..

Bit1 StreamTaskExec

- StreamTaskExec:0 (Stop) => Indicates a StreamTask is completed.
- StreamTaskExec:1 (Execute) => Indicates a StreamTask is in execution.

It is cleared at the time of Reset. Writing to this bit is ignored..

Bit0 TranExec.

- TranExec:0 (Stop) => Indicates a Transaction is completed.
- TranExec:1 (Execute) => Indicates a Transaction is in execution.

It is cleared at the time of Reset. Writing to this bit is ignored..

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x32	SBP2IntStat	7: SplitTimeOut	R(W)	0: None	1: SplitTimeOut			
		6: TxAckedIllegal	R(W)	0: None	1: TxAckedIllegal			
		5: TxAckMiss	R(W)	0: None	1: TxAsyMiss			
		4: BrAbort	R(W)	0: None	1: BrAbort	0x00	0x00	–
		3: NotQuad	R(W)	0: None	1: NotQuad			
		2: RxNotRespCmp	R(W)	0: None	1: RxNotRespCmp			
		1: RxBroadCast	R(W)	0: None	1: RxBroadCast			
		0: RxAckDataErr	R(W)	0: None	1: RxAckDataErr			

Hardware SBP2 Interrupt Status Register

This register indicates error information when an error arises in execution of the hardware SBP2 processing. At the same time, it asserts the HwSBP2Err bit of the SubIntStat Register. When clearing it, write “1” to a bit to clear.

This register is automatically cleared when setting HwSBP2Ctl.HwSBP2Start or the HWSBP2Ctl. HwSBP2Rst.

Bit7 Split Timeout

- SplitTimeOut:1 => During the HwSBP2 processing, an SPLIT TIMEOUT error arose.

Bit6 Tx Acked Illegal

TxAckedIllegal:1 => Though a transmission was completed, a response other than ack_pending was given to a BlkRdReq and a response other than ack_completed was given to a BlkWrReq.

Bit5 Tx Ack Miss

- TxAsyMiss:1 => Though a transmission was completed, no Ack was returned.

Bit4 BRAbort

- When the HwSBP2Ctl.HwSBP2Start bit is set to “1” or HWSBP2Ctl.Resume bit is set to “1” during the BusReset period, this bit becomes “1”,

Bit3 NotQuad

This bit indicates 1 if SegmentLength of PageTableElement is not the Quad unit during the HwSBP2 process. No data transmission to the detected PageTableElement occurs.

This bit is cleared when 1 is written.

This bit is automatically cleared when a Transaction starts or SBP2Reset is issued.

Bit2 RxNotRespCmp

- RxNotRespCmp:1 => Though a response packet receive was completed, its code was other than resp_complete.

Bit1 RxBroadcast

- RxBroadCast:1 => Though a response packet receive was completed, it was a broadcast packet.

Bit0 RxAckDataError

- RxAckDataErr:1 => Though a response packet was received, it was a DataCRCError. It does not assert the interrupt signal SBP2Err. It is automatically cleared on completion of the Transaction.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x33	HwSBP2Index	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: HwSBP2 Index[3] 2: HwSBP2 Index[2] 1: HwSBP2 Index[1] 0: HwSBP2 Index[0]	R/W	HwSBP2 Index				
0x34	HwSBP2Window_H	7: HwSBP2 Window[15] 6: HwSBP2 Window[14] 5: HwSBP2 Window[13] 4: HwSBP2 Window[12] 3: HwSBP2 Window[11] 2: HwSBP2 Window[10] 1: HwSBP2 Window[9] 0: HwSBP2 Window[8]	R/W	HwSBP2 Window		0x00	0x00	–
0x35	HwSBP2Window_L	7: HwSBP2 Window[7] 6: HwSBP2 Window[6] 5: HwSBP2 Window[5] 4: HwSBP2 Window[4] 3: HwSBP2 Window[3] 2: HwSBP2 Window[2] 1: HwSBP2 Window[1] 0: HwSBP2 Window[0]				0x00	0x00	–

Hardware SBP2 Index Window Register

This register functions as an Index Register and Window Register to set a register to use for the HwSBP2 processing.

HwSBP2Index

This register sets an index number to select a channel.

HwSBP2Window

This register indicates a window specified by the HwSBP2Index.

H/W SBP2 Index Chnnel/Window Register									
SBP2Index									
	SBP2Window_H/L	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	PageBoundary						PageBoundary[2:0]		
	PageElementNunber				PageElementNumber[4:0]				
0x01	PgElmentRemain_H	(MSB)	Page Element Remain Length (Bytes)						
	PgElmentRemain_L								(LSB)
0x02	SpeedCode						SpeedCode[2:0]		
	MaxPayload					MaxPayload[3:0]			
0x03	DestinationID_H	(MSB)							
	DestinationID_L				Destination_ID Value				(LSB)
0x04	SplitTime_H		Second[2:0]			Cycle Count[12:8]			
	SplitTime_L				Cycle Count[7:0]				
0x05	(Reserved)								
:	(Reserved)								
0x0F	(Reserved)								

PageBoundary

Set a value of page boundary to use for the HwSBP2. The actual page boundary is as follows.
PageBoundary =2 $^{(PageBoundary\ +8)}$ Bytes

PageElementNumber

Sets a page element number with which the HwSBP2 starts a processing.
When the HwSBP2Ctl.PtPresent:1, set a value equal to or less. than 0x17
When the HwSBP2Ctl.PtPresent:0, set a value equal to or less than 0x02.
If you read it, the page element number currently in process is indicated.

PgElementRemain

Indicates the number of remaining data bytes of the page element currently being processed by the HwSBP2.
This register is read-only.

SpeedCode

Sets the speed code of 1394 bus to be used for data transfer by the HwSBP2.
SpeedCode:0 100Mbps
SpeedCode:1 200Mbps
SpeedCode:2 400Mbps
SpeedCode:3 Reserved

MaxPayload

Sets the max. payload value to be used by the HwSBP2. The actual payload size is as follows.
Payload = 2 $^{(MaxPayload+2)}$ Bytes
Since the max. payload size transferable at 400Mbps is 2048 bytes, set “9” or less for this register.

Destination_ID

This is a register to set a transmit destination of the HwSBP2. Set a Bus ID (10 bits) and Node ID (6 bits).

SplitTime

Set a split timeout time of a transaction of the HwSBP2.
SplitTime.Second: Set a value in second.
SplitTime.CycleCount: Set a value in 125µs. (Set range: 0 to 0x1F3F) Setting of a value exceeding 0x1F3F is not possible.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst

0x36	PayloadSize_H	7:
		6:
		5:
		4:
		3: Payload Size[11]
		2: Payload Size[10]
		1: Payload Size[9]
		0: Payload Size[8]
			R/W	Set Payload Size (Bytes)
				If (HwSBP2Ctl.HwSBP2Exec ==0) {
				Write is valid.
				} else {
				Write is invalid.
				}
					0x00	0x00	–

0x37	PayloadSize_L	7: Payload Size[7] 6: Payload Size[6] 5: Payload Size[5] 4: Payload Size[4] 3: Payload Size[3] 2: Payload Size[2] 1: Payload Size[1] 0: Payload Size[0]			0x00	0x00	–

Hardware SBP2 Payload Size Set Register

Set this register when the firmware handles data to a StreamArea to be used by the HwSBP2.
When the HwSBP2Stat.Exec.:"1" (in execution of HwSBP2), writing to this register is ignored.
When the RxStreamArea receives data the equivalent of this size, the BufMoniter.RxPayldRdy bit becomes "1".
If free space the equivalent of a size set here exists in the TxStreamArea, the BufMoniter. TxPayldRdy bit becomes "1".
Payload Size [11:0]
Set a payload size to use for data transfer in byte.
The settable size is 2^n (n:2 to 11) bytes.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst

0x38	PageTableSize_H	7: Page Table Size[15]
		6: Page Table Size[14]
		5: Page Table Size[13]
		4: Page Table Size[12]
		3: Page Table Size[11]
		2: Page Table Size[10]
		1: Page Table Size[9]
		0: Page Table Size[8]
			R/W	If (HwSBP2Ctl.PtNotPresent == 0) {
				Write:Set PageElement *8 (bytes)
				Read :Indicate Page Table Size
				} else {
				Write:Set Data Length (bytes)
				Read :Indicate Create PageElement *8 (bytes)
				}
					0x00	0x00	–

0x39	PageTableSize_L	7: Page Table Size[7] 6: Page Table Size[6] 5: Page Table Size[5] 4: Page Table Size[4] 3: Page Table Size[3] 2: Page Table Size[2] 1: Page Table Size[1] 0: Page Table Size[0]			0x00	0x00	–

Hardware Page Table Size Set Register

The Write and Read of this register have different meanings depending on whether a PageTable is present (setting of HwSBP2Ctl.PtNotPresent bit).

- When a PageTable is present
  Write: Set a PageTable size in byte. (The number of pages x 8 bytes)
  Read: Indicates the remaining PageTable size.
- When a PageTable is not present
  Write: Set a data length.
  Read: Indicates a new PageTable size based on the written data size. (The number of pages x 8 bytes)
  When it is not written, zero can be read if the HwSBP2 correctly finishes. The remaining table size can be read when it is in execution or it finishes incorrectly.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x3A	PageTableAdrs0	7: PtAdress[47] 6: PtAdress[46] 5: PtAdress[45] 4: PtAdress[44] 3: PtAdress[43] 2: PtAdress[42] 1: PtAdress[41] 0: PtAdress[40]	R/W	Write: Set PageTable Offset Address Read: Indicate NextPageTable Offset Address	0x00	0x00	–
0x3B	PageTableAdrs1	7: PtAdress[39] 6: PtAdress[38] 5: PtAdress[37] 4: PtAdress[36] 3: PtAdress[35] 2: PtAdress[34] 1: PtAdress[33] 0: PtAdress[32]			0x00	0x00	–
0x3C	PageTableAdrs2	7: PtAdress[31] 6: PtAdress[30] 5: PtAdress[29] 4: PtAdress[28] 3: PtAdress[27] 2: PtAdress[26] 1: PtAdress[25] 0: PtAdress[24]			0x00	0x00	–
0x3D	PaqeTableAdrs3	7: PtAdress[23] 6: PtAdress[22] 5: PtAdress[21] 4: PtAdress[20] 3: PtAdress[19] 2: PtAdress[18] 1: PtAdress[17] 0: PtAdress[16]			0x00	0x00	–
0x3E	PageTableAdrs4	7: PtAdress[15] 6: PtAdress[14] 5: PtAdress[13] 4: PtAdress[12] 3: PtAdress[11] 2: PtAdress[10] 1: PtAdress[9] 0: PtAdress[8]			0x00	0x00	–
0x3F	PageTableAdrs5	7: PtAdress[7] 6: PtAdress[6] 5: PtAdress[5] 4: PtAdress[4] 3: PtAdress[3] 2: PtAdress[2] 1: PtAdress[1] 0: PtAdress[0]			0x00	0x00	–

Hardware SBP2 Page Table Address Set Register

This register specifies an address specified by the ORB of the SBP2. It is automatically updated in execution of the HwSBP2.

Page Table Offset Address

Write: Sets a Destination_Offset_Address accessed by the HwSBP2. It is ignored in execution of the HwSBP2.

Read: Indicates the PageTable address following one being processed by the HwSBP2.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x40	LinkRxHdrPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: LRHP[12] 3: LRHP[11] 2: LRHP[10] 1: LRHP[9] 0: LRHP[8]	R/W	Current Received Packet Header Area Pointer			
0x41	LinkRxHdrPtr_L	7: LRHP[7] 6: LRHP[6] 5: LRHP[5]					
		4: 3: 2: 1: 0:		Write is ignore Read is always zero	0x00	0x00	–

Receive Header LINK Pointer Register

This Receive Header LINK Pointer Register indicates the starting address of the latest receive packet in the RxHeaderArea. Since the buffer pointer is given in 8Quadlet unit, the lower order 5 bits are always “0”. Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always “0”.

Reading the higher order bytes holds the lower order bytes. Read the higher order bytes first, then the lower order bytes.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x42	LinkRxORBPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: POP[12] 3: POP[11] 2: POP[10] 1: POP[9] 0: POP[8]	R/W	Current Received Packet ORB Data Area Pointer			
0x43	LinkRxORBPtr_L	7: POP[7] 6: POP[6] 5: POP[5] 4: POP[4] 3: POP[3] 2: POP[2]					
		1: 0:		Write is ignore Read is always zero			

Receive ORB Data LINK Pointer Register

This Receive ORB Data LINK Pointer Register indicates the starting address of the latest receive ORB data in the RxORBdataArea. Since the buffer pointer is in Quadlet unit, the lower order 2 bits are always “0”. Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always “0”.

Reading the higher order bytes holds the lower order bytes. Read the higher order bytes first, then the lower order bytes.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x44	LinkRxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: PSP[12] 3: PSP[11] 2: PSP[10] 1: PSP[9] 0: PSP[8]	R/W	Current Received Packet Stream Data Area Pointer			
0x45	LinkRxStreamPtr_L	7: PSP[7] 6: PSP[6] 5: PSP[5] 4: PSP[4] 3: PSP[3] 2: PSP[2]			0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			

Receive Stream Data LINK Pointer Register

This Receive Stream Data LINK Pointer Register indicates the starting address of the latest received stream data in the RxStreamdataArea. Since the buffer pointer is in Quadlet unit, the lower order 2 bits are always “0”. Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always “0”.

Reading the higher order bytes holds the lower order bytes. Read the higher order bytes first, then the lower order bytes.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x46	LinkTxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	
		4: PTDP[12] 3: PTDP[11] 2: PTDP[10] 1: PTDP[9] 0: PTDP[8]	R	Current Transmit Packet Data Area Pointer			
0x47	LinkTxStreamPtr_L	7: PTDP[7] 6: PTDP[6] 5: PTDP[5] 4: PTDP[4] 3: PTDP[3] 2: PTDP[2]			0x00	0x00	
		1: 0:		Write is ignore Read is always zero			

Transmit Stream Data LINK Pointer Register

This Transmit Stream Data LINK Pointer Register indicates the starting address of unused area in the RxStreamArea. Since the buffer pointer is in Quadlet unit, the lower order 2 bits are always “0”. Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always “0”.

Reading the higher order bytes holds the lower order bytes. Read the higher order bytes first, then the lower order bytes. This register is read-only. Writing is ignored.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x48	UsedRxHdrPtr_H	7: 6: 5:		Write is ignore Read always zero	0x00	0x00	–
		4: URHP[12] 3: URHP[11] 2: URHP[10] 1: URHP[9] 0: URHP[8]	R/W	Received Packet Header Area Used Pointer			
0x49	UsedRxHdrPtr_L	7: URHP[7] 6: URHP[6] 5: URHP[5]					
		4: 3: 2: 1: 0:		Write is ignore Read is always zero	0x00	0x00	–

Used Receive Header Pointer Register

This Used Receive Header Pointer Register indicates the starting address of used header of a receive packet in the RxHdrArea. Since the buffer pointer is in 8Quadlet unit, the lower order 5 bits are always “0”. Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always “0”.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x4A	UsedRxORBPtr_H	7: 6: 5:		Write is ignore Read is always zero	0x00	0x00	–
		4: UOP[12] 3: UOP[11] 2: UOP[10] 1: UOP[9] 0: UOP[8]	R/W	Received Packet ORB Data Area Used Pointer			
0x4B	UsedRxORBPtr_L	7: UOP[7] 6: UOP[6] 5: UOP[5] 4: UOP[4] 3: UOP[3] 2: UOP[2]					
		1: 0:		Write is ignore Read is always zero			

Used Receive ORB Data Pointer Register

This Used Receive ORB Data Pointer Register indicates the starting address of used ORB data of receive packet in the RxORBArea. Since the buffer pointer is in Quadlet unit, the lower order 2 bits are always “0”. Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always “0”.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x4C	IDE_RxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero			
		4: IRSP[12] 3: IRSP[11] 2: IRSP[10] 1: IRSP[9] 0: IRSP[8]			0x00	0x00	–
0x4D	IDE_RxStreamPtr_L	7: IRSP[7] 6: IRSP[6] 5: IRSP[5] 4: IRSP[4] 3: IRSP[3] 2: IRSP[2]	R/W	Received Packet Stream Data Area IDE Pointer			
		1: 0:		Write is ignore Read is always zero	0x00	0x00	–

Receive Stream Data IDE Pointer Register

This Receive Stream Data IDE Pointer Register indicates the starting address of received stream data in the RxSTreamArea that is to be transmitted to the IDE side but not yet transmitted. Since the buffer pointer is in Quadlet unit, the lower order 2 bits are always "0". Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always "0".

Reading the higher order bytes holds the lower order bytes. Read the higher order bytes first, then the lower order bytes.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x4E	IDE_TxStreamPtr_H	7: 6: 5:		Write is ignore Read is always zero			
		4: ITSP[12] 3: ITSP[11] 2: ITSP[10] 1: ITSP[9] 0: ITSP[8]			0x00	0x00	–
0x4F	IDE_TxStreamPtr_L	7: ITSP[7] 6: ITSP[6] 5: ITSP[5] 4: ITSP[4] 3: ITSP[3] 2: ITSP[2]	R/W	Transmit Packet Stream Data Area IDE Pointer			
		1: 0:		Write is ignore Read is always zero	0x00	0x00	–

Transmit Stream Data IDE Pointer Register

This Transmit Stream Data IDE Pointer Register indicates the starting address of stream data in the RxStreamArea to be stored following the data that was transmitted from the IDE to the SRAM. Since the buffer pointer is in Quadlet unit, the lower order 2 bits are always "0". Also, since the buffer size is 2 Kbytes, the higher order 3 bits are always "0".

Reading the higher order bytes holds the lower order bytes. Read the higher order bytes first, then the lower order bytes.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x50	BufControl	7: TxStreamClr	W	0: None Affect	1: Tx Stream Data Clear			
		6: RxStreamClr	W	0: None Affect	1: Rx Stream Data Clear			
		5: RxORBClr	W	0: None Affect	1: Rx ORB Dat Clear			
		4: RxHdrClr	W	0: None Affect	1: Rx Header Clear	0x00	0x00	–
		3:		0:	1:			
		2:		0:	1:			
		1:		0:	1:			
		0: UpdLinkTxStrm	W	0: None Affect	1: Update Link Tx Stream Ptr			

Buffer Control Register

This Buffer Control Register restores each pointer of the TxStreamArea, RxStreamArea, RxORBARea, and RxHeaderArea to the initial set pointer address. It also controls updates of the LINKTxStreamPtr. This register is read-only. If you read it, it always indicates zero.

bit7 Tx Stream Clear

Writing “1” to this bit changes the values of LINKTxStreamPtr and IDE_TxStreamPtr to ones set by the TxStreamAreaStart Register.

bit6 Rx Stream Clear

Writing “1” to this bit changes the values of LINKRxStreamPtr and IDE_RxStreamPtr to ones set by the RxStreamAreaStart Register.

bit5 Rx ORB Clear

Writing “1” to this bit changes the values of LINKRxORBPtr and IDE_RxORBPtr to ones set by the RxORBAreaStart Register.

bit4 Rx Header Clear

Writing “1” to this bit changes the values of LINKRxHdrPtr and UsedRxHdrPtr to the value of 0x0100.

bit3::1 Reserved

bit0 Update LINKTxStreamPtr

Writing “1” to this bit updates the value of LINKTxStreamPtr to the latest value.

When the firmware transmits data, this bit confirms that the transmit is normally completed as an error recovery to update the LINKTxStreamPtr. Do not use this bit in execution of the HwSBP2.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x51	BufMonitor	7: RxPayldRdy	R	0: Rx Payld Capa not Ready	1: Rx Payload Capa Ready			
		6: TxPayldRdy	R	0: Tx Payld Capa not Ready	1: Tx Payload Capa Ready			
		5:		0:	1:			
		4: TxStreamFull	R	0: NotFull	1: Full	0x00	0x00	–
		3: RxHdrRemain	R	0: Rx Header Area Empty	1: Rx Header not Empty			
		2: RxORBFull	R	0: Rx ORB Area not Full	1: Rx ORB Data Area Full			
		1: RxStreamFull	R	0: Rx Stream Area not Full	1: Rx Stream Data Area Full			
		0: RxHdrFull	R	0: Rx Header Area not Full	1: Rx Header Area Full			

Buffer Monitor Register

This Buffer Monitor Register indicates each buffer area status.
This register is read-only. Writing to this register is ignored..

bit7 Rx Payload Ready

When a free space the equivalent of the size set by the PyloadSize Register exists in the RxStreamArea, this bit becomes “1”. When not, this bit becomes “0”.

bit6 Tx Payload Ready

When transmit data the equivalent of the size set by the PayloadSize Register is accumulated in the RxStreamArea, this bit becomes “1”. When not, this bit becomes “0”.

bit5 Reserved

bit4 TxStreamFull

This bit indicates the status of the transmitting stream buffer. This bit becomes “1” when the buffer is full, and “0” in other statuses.

bit3 Received Header Remain

When an unused packet header exists in the header area of a receive packet, this bit becomes “1”.
When the firmware rewrites the UsedRxHdrPtr to one same as LINKRxHdrPtr or when you write “1” to the BufControl.RxHdrCtr bit, this bit becomes “0”.

Bit2 Received ORB Data Full

When the ORB buffer area of receive packet data is full of received data, this bit becomes “1”. The firmware must turn on RxDMACtl.ForceBusy bit if this bit is turned on to give priority to the processing to free the buffer by starting a processing with the first received packet immediately. When the receive buffer area is freed, the RxDMACtl.ForceBusy is cleared.

Bit1 Received Stream Data Full

When the stream buffer area of receive packet data is full of received data, this bit becomes “1”. The firmware must turn on the RxDMACtl.ForceBusy bit if this bit is turned on to give priority to the processing to free the buffer by starting a processing with the first received packet immediately. When the receive buffer area is freed, the RxDMACtl.ForceBusy is cleared.

Bit0 Received Header Full

When the header area of receive packet data is full, this bit becomes “1”. The firmware must turn on the RxDMACtl.ForceBusy bit if this bit is turned on to give priority to the processing to free the buffer by starting a processing with the first received packet immediately. When the receive buffer area is freed, the RxDMACtl.ForceBusy is cleared.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x52	AsyDmaCtl	7: AsyChnlSel	R/W	0: AsyTxPktHdr0	1: AsyTxPktHdr1			
		6:		0:	1:			
		5:		0:	1:			
		4: BlkWrAreaSel	R/W	0: Rx ORB Area	1: Rx Stream Area	0x00	0x00	–
		3: AsyFIFOEpty	R	0: AsyFIFO Empty	1: Non Empty			
		2: AsyFIFOClr	W	0: Normal	1: AsyFIFO Clear			
		1: AsyTxMon	R	0: Async Tx Stop	1: Async Tx Run			
		0: AsyStart	W	0: normal	1: Async Start			

Async TxDMA Control Register

Bit7 Async Transmit Packet Header Channel Select

Selects the header area of an Async Transmit packet from DMA. You transmit send a transmit packet from the selected area. This bit selects “0”: AsyncTxPktHdr0 or “1”: AsyncTxPktHdr1. Since the AsyncTxPktHdr1 area overlaps the ISOTxPktHdr area, however, the firmware must decide how to use this area.

Bit6 Reserved

Bit5 Reserved

Bit4 Block Write Request Packet Data Area Select

Can divide the store area of the Block Write Request packet data between the RxORBArea and RxStreamArea.
o:RxORBArea
1:RxStreamArea

Bit3 Async FIFO Empty

When the DMA-FIFO for Async is empty, this bit becomes “0”. When it is not empty, it is “1”. This bit is read-only and writing to this bit is ignored.

Bit2 Async FIFO Clear

Clears the DMA-FIFO for Async. Writing “1” to this bit clears the FIFO. After clearing it, this bit is automatically restored to “0”.

Bit1 Async Transmit Monitor

Indicates the transmit status of Async. “1” indicates that an Async packet is in transmission and “0” indicates that no Async packet is in transmission. This bit is read-only and writing to this bit is ignored.

Bit0 Async Transmit Start

Transmits an Async packet. Writing “1” to this bit starts to transmit an Async packet. On completion of the transmission, it is automatically restored to “0”. If you read this bit, it always indicates “0” regardless of presence/absence of transmit.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x53	IsoDmaCtl	7: IsoChnlSel	R/W	0: IsoTxPktHdr0	1: IsoTxPktHdr1			
		6:		0:	1:			
		5:		0:	1:			
		4: SelTxPtr	R/W	0: Async Tx Pointer Select	1: ISO Tx Pointer Select	0x00	0x00	–
		3: IsoFIFOEpty	R	0: IsoFIFO Empty	1: Non Empty			
		2: IsoFIFOClr	W	0: Normal	1: IsoFIFO Clear			
		1: IsoTxMon	R	0: Iso Tx Stop	1: Iso Tx Run			
		0: IsoStart	W	0: normal	1: Start			

ISO TxDMA Control Register

Bit7 ISO Transmit Packet Header Channel Select

Selects the header area of an ISO Transmit packet from DMA. You can transmit a transmit packet from the selected area. This bit selects “0”: ISOTxPktHdr0 or “1”: ISOTxPktHdr1. Since the ISOAsyncTxPktHdr0 and ISOAsyncTxPktHdr1 areas overlap the AsyncTxPktHdr1 area, however, the firmware must decide how to use this area.

Bit6..5 Reserved

Bit4 Select Transmit Pointer

Can switch the address pointed by the PostTxDataPtr of a transmit packet to one for Async or ISO. The PostTxData Ptr indicates a pointer of current transmit address; “0” indicates it is for Async and “1” indicates it is for ISO.

Bit3 ISO FIFO Empty

When the DMA-FIFO for ISO is empty, this bit becomes “0”. When it is not empty, it is “1”. This bit is read-only and writing to this bit is ignored.

Bit2 ISO FIFO Clear

Clears the DMA-FIFO for ISO. Writing “1” to this bit clears the FIFO. After clearing it, this bit is automatically restored to “0”.

Bit1 ISO Transmit Monitor

Indicates the transmit status of ISO. “1” indicates that an ISO packet is in transmission and “0” indicates that no ISO packet is in transmission. This bit is read-only and writing to this bit is ignored.

Bit0 ISO Transmit Start

Transmits an ISO packet. Writing “1” to this bit starts to transmit an ISO packet. On completion of the transmission, it is automatically restored to “0”. If you read this bit, it always indicates “0” regardless of presence/absence of transmit.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x54	RxDmaCtl	7:		0:	1:			
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:	0x00	0x00	–
		3: RxFIFOEpty	R	0: Rx FIFO Empty	1: Non Empty			
		2: RxFIFOClr	W	0: Normal	1: Rx FIFO Clear			
		1: RxMon	R	0: Rx Stop	1: Rx Run			
		0: ForceBusy	R/W	0: Normal	1: Busy			

Rx DMA Control Register

Bit7..4 Reserved

Bit3 Receive FIFO Empty

When the DMA-FIFO for reception is empty, this bit becomes “0”. When it is not empty, it is “1”. This bit is read-only and writing to this bit is ignored.

Bit2 Receive FIFO Clear

Clears the DMA-FIFO for reception. Writing “1” to this bit clears the FIFO. After clearing it, this bit is automatically restored to “0”.

Bit1 Reception Monitor

Indicates the receive status of ISO. “1” indicates that a receive packet is in reception and “0” indicates that no receive packet is in reception. This bit is read-only and writing to this bit is ignored.

Bit0 Force Busy

Setting this bit to “1” can forcedly return an Ack_Busy to a receive packet.

Before performing the RxData Clear or RxHdrClear, be sure to set this bit.

If you set this bit during receiving a packet, the packet operates to complete the reception regardless of to what extent the packet has been received. It means that a RxDmaCmp interrupt occurs if this packet has been correctly received. The Ack_busy is continuously returned to the subsequent receive packets.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x55	AreaIndex	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: MemMapIndex[3] 2: MemMapIndex[2] 1: MemMapIndex[1] 0: MemMapIndex[0]	R/W	Memory Map Area Index				
0x56	AreaWindow_H	7: MemMapWindow[15] 6: MemMapWindow[14] 5: MemMapWindow[13] 4: MemMapWindow[12] 3: MemMapWindow[11] 2: MemMapWindow[10] 1: MemMapWindow[9] 0: MemMapWindow[8]	R/W	Memory Map Area Window		0x00	0x00	–
0x57	AreaWindow_L	7: MemMapWindow[7] 6: MemMapWindow[6] 5: MemMapWindow[5] 4: MemMapWindow[4] 3: MemMapWindow[3] 2: MemMapWindow[2] 1: MemMapWindow[1] 0: MemMapWindow[0]				0x00	0x00	–

Memory Map Area Set Index Window Register

This register is an Index Register and Window Register to set each area of a memory map.

MemMapIndex

Sets an index number to select a register to set the starting address of each area of a memory map.

MemMapWindow

Indicates a window specified by the MemMapWindow.

Memory Map Area Index/Window Register									
AreaIndex									
	AreaWindow_H/L	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	RxORBAreaStart_H				(MSB)	RxORBAreaStart[12:8]			
	RxORBAreaStart_L	RxORBAreaStart[7:2]					(LSB)		
0x01	TxHdrAreaStart_H				(MSB)	TxHdrAreaStart[12:8]			
	TxHdrAreaStart_L	TxHdrAreaStart[7:2]					(LSB)		
0x02	TxStreamAreaStart_H				(MSB)	TxStreamAreaStart[12:8]			
	TxStreamAreaStart_L	TxStreamAreaStart[7:2]					(LSB)		
0x03	TxStreamAreaEnd_H				(MSB)	TxStreamAreaEnd[12:8]			
	TxStreamAreaEnd_L	TxStreamAreaEnd[7:2]					(LSB)		
0x04	RxStreamAreaStart_H				(MSB)	RxStreamAreaStart[12:8]			
	RxStreamAreaStart_L	RxStreamAreaStart[7:2]					(LSB)		
0x05	(Reserved)								
:	(Reserved)								
0x0F	(Reserved)								

RxORBAreaStart

This register sets the starting address of a receive ORB data area.

TxHeaderAreaStart

This register sets the starting address of a transmit header area.

TxStreamAreaStart

This register sets the starting address of a transmit stream data area.

TxStreamAreaEnd

This register sets the ending address of a transmit stream data area. The actual data store area is up to immediately before this specified address.

RxStreamAreaStart

This register sets the starting address of a receive stream data area.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x58	BRstHdrPtr_H	7: 6: 5:		Write is ignore Read is always zero			
		4: BusResetPtr[12] 3: BusResetPtr[11] 2: BusResetPtr[10] 1: BusResetPtr[9] 0: BusResetPtr[8]	R	Bus Reset Header Area Pointer This register indicates Address in Rx Header Area	0x00	0x00	–
0x59	BRstHdrPtr_L	7: BusResetPtr[7] 6: BusResetPtr[6] 5: BusResetPtr[5]		when BusRest detected.			
		4: 3: 2: 1: 0:		Write is ignore Read is always zero	0x00	0x00	–

Bus Reset Header Pointer Register

This Bus Reset Header Pointer Register holds the value of a PostRxHdrPtr when a bus reset occurs. When several bus resets occur, it is updated to the latest PostRxHdrPtr. This register is read-only and writing to this register is ignored.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x5A	BRstORBPtr_H	7: 6: 5:		Write is ignore Read is always zero			
		4: BusRstORBPtr[12] 3: BusRstORBPtr[11] 2: BusRstORBPtr[10] 1: BusRstORBPtr[9] 0: BusRstORBPtr[8]		Bus Reset ORB-Data Area Pointer	0x00	0x00	–
0x5B	BRstORBPtr_L	7: BusRstORBPtr[7] 6: BusRstORBPtr[6] 5: BusRstORBPtr[5] 4: BusRstORBPtr[4] 3: BusRstORBPtr[3] 2: BusRstORBPtr[2]	R	This register indicates Address in Rx ORB Data Area when BusRest detected.	0x00	0x00	–
		1: 0:		Write is ignore Read is always zero			

Bus Reset ORB Pointer Register

This Bus Reset Header Pointer Register holds the value of a PostRxORBPtr when a bus reset occurs. When several bus resets occur, it is updated to the latest PostRxORBPtr. This register is read-only and writing to this register is ignored.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x5E	MaintCtl_H	7: E_Hcrc	R/W	0: 1: Add Header CRC Error			
		6: E_Dcrc	R/W	0: 1: Add Data CRC Error			
		5: No_Pkt	R/W	0: 1: No Transmit Next Packet			
		4: F_Ack	R/W	0: 1: Tx Optional AckCode	0x00	0x00	–
		3: N_ack	R/W	0: 1: No Transmit AckPacket			
		2:		0: 1:			
		1:		0: 1:			
		0:		0: 1:			

Maintenance Control Register

This Maintenance Control Register enables intentional generation of a serial bus error.

Bit7 Error Header CRC

Writing “1” to this bit sets an invalid value for the Header CRC of a transmit packet to be generated next. After transmitting it, this bit is cleared to “0”.

Bit6 Error Data CRC

Writing “1” to this bit sets an invalid value for the Data CRC of a transmit packet to be generated next. After transmitting it, this bit is cleared to “0”.

Bit5 No Packet

Writing “1” to this bit abandons a transmit packet to be generated next. Immediately after abandoning it, this bit is cleared.

Bit4 F_Ack

Writing “1” to this bit transmits the value in the MainCtl(Lo).Ack Register to the ACK packet to be generated next. Immediately after transmitting it, this bit is cleared to “0”.

Bit3 No_Ack

Writing “1” to this bit abandons the ACK packet to be generated next without transmitting it. Immediately after abandoning it, this bit is cleared to “0”.

Bit2..0 Reserved

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x5F	MaintCtl_L	7: Ack[7] 6: Ack[6] 5: Ack[5] 4: Ack[4] 3: Ack[3] 2: Ack[2] 1: Ack[1] 0: Ack[0]	R/W	Optional AckCode	0x00	0x00	–

Maintenance Control Register

When the F_Ack bit is “1”, this register is enabled. When the F_Ack bit is set, an Ack_Code (Ack[7::4]) and Ack_Parity(Ack[3::0]) specified on this register are transmitted.

Bit7..4 Ack Code

Set an arbitrary Ack code.

Bit3..0 Ack_Parity

Set a parity bit for the Ack_Code.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x60	IDE_Config0	7: UltraDmaMode	R/W	0: DMA Mode	1: Ultra DMA Mode	0x00	0x00	–
		6: DmaMode		0: PIO Mode	1: DMA Mode			
		5: ActPort		0: None	1: Active			
		4:		0:	1:			
		3: DMARQ_Level		0: Positive Logic	1: Negative Logic			
		2: Swap		0: Nomal	1: Swap IDE Port Hi & Lo			
		1:		0:	1:			
		0:		0:	1:			

IDE Configuration Register

This register sets the mode of operation of the IDE interface of this IC.

Bit7 UltraDmaMode

When bit6:DmaMode is “1” and bit 7:Ultra Dma Mode is “1”, this bit sets the DMA transfer mode at ULTRA-DMA.

When bit6:DmaMode is “0”, the setting of this bit is invalid.

Bit6 DmaMode

Sets the IDE interface transfer mode at DMA or PIO.

DmaMode:1 DMA mode

DmaMode:0 PIO mode

Bit5 Activate IDE Port

The IDE interface is in all-pin input mode after a reset. By setting this bit at “1”, it is activated.

Bit4 Reserved

This bit should be set to “0”.

Bit3 DMARQ_Level

Decides the level of operation of the HDMARQ signal. Set “0” when using the IDE interface in IDE bus compatible mode.

DMARQ_Level:1 Negative logic

DMARQ_Level:0 Positive logic

Bit2 Swap

Swaps the higher order 8 bits and lower order 8 bits when using the interface at 16 bits width. The access order to an address of 0x70 of the IDE-CSO Register is reversed.

SWAP:1 Transfers the higher order 8 bit data first.

SWAP:0 Transfers the lower order 8 bit data first.

Bit1::0 Reserved

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x61	IDE_Config1	7: IDE_Reset	R/W	0: None	1: IDE Reset	0x00	0x00	–
		6:		0:	1:			
		5:		0:	1:			
		4:		0:	1:			
		3:		0:	1:			
		2: XDIOW_DLYen	R/W	0: None	1: Delay XDIOW			
		1:		0:	1:			
		0:		0:	1:			

IDE Configuration Register

This register sets the mode of operation of the IDE interface of this IC.

Bit7 IDE_Reset

Writing "1" to this bit asserts the RESET signal to the IDE interface for 50µs. During asserting the XHRESET, this bit reads "1". If you reset it during the assertion, the XHRESET is output for 50µs from that time.

Bit6::3 Reserved

Bit2 XDIOW_DLYen

XDIOW is delayed by one clock (20 ns) as compared with XDMACK on Multiword DMA.

Bit1::0 Reserved

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x62	IDE_RegAccCyc	7: Assert Pulse[3]			0x00	0x00	–
		6: Assert Pulse[2]	R/W	IDE Register Access Strobe Signal Assert Pulse Width Minimum Value			
		5: Assert Pulse[1]					
		4: Assert Pulse[0]					
		3: Negate Pulse[3]					
		2: Negate Pulse[2]	R/W	IDE Register Access Strobe Signal Negate Pulse Width Minimum Value			
		1: Negate Pulse[1]					
		0: Negate Pulse[0]					

IDE Register Access Cycle Register

This register sets a transfer mode when accessing the register area of the IDE interface. It is enabled for an access to 0x70 to 0x7F of the IDE-CS0/CS1 Register.

Bit7::4 Assert Pulse

Decides the minimum value of the assert period of the strobe signal when accessing the register area of the IDE interface. It is a value [Assert Pulse + 2] times the internal operation clock (50MHz) cycle.

Bit3::0 Negate Pulse

Decides the minimum value of the negate period of the strobe signal when accessing the register area of the IDE interface. It is a value [Assert Pulse + 2] times the internal operation clock (50MHz) cycle.

Example: 0000: 2 x 20ns = 40ns

0001: 3 x 20s = 60ns

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x63	IDE_PioDmaCyc	7: Assert Pulse[3] 6: Assert Pulse[2] 5: Assert Pulse[1] 4: Assert Pulse[0]	R/W	IDE Transfer Mode Strobe Signal Assert Pulse Width Minimum Value	0x00	0x00	–
		3: Negate Pulse[3] 2: Negate Pulse[2] 1: Negate Pulse[1] 0: Negate Pulse[0]	R/W	IDE Transfer Mode Strobe Signal Negate Pulse Width Minimum Value			

IDE PIO/DMA Cycle Register

This register sets a transfer mode when transferring data through the IDE interface. It is enabled for an access to 0x70 of the IDE-CSO Register.

It is common to both PIO/DMA modes.

Bit7::4 Asset Pulse

Decides the minimum value of the assert period of the strobe signal when transferring data through the IDE interface. It is a value [Assert Pulse + 2] times the internal operation clock (50MHz) cycle.

Bit3::0 Negate Pulse

Decides the minimum value of the negate period of the strobe signal when transferring data through the IDE interface. It is a value [Assert Pulse + 2] times the internal operation clock (50MHz) cycle.

Example: 0000: 2 x 20ns = 40ns
0001: 3 x 20s = 60ns

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x64	IDE_UltraDmaCyc	7: 6: 5: 4:		0: 0: 0: 0:	1: 1: 1: 1:	0x00	0x00	–
		3: Cycle Time[3] 2: Cycle Time[2] 1: Cycle Time[1] 0: Cycle Time[0]	R/W	IDE Ultra DMA Transfer Mode Strobe Signal Minimum Cycle Time				

IDE UltraDMA Cycle Register

This register sets a transfer mode when transferring data by the Ultra-DMA through the IDE interface.

Bit7::4 Assert Pulse

Decides the minimum value of the assert period of the strobe signal when transferring data through the IDE interface. It is a value [Assert Pulse + 2] times the internal operation clock (50MHz) cycle.

Bit3::0 Cycle Pulse

Decides the minimum cycle time of the strobe signal when transferring Ultra-DMA data through the IDE interface. It is a value [Assert Pulse + 2] times the internal operation clock (50MHz) cycle.

Example: 0000: 2 x 20ns = 40ns
0001: 3 x 20s = 60ns

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x65	IDE_DmaCtl	7:		0:	1:	0x00	0x00	–
		6:		0:	1:			
		5: IncFIFOCnt	W	0: None	1: Push FIFO Data			
		4: CRC_Clear	W	0: None	1: CRC Clear			
		3: FIFO_Clear	W	0: None	1: FIFO Clear			
		2: IDE_Abort	W	0: None	1: IDE Transfer Abort			
		1: IDE_Direction	R/W	0: SRAM –> IDE	1: IDE –> SRAM			
		0: DmaStart	W	0: None	1: IDE DMA Start			

IDE DMA Control Register

This register makes control when transferring data through the IDE interface.

Bit7..6 Reserved

Bit5 IncFIFOCnt

This bit causes FIFO counter increments to dump the data in the FIFO.
If DMA transfer is aborted, the data remained in the FIFO is discharged to the SRAM.
Operation:
1) Wait if FIFOCnt of the IDE_DmaStat register (0x67) is 3'b010 or higher.
2) When FIFOCnt becomes 3'b001, set IncFIFOCnt to 1 unless TxStreamFull of the BufMonitor register is full.
3) Abort the transfer when FIFOCnt becomes 3'b000.

Bit4 CRC_Clear

Initializes the internal CRC calculation circuit. At start-up of the DMA, even the internal circuits are initialized . Writing "1" to this bit clears the IDE_CRC0 and IDE_CRC1 Registers.

Bit3 FIFO_Clear

Clears the FIFO for IDE data transfer. Writing "1" to this bit clears the FIFO.

Bit2 IDE_Abort

Use this bit to abort DMA data transfer in execution through the IDE interface. Writing "1" to this bit aborts the DMA transfer.

Bit1 IDE_Direction

Specifies a data flow direction for DMA data transfer in accordance with the IDE.
IDE_Direction:1 IDE -> SRAM (Buffer)
IDE_Direction:1 IDE <- SRAM (Buffer)

Bit0 DmaStart

Setting this bit to "1" starts DMA transfer between the buffer and the IDE interface.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x66	IDE_BusStat	7: DMARQ	R	Indicate IDE I/F Signals State	0x00	0x00	–
		6: DMACK					
		5: INTRQ					
		4: IORDY					
		3:					
		2:					
		1: DIAG					
		0: DASP					

IDE Bus Status Read Register

This register indicates the status of the signal of the IDE interface.

Bit7 DMARQ

Indicates the state of the HDMARQ signal by positive logic.
(The status of the DMARQ_Level bit of the CONFIG0 is reflected.)

Bit6 DMACK

Indicates the state of the XHDMACK signal by positive logic.

Bit5 INTRQ

Indicates the state of the HINTRQ signal by positive logic.

Bit4 IORDY

Indicates the state of the HIORDY signal by positive logic.

Bit3::2 Reserved

Bit1 DIAG

Indicates the state of the XHPDIAG signal by positive logic.

Bit0 DASP

Indicates the state of the XHDASP signal by positive logic.

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x67	IDE_DmaStat	7: FIFOCnt[2] 6: FIFOCnt[1] 5: FIFOCnt[0]	R R R	Indecate word count in FIFO				
		4: 3: 2:		0: 0: 0:	1: 1: 1:	0x00	0x00	–
		1: DmaPause 0: DmaRun	R R	0: IDE DMA not Pause 0: Not DMA	1: IDE DMA Pause 1: IDE DMA Running			

IDE DMA Status Register

This register indicates the status of the DMA of the IDE interface.

Bit7::5 FIFOCnt[2:0]

This bit indicates the number of words in the FIFO.

Bit4::2 Reserved

Bit1 DmaPause

Indicates whether the DMA mode in execution is in pause status or not. It is enabled when the DmaRun bit is "1".

DmaPause:1 DMA is in pause.

DmaPause:0 DMA is in execution.

Bit0 DmaRun

Indicates whether the DMA mode in execution is in execution or not. It is enabled when the DmaRun bit is "1".

DmaPause:1 DMA is in execution.

DmaPause:0 DMA is not in execution.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x68	IDE_ByteCount0	7: ByteCount[31] 6: ByteCount[30] 5: ByteCount[29] 4: ByteCount[28] 3: ByteCount[27] 2: ByteCount[26] 1: ByteCount[25] 0: ByteCount[24]	R/W	IDE Data Transfer Byte Count Register Read: Indicate Remain Byte Count Write: Set Total Transfer Byte Count	0x00	0x00	–
0x69	IDE_ByteCount1	7: ByteCount[23] 6: ByteCount[22] 5: ByteCount[21] 4: ByteCount[20] 3: ByteCount[19] 2: ByteCount[18] 1: ByteCount[17] 0: ByteCount[16]			0x00	0x00	–
0x6A	IDE_ByteCount2	7: ByteCount[15] 6: ByteCount[14] 5: ByteCount[13] 4: ByteCount[12] 3: ByteCount[11] 2: ByteCount[10] 1: ByteCount[9] 0: ByteCount[8]			0x00	0x00	–
0x6B	IDE_ByteCount3	7: ByteCount[7] 6: ByteCount[6] 5: ByteCount[5] 4: ByteCount[4] 3: ByteCount[3] 2: ByteCount[2] 1: ByteCount[1] 0: ByteCount[0]			0x00	0x00	–

IDE Byte Count Set Register

This register sets a total data length in DMA transfer in the unit of byte. By setting each register of IDE_ByteCount0 to 3, setting up to max. 0xFFFFFFFF is possible.

If you set an odd byte to this register or the OddStart bit of the CONFIG0 Register when using the data port of the IDE bus based on word size, 1 byte is short at the first or last transfer. It is automatically padded by the IC (data is undefined).

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x6C	IDE_CRC0	7: CRC[15] 6: CRC[14] 5: CRC[13] 4: CRC[12] 3: CRC[11] 2: CRC[10] 1: CRC[9] 0: CRC[8]	R	IDE CRC Data Register	0x00	0x00	–
0x6D	IDE_CRC1	7: CRC[7] 6: CRC[6] 5: CRC[5] 4: CRC[4] 3: CRC[3] 2: CRC[2] 1: CRC[1] 0: CRC[0]			0x00	0x00	–

CRC Read Register

This register indicates CRC calculation results when transferring data by the Ultra-DMA through the IDE interface.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x70	IDE_CS00	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Data Register	0x00	0x00	–
0x71	IDE_CS01	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Read : Error Register Write: Features Register	0x00	0x00	–
0x72	IDE_CS02	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Sector Count Register	0x00	0x00	–
0x73	IDE_CS03	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Sector Number Register or Logical Block Address(LBA) bit 0 – 7	0x00	0x00	–
0x74	IDE_CS04	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Cylinder Low Register or Logical Block Address(LBA) bit 8 – 15	0x00	0x00	–
0x75	IDE_CS05	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Cylinder High Register or Logical Block Address(LBA) bit 16 – 23	0x00	0x00	–
0x76	IDE_CS06	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Device/Head Register 0x00 Logical Block Address(LBA) bit 24 – 27	0x00	0x00	–
0x77	IDE_CS07	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Command Block Register Read : Status Register 0x00 Write: Command Register	0x00	0x00	–

IDE Command Block Register

This register is a Command Block Register that is the I/O port of the IDE interface.
The transfer mode of the Data Register is PIO mode-fixed, having access based on conditions set on the IDE_PioDmaCyc Register. Since the setting at the BUS8/SWAP bit of the CONFIG Register is reflected, 16-bit access is possible by always accessing the Data Register twice if it is 16 bits wide.
During DMA transfer, access to the Data Register is disabled.
If you access the 0x71-0x77 in the DMA mode or when the InterLock bit is not on, the HDMARQ is negated once and CPU access is done.
When the Interlock bit is on or at the time of UltraDMA, the XHDMACK is negated at the time of HDMAQR off or on completion of transfer. Note that, for this reason, the CPU access is put in wait state.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x78	IDE_CS10	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x79	IDE_CS11	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7A	IDE_CS12	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7B	IDE_CS13	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7C	IDE_CS14	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7D	IDE_CS15	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Data Bus Hi – Impedance Write: Not Used	0x00	0x00	–
0x7E	IDE_CS16	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : Alternate Status Write: Device Control	0x00	0x00	–
0x7F	IDE_CS17	7: 6: 5: 4: 3: 2: 1: 0:	R/W	Control Block Register Read : (obsolete) Write: Not Used	0x00	0x00	–

IDE Command Control Register

This register is a Command Block Register that is the I/O port of the IDE interface.

8.2 FLASH ROM CONTROL REGISTER

Address	Register Name	Bit Symbol	R/W	Description		H.Rst	S.Rst	B.Rst
0x200000	FlashCtl	7: FlashCtlEnb	R/W	0: Flash Control Disable	1: Flash Control Enable			
		6:		0:	1:			
		5:		0:	1:			
		4: Erase	W	0: None	1: Erase Execute	0x00	0x00	–
		3: FlashStat	R	0: Write/Erase Complete	1: Write/Erase Run			
		2: FlashChipErs	R/W	0: Chip All Erase Disable	1: Chip All Erase Enable			
		1: FlashSctErs	R/W	0: Sector Erase Disable	1: Sector Erase Enable			
		0: FlashWrEnb	R/W	0: Flash Data Write Disable	1: Flash Data Write Enable			

Flash Control Register

This register controls the erase and write of the built-in Flash.

Bit7 FlashCtlEnb

Enables Flash control.

Setting this bit to “1” enables the lower order 5 bits of this register. Setting “0” disables having access to the built-in Flash.

Bit6 Reserved

Bit5 Reserved

Bit4 Erase

Setting this bit to “1” starts to erase the built-in Flash. This bit is read-only. If you read it, it always indicates zero.

Setting this bit to “1” at the time of FlashSctErs=1, the Flash Address is updated after erasing one sector.

Bit3 FlashStat

Indicates the operation of Write/Erase.

“1”: In execution

“0”: Processing finishes.

Bit2 FlashChipErs

Use this bit to erase all the built-in Flash.

“1”: All Erase is enabled..

“0”: All Erase is disabled.

Bit1 FlashSctErs

Use this bit to erase the built-in Flash in the unit of sector. It enables the erase of the sector address set on the Flash Address.

“1”: Sector Erase is enabled..

“0”: Sector Erase is disabled.

Bit1 FlashWREnb

Enables Data Write into the built-in Flash.

“1”: Data Write is enabled..

“0”: Data Write is disabled.

Sequence to set a default value on FlashCtlCnt_reg

Turn on one of Bit0, Bit1 or Bit2 to select a desired operation.

Next, turn on bit7.

Sequence to set a value on FlashCtlCnt_reg

Turn on Bit7 and one of Bit0, Bit1 and Bit2.

Next, set a value on the FlashCtlCnt_reg.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x200001	FlashCtlCnt_H	7: 6:		0: 0: 1:			

		5: FlashCtlCnt[21]
		4: FlashCtlCnt[20]
		3: FlashCtlCnt[19]
		2: FlashCtlCnt[18]
		1: FlashCtlCnt[17]
		0: FlashCtlCnt[16]
				IF(FlashChipErs==1 && FlashSctErs==0 && FlashWrEnb==0){
				R/W Enable;
				Default Value = 0x3FFFFF;
				}
					0x00	0x00	–

0x200002	FlashCtlCnt_M	7: FlashCtlCnt[15]
		6: FlashCtlCnt[14]
		5: FlashCtlCnt[13]
		4: FlashCtlCnt[12]
		3: FlashCtlCnt[11]
		2: FlashCtlCnt[10]
		1: FlashCtlCnt[9]
		0: FlashCtlCnt[8]
			R/W	erase if(FlashChipErs==0 && FlashSctErs==1 && FlashWrEnb==0){
				R/W Enable;
				Default Value = 0x0FFFFF;
				}
				erase if(FlashChipErs==0 && FlashSctErs==0 && FlashWrEnb==1){
				R/W Enable;
				Default Value = 0x000190;
				} else {
				Read is alway Zero;
				Write is Ignore;
				}
					0x00	0x00	–

0x200003	FlashCtlCnt_L	7: FlashCtlCnt[7] 6: FlashCtlCnt[6] 5: FlashCtlCnt[5] 4: FlashCtlCnt[4] 3: FlashCtlCnt[3] 2: FlashCtlCnt[2] 1: FlashCtlCnt[1] 0: FlashCtlCnt[0]			0x00	0x00	–

Flash Control Count Register

This register is enabled when the FlashChipErs bit, FlashSctErs bit or FlashWrEnb bit of the FlashCtl Register is set alone. It is disabled when two or more bits are set.

When setting them in the unit of byte, conform to the order of FlashCtlCnt_H (higher order byte), FlashCtlCnt_M, and FlashCtlCnt_L (lower order byte). On completion of writing to the lower order byte, setting of this register is enabled.

Pulse width (Default value)

FlashChipErs: 40ns x 0x3FFFFF = 167.8ms

FlashSctErs: 40ns x 0x0FFFFF = 41.9ms

FlashWrEnb: 40ns x 0x000190 = 16.0μs

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x200004	FlashAdrs_H	7: Flash Address[15]	R/W	Write: Flash Write/Erase Sector Address Set Read: Current Flash Sector Address When All of Sector are erased, This Address is Ignored. When Data register's Low Byte is accessed, This Register is updated.	0x00	0x00	–
		6: Flash Address[14]					
		5: Flash Address[13]					
		4: Flash Address[12]					
		3: Flash Address[11]					
		2: Flash Address[10]					
		1: Flash Address[9]					
		0: Flash Address[8]					
0x200005	FlashAdrs_M	7: Flash Address[7]			0x00	0x00	–
		6: Flash Address[6]					
		5: Flash Address[5]					
		4: Flash Address[4]					
		3: Flash Address[3]					
		2: Flash Address[2]					
		1: Flash Address[1]					
		0:		Reserved(Always Zero)			

Flash Address Register

This register specifies a write/erase address of the built-in Flash.
In the Built-in Flash All Erase mode, the setting of this register is ignored.
During writing operation, writing to the lower order byte of the Flash Data Register increments the address of this register.

Address	Register Name	Bit Symbol	R/W	Description	H.Rst	S.Rst	B.Rst
0x200006	FlashData_H	7: Flash Address[15]	R/W	Write: Flash Write Data Set Read: Flash Address's Word Data is read. When operation is Write, It shall be set from high byte. Because when Data register's Low Byte is accessed, Flash Address is updated.	0x00	0x00	–
		6: Flash Address[14]					
		5: Flash Address[13]					
		4: Flash Address[12]					
		3: Flash Address[11]					
		2: Flash Address[10]					
		1: Flash Address[9]					
		0: Flash Address[8]					
0x200007	FlashData_L	7: Flash Address[7]			0x00	0x00	–
		6: Flash Address[6]					
		5: Flash Address[5]					
		4: Flash Address[4]					
		3: Flash Address[3]					
		2: Flash Address[2]					
		1: Flash Address[1]					
		0: Flash Address[0]					

Flash Write Data Register

This register specifies write data of the built-in Flash.
When setting it in the unit of byte, conform to the order of higher order byte - lower order byte. If you reverse the order, data cannot be correctly written.
Writing to the lower order byte updates the Flash Address Register to the next write address.

9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	HV_{DD}	–0.3 to 7.0	V
	LV_{DD}	–0.3 to 4.0	V
Input voltage	HV_{IN}	–0.3 to HV_{DD} + 0.5	V
	LV_{IN}	–0.3 to LV_{DD} + 0.5	V
Output voltage	HV_{OUT}	–0.3 to HV_{DD} + 0.5	V
	LV_{OUT}	–0.3 to LV_{DD} + 0.5	V
Output current/pin	I_{OUT}	–30	mA
Storage temperature	T_{STG}	–65 to 150	°C

9.2 RECOMMENDED OPERATING CONDITION

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	HV_{DD}	4.5	5	5.5	V
	LV_{DD}	3	3.3	3.6	V
Input voltage	HV_{IN}	V_{SS}	–	HV_{DD}	V
	LV_{IN}	V_{SS}	–	LV_{DD}	V
Operating temperature	TOPr1	0	–	70	°C
Operating temperature when writing to FLASH ROM	TOPr2	0	–	70	°C

9.3 DC CHARACTERISTICS (ACCORDING TO RECOMMENDED OPERATING CONDITION) (1)

(HV_{DD} = 5.0V ± 0.5V, LV_{DD} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current						
Power supply current	I_{DD}	HV_{DD} =5.5V LV_{DD} =3.6V	–	–	150	mA
Static current (Static current between HV_{DD} to V_{SS})						
Power supply current	I_{DDSH}	V_{IN} =HV_{DD} or LV_{DD} or V_{SS} HV_{DD} =5.5V LV_{DD} =3.6V	–	–	45	µA
Static current (Static current between LV_{DD} to V_{SS})						
Power supply current	I_{DDSL}	V_{IN} =HV_{DD} or LV_{DD} or V_{SS} HV_{DD} =5.5V LV_{DD} =3.6V	–	–	107	µA
Input leak						
Input leak current	I_L	HV_{DD} =5.5V LV_{DD} =3.6V HV_{IH} =HV_{DD} LV_{IH} =LV_{DD} V_{IL} =V_{SS}	–1	–	1	µA
Input characteristics (CMOS)						
HIGH level input voltage	V_{IH1H}	HV_{DD} =5.5V	3.5	–	–	V
LOW level input voltage	V_{IL1H}	HV_{DD} =4.5V	–	–	1	V
Input characteristics (TTL)						
HIGH level input voltage	V_{IH2H}	HV_{DD} =5.5V	2	–	–	V
LOW level input voltage	V_{IL2H}	HV_{DD} =4.5V	–	–	0.8	V
Input characteristics (CMOS)						
HIGH level input voltage	V_{IH1L}	HV_{DD} =3.6V	2	–	–	V
LOW level input voltage	V_{IL1L}	HV_{DD} =3.0V	–	–	0.8	V
Schmitt input characteristics (TTL)						
HIGH level trigger voltage	V_{T2+}	HV_{DD} =5.5V LV_{DD} =3.6V	1.2	–	2.4	V
LOW level trigger voltage	V_{T2-}	HV_{DD} =4.5V LV_{DD} =3.0V	0.6	–	1,8	V
Hysteresis voltage	dV_2	HV_{DD} =4.5V LV_{DD} =3.0V	0.1	–	–	V

DC CHARACTERISTICS (ACCORDING TO RECOMMENDED OPERATING CONDITION) (2)

(HV_{DD} = 5.0V ± 0.5V, LV_{DD} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output characteristics		Pin name: CTL0, CTL1, D0..D07, LREQ, LPS, PD				
LOW level output voltage	V_{OL2}	LV_{DD} =3.0V I_{OL} =–6.0mA	–	–	V_{SS}+0.4	V
HIGH level output voltage	V_{OH2}	LV_{DD} =3.0V I_{OH} =6.0mA	V_{SS}–0.4	–	–	V
Output characteristics		Pin name: CTL0, CTL1, D0.. D7				
OFF-STATE leak current	I_{OZ}	HV_{DD} =5.5V LV_{DD} =3.6V HV_{OH} =HV_{DD} LV_{OH} =LV_{DD} V_{OL} =V_{SS}	–1	–	1	µA
Input characteristics (Bus hold)		Pin name: LINKON, SCLK, CTL0, CTL1, D0..D7, T18				
LOW level HOLD current	I_{BHL}	LV_{DD} =3.0V V_{BHL} =0.4V	–	–	0.3	mA
HIGH level HOLD current	I_{BHH}	LV_{DD} =3.0V V_{BHH} =2.6V	–0.3	–	–	mA
Output characteristics (Bus drive)		Pin name: LINKON, SCLK, CTL0, CTL1, D0..D7, T18				
LOW level output voltage	V_{BHL}	LV_{DD} =3.6V I_{BHL} =0.9mA	L_{VDD}–0.4	–	–	V
HIGH level output voltage	V_{BHH}	LV_{DD} =3.6V I_{BHH} =–0.9mA	–	–	V_{SS}+0.4	V

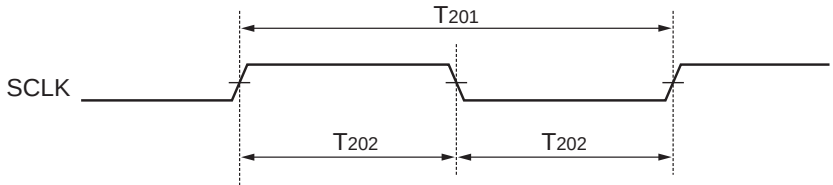
(HV_{DD} = 5.0V ± 0.5V, LV_{DD} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output characteristics		Pin name: XHCS1, XHCS0, HDA2, HDA1, HDA0, XHPDIAG, HINTRQ, XHDMACK, HIORDY, XHIOR, XHIOW, HDMARQ, HDD15...0, XHRST				
HIGH level output voltage	LV_{OH1}	LV_{DD} =3.0V I_{OH} =–2mA	LV_{DD} –0.4	–	–	V
LOW level output voltage	LV_{OL1}	LV_{DD} =3.0V I_{OL} =2mA	–	–	V_{SS}+0.4	V

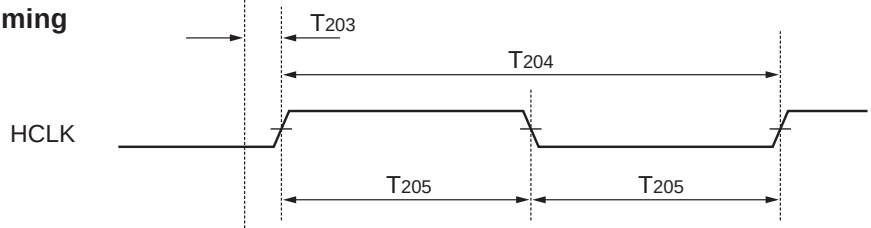
9.4 AC CHARACTERISTICS

9.4.1 Clock Timing

9.4.1.1 SCLK Timing



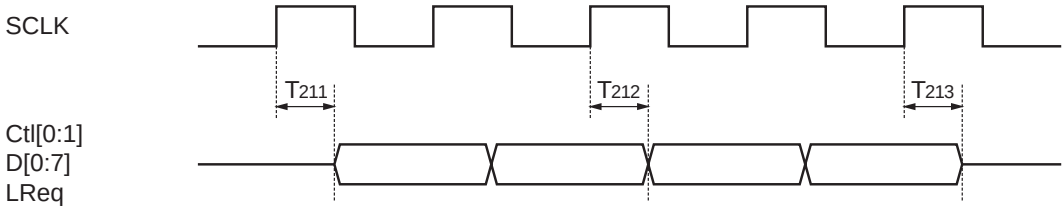
9.4.1.2 HCLK Timing



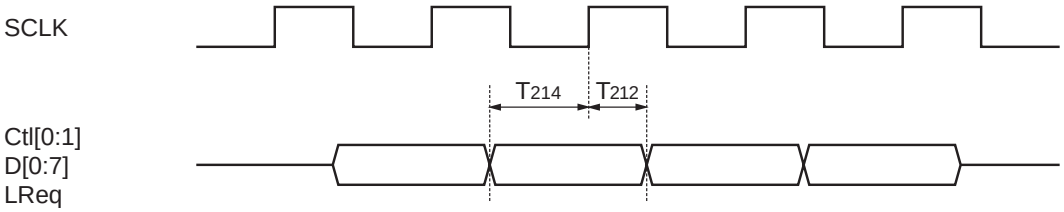
Symbol	Description	Unit	Min.	Max.
T_{201}	SCLK frequency	49.152MHz ± 100ppm		
T_{202}	SCLK duty cycle	%	45	55
T_{203}	SCLK start → HCLK start delay time	ns	5	15
T_{204}	HCLK frequency	MHz	20	24.576
T_{205}	HCLK duty cycle	%	40	60

9.4.2 PHY-LINK Interface Timing

9.4.2.1 Output timing



9.4.2.2 Input timing



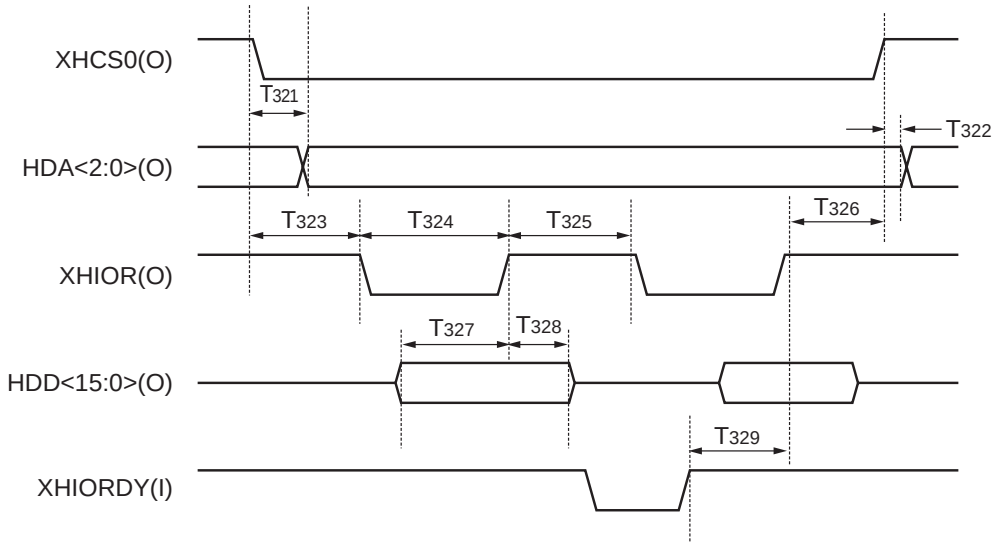
Symbol	Description	Unit	Min.	Max.
T211	SCLK rising edge → C, Ctl, LReq delay time (Hi-Z → Output starts.)	ns	1	10
T212	SCLK rising edge → C, Ctl, LReq delay time (Outputting)	ns	1	10
T213	SCLK rising edge → C, Ctl, LReq delay time (When output ends.)	ns	1	10

Symbol	Description	Unit	Min.	Max.
T214	SCLK rising edge → C, Ctl set-up time	ns	6	
T215	SCLK rising edge → C, Ctl hold time	ns	0	

9.4.3 IDE Interface Timing

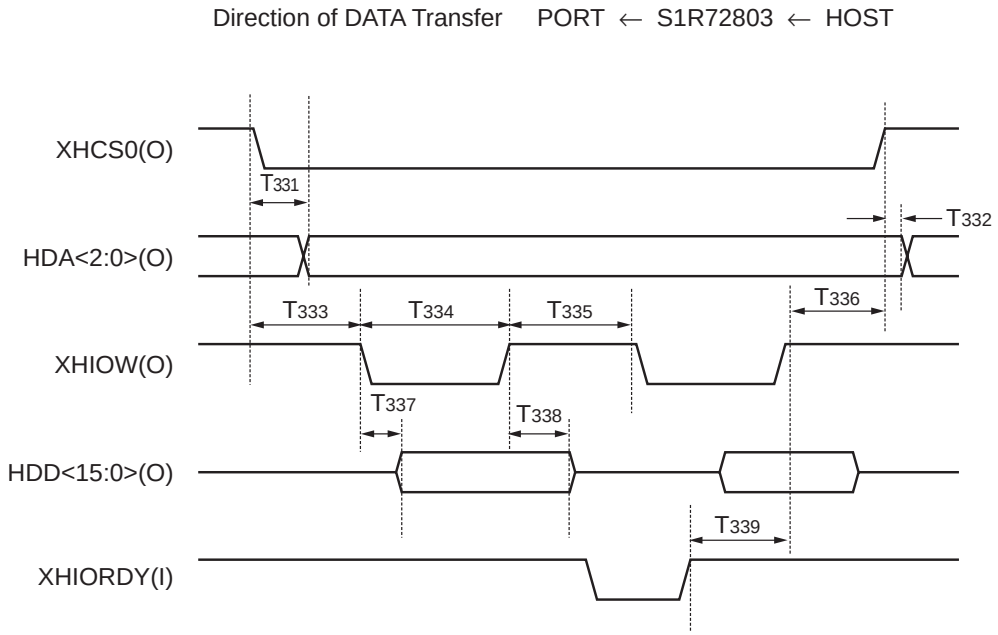
9.4.3.1 PIO Read

Direction of DATA Transfer PORT → S1R72803 → HOST



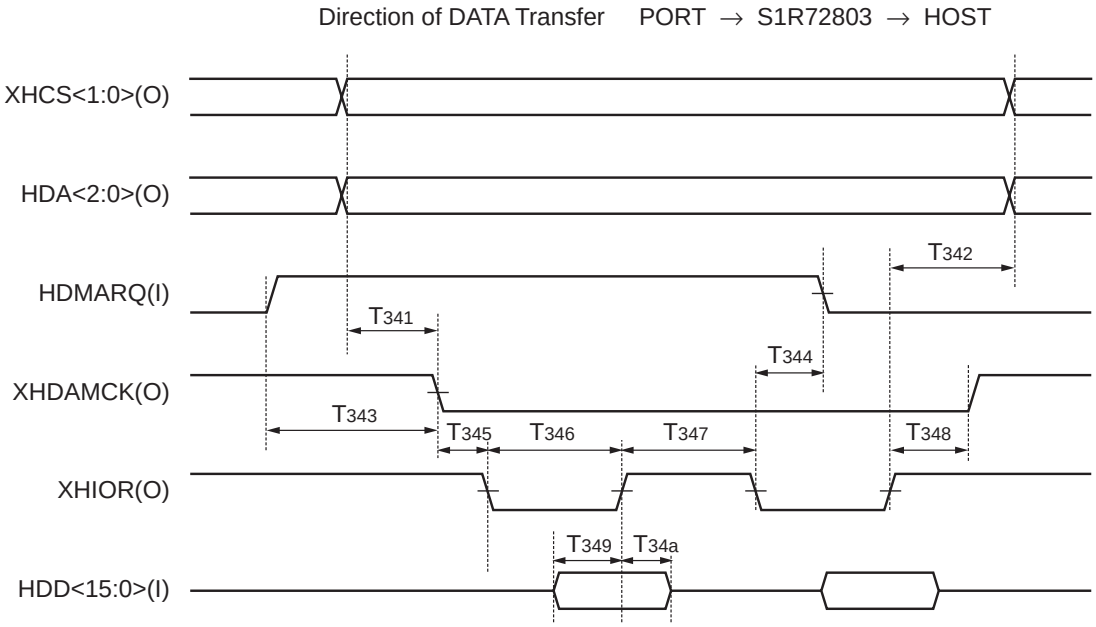
Symbol	Specification	Min.	Typ.	Max.	Unit
T321	XHCS0 ↓→ HDA HDA output delay time	–	0	–	ns
T322	XHCS0 ↑→ HDA HDA hold time	–	0	–	ns
T323	XHCS0 ↓→ XHIOR ↓ XHIOR set-up time	60	–	–	ns
T324	XHIOR ↓→ XHIOR ↑ XHIOR assert pulse time	–	IDEPIO (AP+2)×20	–	ns
T325	XHIOR ↑→ XHIOR ↓ XHIOR negate pulse time	–	IDEPIO (NP+2)×20	–	ns
T326	XHIOR ↑→ XHCS0 ↑ XHIOR hold time	20	–	–	ns
T327	HDD→ XHIOR ↑ Data set-up time	10	–	–	ns
T328	XHIOR ↑→ HDD Data hold time	0	–	–	ns
T329	HIORDY assert → XHIOR ↑ XHDMACK set-up time	–	–	40	ns

9.4.3.2 PIO Write



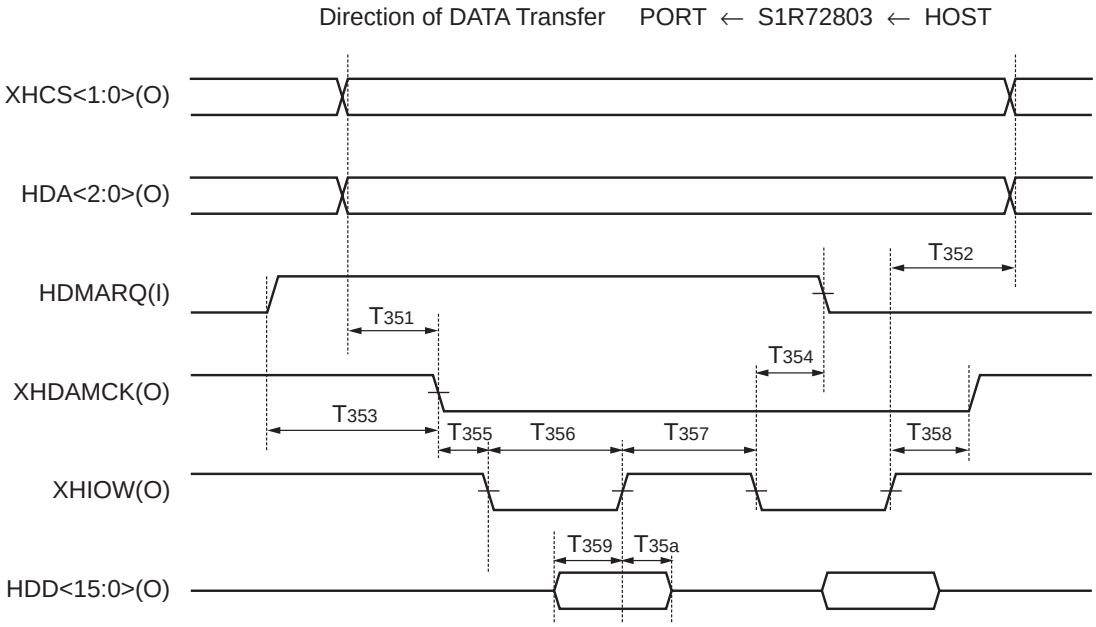
Symbol	Specification	Min.	Typ.	Max.	Unit
T331	XHCS0 ↓→ HDA HDA output delay time	–	0	–	ns
T332	XHCS0 ↑→ HDA HDA hold time	–	0	–	ns
T333	XHCS0 ↓→ XHIOW ↓ XHIOW set-up time	60	–	–	ns
T334	XHIOW ↓→ XHIOW ↑ XHIOW assert pulse width	–	IDEPIO (AP+2)×20	–	ns
T335	XHIOW ↑→ XHIOW ↓ XHIOW negate pulse width	–	IDEPIO (NP+2)×20	–	ns
T336	XHIOW ↑→ XHCS0 ↑ XHIOW hold time	20	–	–	ns
T337	XHIOW ↓→ HDD Data output delay time	0	–	20	ns
T338	XHIOW ↑→ HDD Data bus negate time	40	–	60	ns
T339	HIORDY assert → XHIOW ↑ XHDMACK set-up time	–	–	40	ns

9.4.3.3 DMA Read



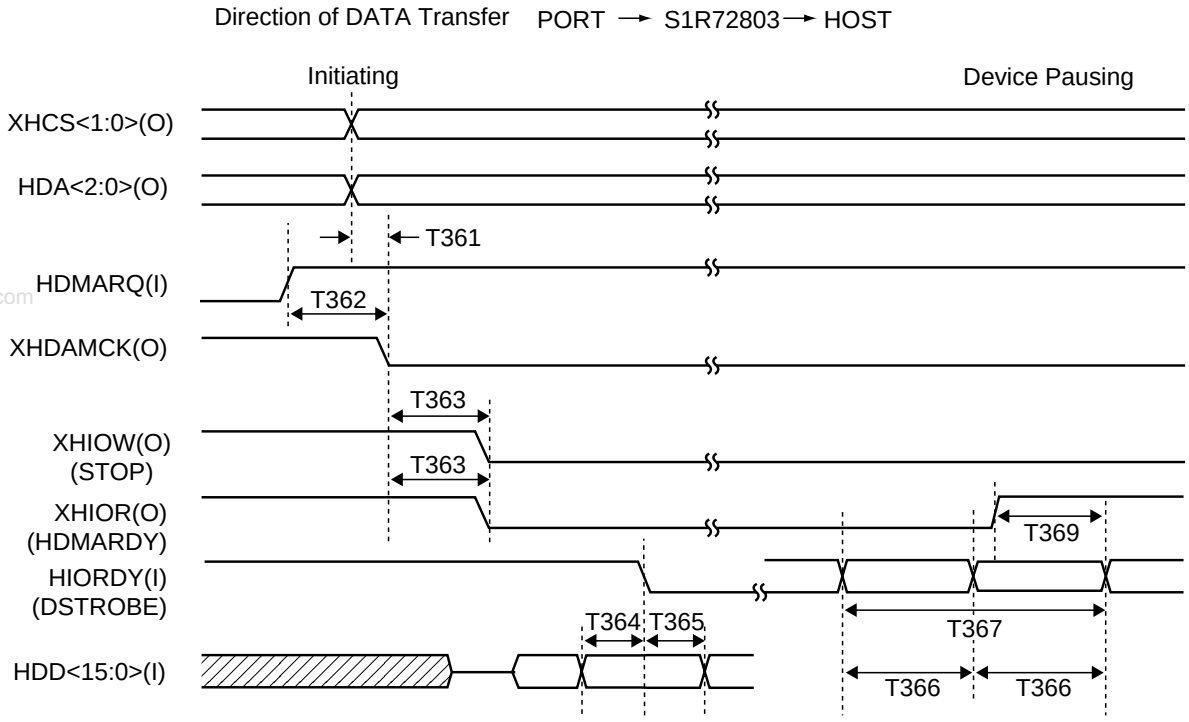
Symbol	Specification	Min.	Typ.	Max.	Unit
T_{341}	XHCS0,1 ↑→ XHDMACK ↓ Address set-up time	60	–	–	ns
T_{342}	XHIOR ↑→ XHCS0,1 ↓ Address hold time	25	–	–	ns
T_{343}	HDMARQ ↑→ XHDMACK ↓ XHDMACK response time	0	–	–	ns
T_{344}	XHIOR ↓→ HDMARQ negate HDMARQ hold time	0	–	–	ns
T_{345}	XHDMACK ↓→ XHIOR ↓ XHIOR set-up time	0	–	–	ns
T_{346}	XHIOR ↓→ XHIOR ↑ XHIOR assert pulse width	–	IDE (AP+2)×20	–	ns
T_{347}	XHIOR ↑→ XHIOR ↓ XHIOR negate pulse width	–	IDE (AP+2)×20	–	ns
T_{348}	XHIOR ↑→ XHDMACK ↑ XHIOR hold time	20	–	–	ns
T_{349}	HDD→ XHIOR ↑ Data set-up time	10	–	–	ns
T_{34a}	XHIOR ↑→ HDD Data bus hold time	0	–	–	ns

9.4.3.4 DMA Write

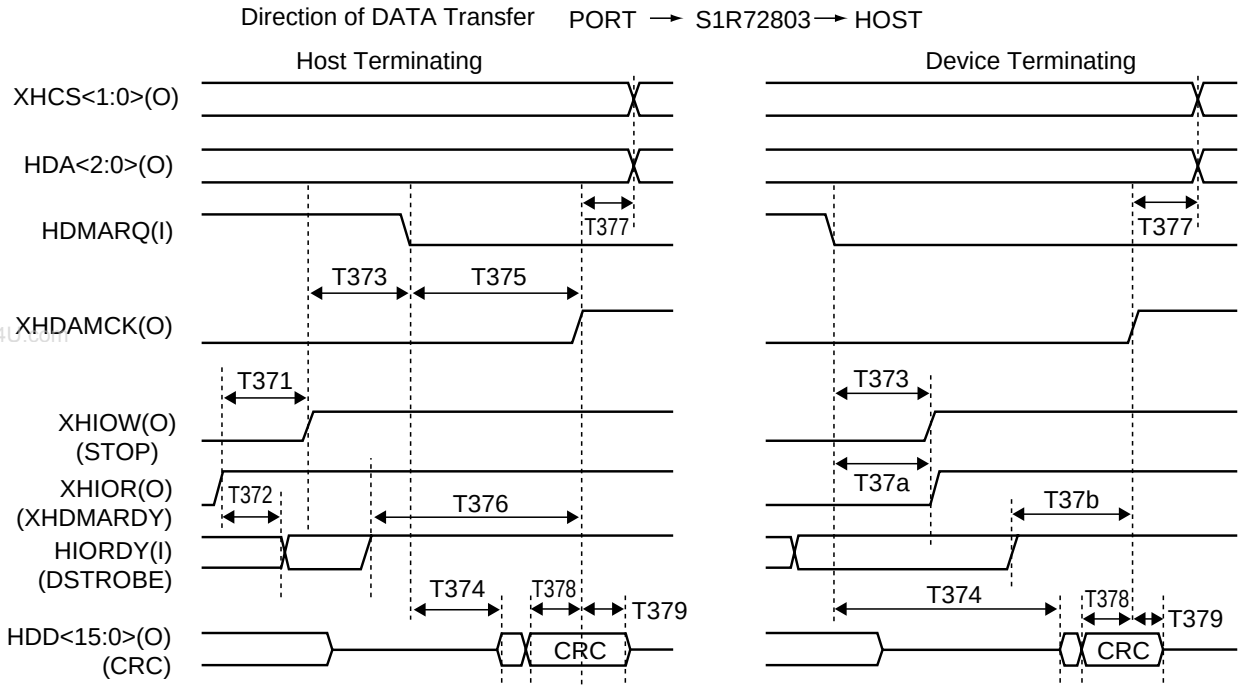


Symbol	Specification	Min.	Typ.	Max.	Unit
T_{351}	XHCS0,1 ↑→ XHDMACK ↓ Address set-up time	60	–	–	ns
T_{352}	XHIOW ↑→ XHCS0,1 ↓ Address hold time	20	–	–	ns
T_{353}	HDMARQ ↑→ XHDMACK ↓ XHDMACK response time	0	–	–	ns
T_{354}	XHIOW ↓→ HDMARQ negate HDMARQ hold time	0	–	–	ns
T_{355}	XHDMACK ↓→ XHIOW ↓ XHIOR set-up time	0	–	–	ns
T_{356}	XHIOW ↓→ XHIOW ↑ XHIOW assert pulse width	–	IDE (AP+2)×20	–	ns
T_{357}	XHIOW ↑→ XHIOW ↓ XHIOW negate pulse width	–	IDE (AP+2)×20	–	ns
T_{358}	XHIOW ↑→ XHDMACK ↑ XHIOW hold time	20	–	–	ns
T_{359}	XHIOW ↓→ HDD Data output delay time	0	–	20	ns
T_{35a}	XHIOR ↑→ HDD Data bus negate time	20	–	40	ns

9.4.3.5 Ultra-DMA Read

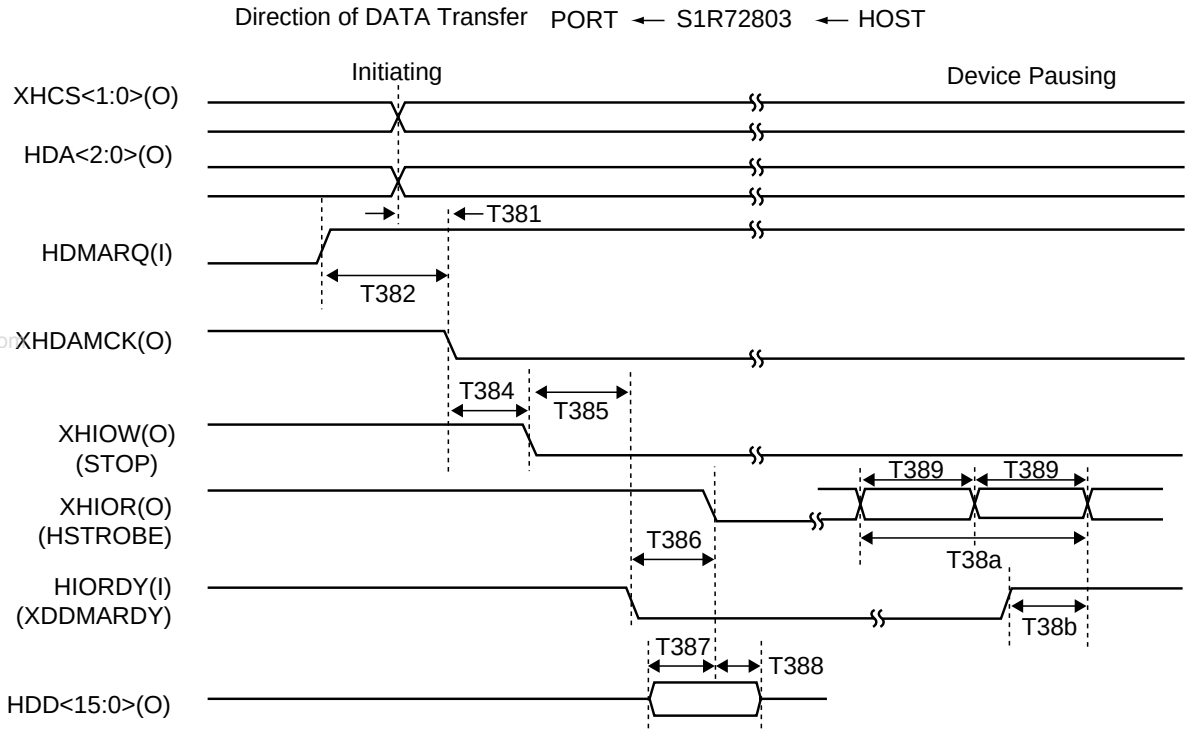


Symbol	Specification	Min.	Typ.	Max.	Unit
T_{361}	XHCS0,1 ↑→ XHDMACK ↓ Address setup time	20	–	–	ns
T_{362}	HDMARQ ↑→ XHDMACK ↓ XHDMACK response time	0	–	–	ns
T_{363}	HDMACK ↓→ HIOR,XHIOW↑ Envelope time	20	–	55	ns
T_{364}	HDD→HIORDY Data setup time	6	–	–	ns
T_{365}	HIORDY → HDD Data hold time	6	–	–	ns
T_{366}	HIORDY → HIORDY HIORDY cycle time	25	–	–	ns
T_{367}	HIORDY → HIORDY HIORDY cycle time x 2	57	–	–	ns
T_{369}	XHIOR ↑→ HIORDY Last strobe time	–	–	60	ns

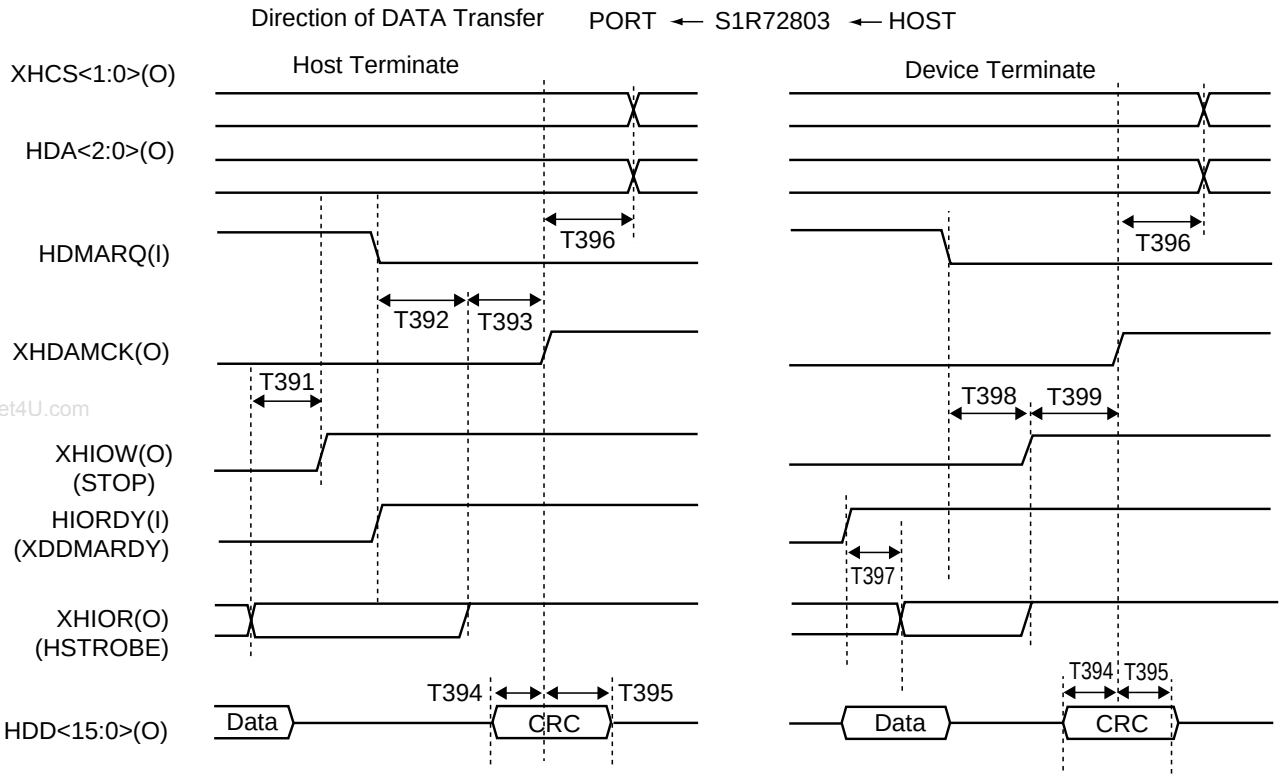


Symbol	Specification	Min.	Typ.	Max.	Unit
T_{371}	XHIOR ↓→ XHIOW ↑ Time before STOP is asserted	100	–	–	ns
T_{372}	XHIOR ↓→ HIORDY Last strobe time	–	–	60	ns
T_{373}	XHIOW ↑→HDMARQ ↓ Constrained interlock time	0	–	100	ns
T_{374}	HDMARQ ↓→HDD Output delay time	20	–	–	ns
T_{375}	HDMARQ ↓→HDMACK ↓ Minimum interlock time	20	–	–	ns
T_{376}	HIORDY→ HDMACK Minimum interlock time	20	–	–	ns
T_{377}	XHDMACK ↓→ XHCS0,1 XHDMACK hold time	20	–	–	ns
T_{378}	HDD(CRC)→ HDMACK ↑ CRC data setup time	6	–	–	ns
T_{379}	HDMACK ↑→ HDD(CRC) CRC data hold time	6	–	–	ns
T_{37a}	HDMARQ ↑→XHIOR ↓ Constrained interlock time	0	–	100	ns
T_{37b}	HIORDY→ HDMACK Minimum interlock time	20	–	–	ns

9.4.3.6 Ultra-DMA Write



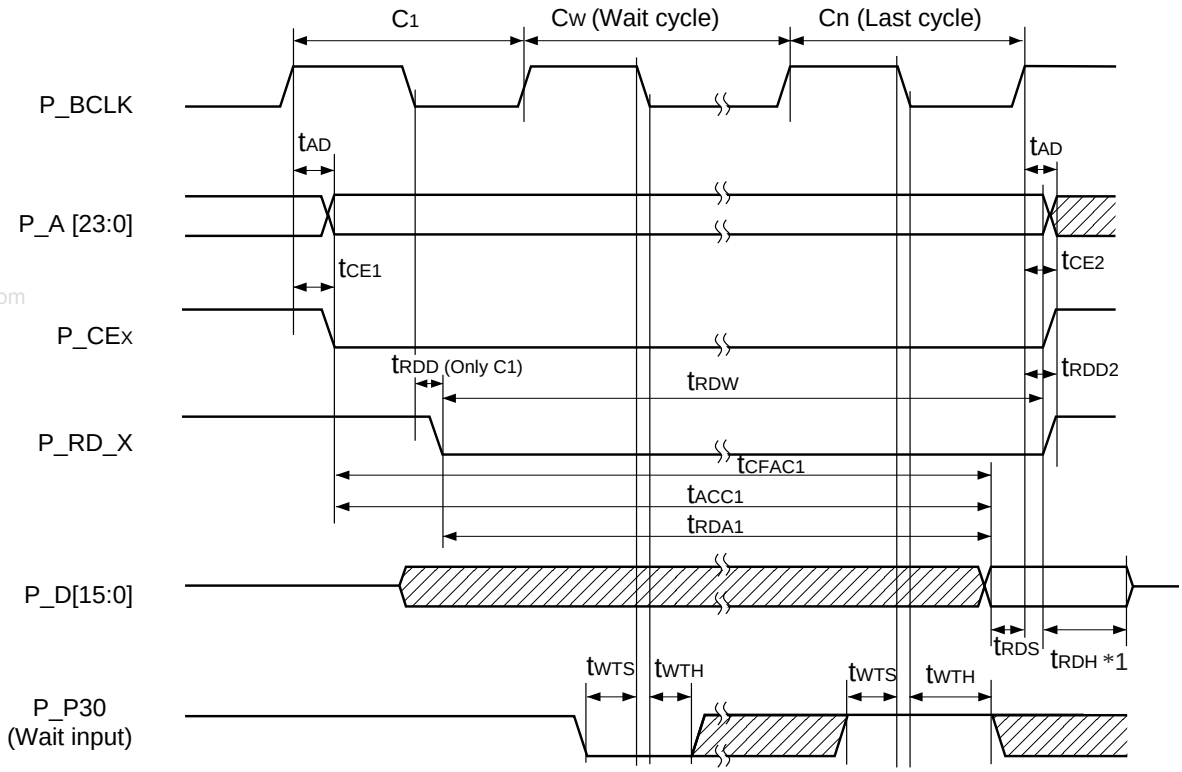
Symbol	Specification	Min.	Typ.	Max.	Unit
T_{381}	XHCS0,1 ↑→XHDMACK ↓ Address setup time	20	–	–	ns
T_{382}	HDMARQ ↑→XHDMACK ↓ XHDMACK response time	0	–	–	ns
T_{384}	HDMACK ↓→HIORDY,XHIOW ↑ Envelope time	20	–	40	ns
T_{385}	XHIOW ↓→XHIOR Constrained interlock time	0	–	100	ns
T_{386}	XHIOR → HIORDY ↓ Unconstrained interlock time	0	–	–	ns
T_{387}	HDD → XHIOR Data setup time	6	–	–	ns
T_{388}	XHIOR → HDD Data hold time	6	–	–	ns
T_{389}	XHIOR → XHIOR XHIOR cycle time	25	–	–	ns
T_{38a}	XHIOR → XHIOR XHIOR cycle time x 2	57	–	–	ns
T_{38b}	HIORDY↑→ XHIOR Last strobe time	–	–	60	ns



Symbol	Specification	Min.	Typ.	Max.	Unit
T_{391}	XHIOR → XHIOW ↑ Strobe stop time	50	–	–	ns
T_{392}	HDMARQ ↓→ XHIOR OFF Constrained interlock time	0	–	100	ns
T_{393}	XHIOR ↑ XHDMACK ↑ Mimimum interlock time	20	–	–	ns
T_{394}	HDD(CRC) →XHDMACK ↑ CRC data setup time	6	–	–	ns
T_{395}	XHDMACK ↑→ HDD(CRC) CRC data hold time	6	–	–	ns
T_{396}	XHDMACK ↑→XHCS0,1 XHDMACK hold time	20	–	–	ns
T_{397}	HIORDY ↑→XHIOR Last strobe time	–	–	60	ns
T_{398}	HDMAQ ↓→ XHIOW Constrained interlock time	0	–	100	ns
T_{399}	XHIOW ↑→ XHDMACK ↑ Minimum interlock time	20	–	–	ns

9.4.4 CPU Interface Timing

9.4.4.1 CPU Read Cycle

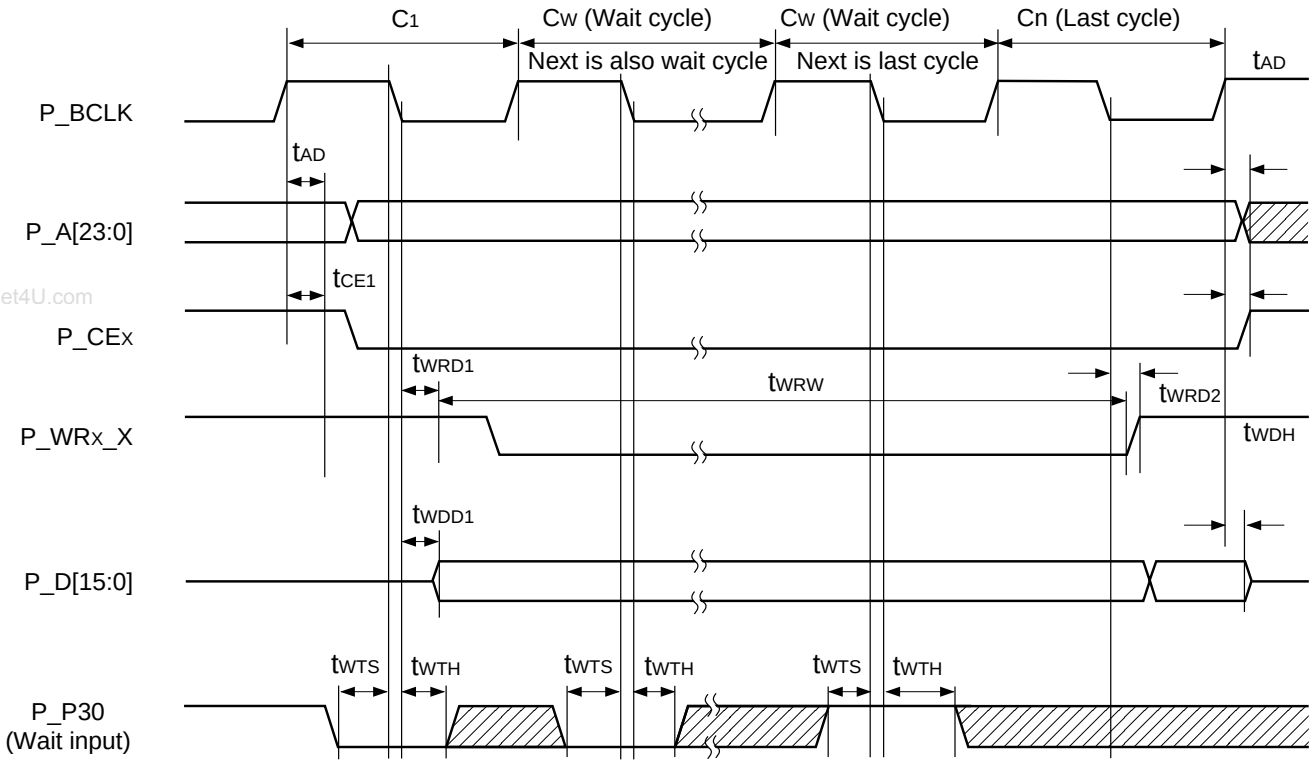


*1 tRDH is formulated according to the earliest signal change (Negate) among P_RD, P_CEx, P_A[23:0]

Symbol	Specification	Min.	Max.	Unit
tAD	Address delay time	–	8	ns
tCE1	P_CEx delay time (1)	–	8	ns
tCE2	P_CEx delay time (2)	–	8	ns
tWTS	Wait set-up time	29	–	ns
tWTH	Wait hold time	0	–	ns
tRDD1	Read signal delay time (1)	–	8	ns
tRDS	Read data set-up time	24	–	ns
tRDH	Read data hold time	0	–	ns
tRDD2	Read signal delay time (2)	–	8	ns
tRDW	Read signal pulse width	tCYC(0.5+WC)–8	–	ns
tACC1	Read address access time (1)	–	tCYC(1+WC)–20	ns
tCEAC1	Chip enable access time (1)	–	tCYC(1+WC)–20	ns
tRDAC1	Read signal access time (1)	–	tCYC(0.5+WC)–20	ns

* tCYC=40ns when bus clock is 25MHz in X2 mode.
* WC: Wait cycle signal

9.4.4.2 CPU Write Cycle

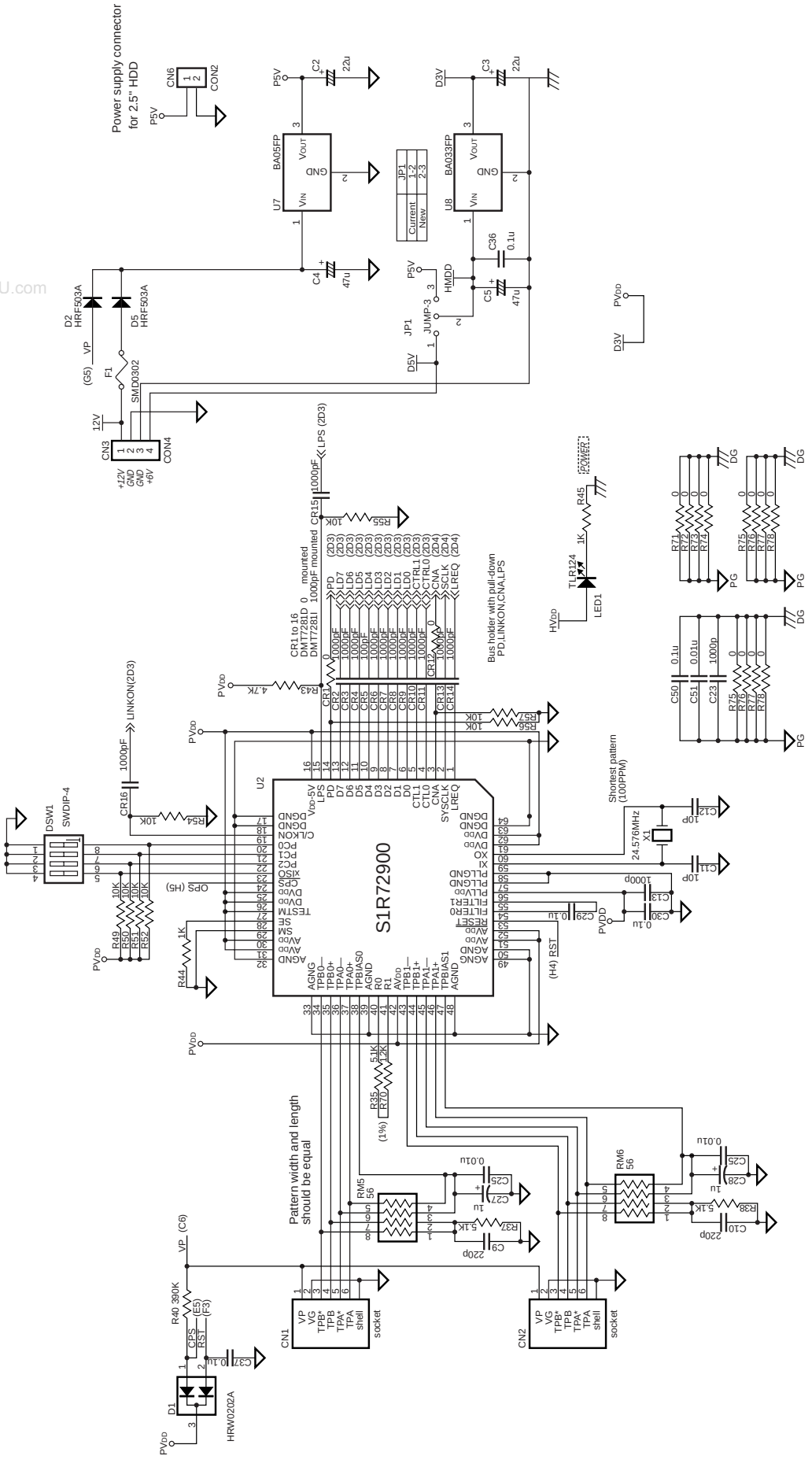


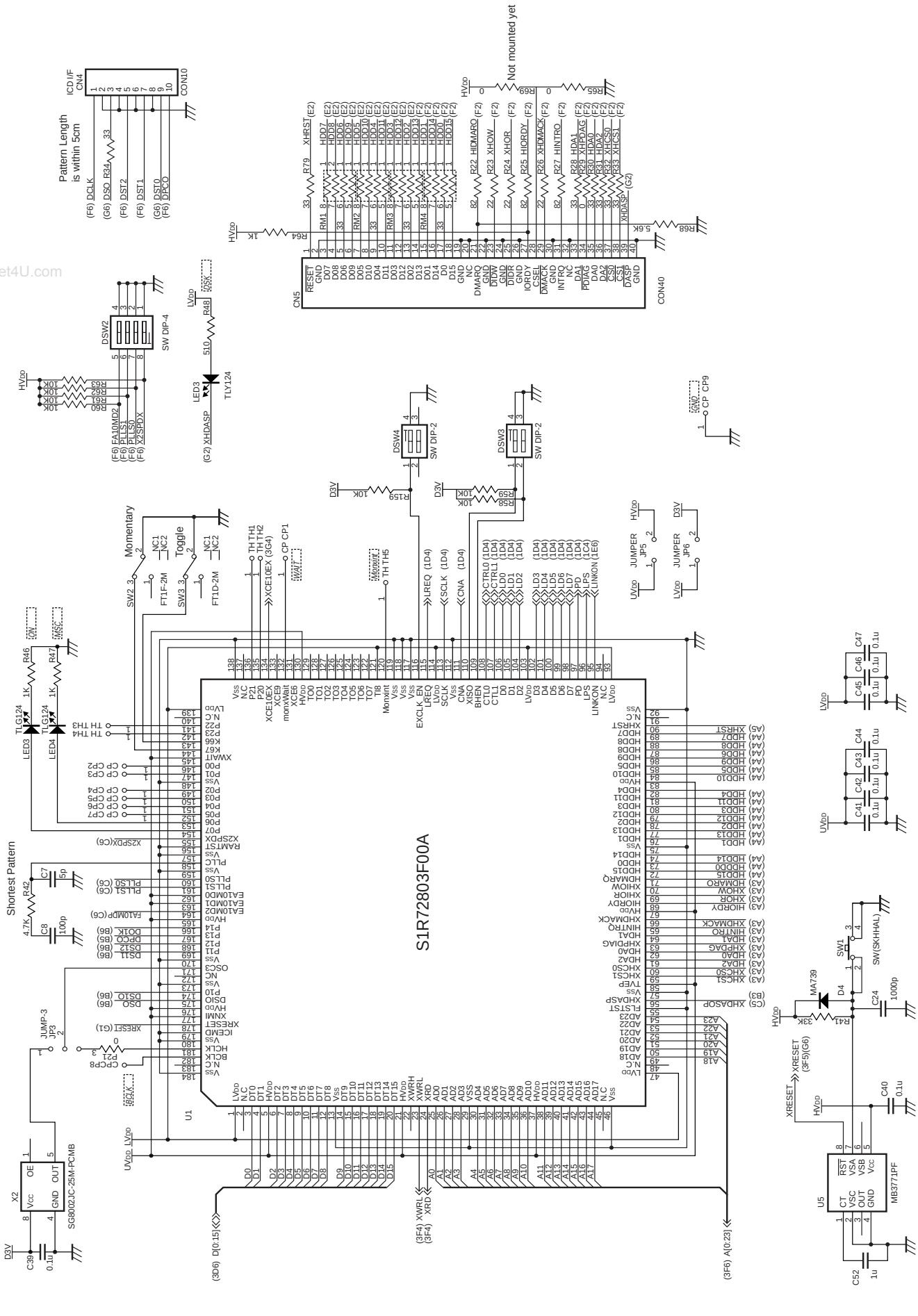
Symbol	Specification	Min.	Max.	Unit
t_{AD}	Address delay time	–	8	ns
t_{CE1}	P_CEx delay time (1)	–	8	ns
t_{CE2}	P_CEx delay time (2)	–	8	ns
t_{WTS}	Wait set-up time	29	–	ns
t_{WTH}	Wait hold time	0	–	ns
t_{WRD1}	Write signal delay time (1)	–	8	ns
t_{WDD1}	Write data delay time (1)	–	10	ns
t_{WDH}	Write data hold time	0	–	ns
t_{WRD2}	Write signal delay time (2)	–	8	ns
t_{WRW}	Write signal pulse width	t_{CYC}(1+WC)–10	–	ns

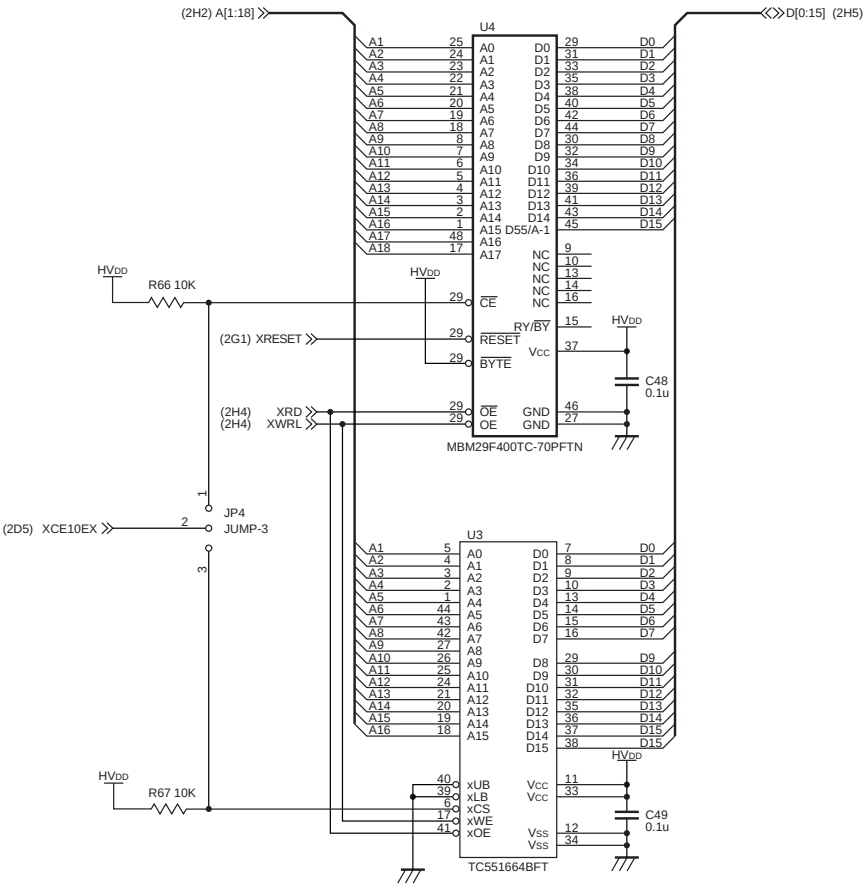
* t_{CYC}=40ns when bus clock is 25MHz in X2 mode.
* WC: Wait cycle signal

Regarding the built-in CPU, refer to the S1C33208/204/202 Technical Manual and S1C33 Family ASIC Macro Manual. In the built-in CPU core, however, a DMA controller or A/D converter are not integrated; this part is different from the description on the DMA controller and A/D converter given in the Technical Manual and Macro Manual. Both low-speed oscillation circuit (OSC1) and high-speed oscillation circuit (OSC4) are not available.

10. EXAMPLES OF EXTERNAL CONNECTION FOR REFERENCE PURPOSES



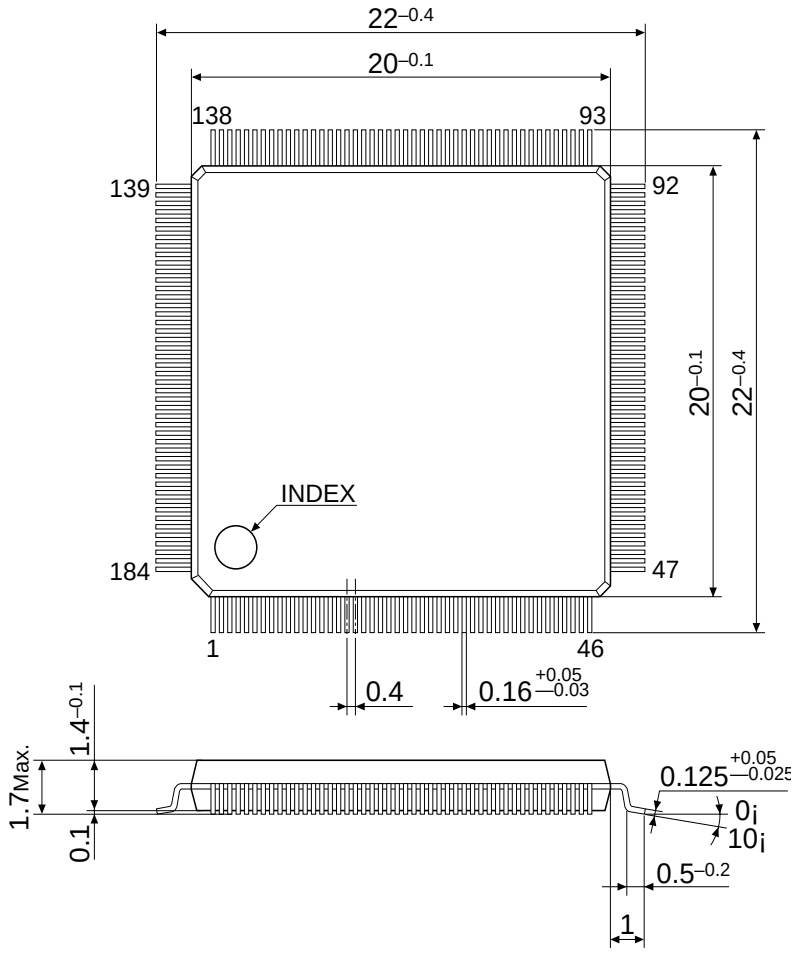




Note: The circuit of this sheet is an example of connection when an external ROM and SRAM are connected during the process of system development. This circuit is not required on a system of finished product.

11. SHAPE OF PACKAGE

Plastic QFP20-184 pin



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First issue September,2001
Printed in JapanⒽA