

# INTEGRATED CIRCUIT

## TOSHIBA

### TECHNICAL DATA

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT

TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70L  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80L, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10L  
 SILICON GATE CMOS

### 131,072-WORD BY 8-BIT CMOS PSEUDO STATIC RAM

#### DESCRIPTION

The TC518128CPL/CSPL/CFL/CFWL/CFTL is a 1,048,578-bit CMOS pseudo static random access memory (PSRAM) organized as 131,072 words by 8 bits. It features a one-transistor dynamic memory cell using CMOS peripheral circuitry to provide large capacity, high speed and low power. It uses a single 5 V  $\pm$  10% power supply. A RFSH input selects either auto or self refresh operation. This device family also features SRAM-like write functions whereby data is written to the memory cell rising edge of R/W signal, for easy interfacing to microprocessors. The TC518128CPL/CSPL/CFL/CFWL/CFTL meets the JEDEC CMOS SRAM pin-compatibility standard and is available in molded 32-pin standard 0.6-inch and 0.3-inch dual-inline plastic packages (DIP) and 0.45-inch and 0.525-inch small-outline plastic packages (SOP), and thin small-outline plastic package (TSOP).

#### FEATURES

- Organized as 131,072 words by 8 bits (1,048,576 bits).
- Fast access time and low power dissipation.
- Single power supply voltage of 5 V  $\pm$  10%.
- Internal counter can be used for auto and self refresh operations.
- Internal timer can be used for self refresh operation.
- Auto refresh power down function.
- 512 refresh cycles per 8 ms.
- All inputs and outputs are TTL compatible.
- Pin compatible with 1M SRAM (JEDEC).
- Logic compatible with SRAM R/W pin.
- Packages: DIP32-P-600 (CPL) (Weight: 4.45 g typ)  
 SOP32-P-450 (CFL) (Weight: 2.34 g typ)  
 DIP32-P-300 (CSPL) (Weight: 0.86 g typ)  
 SOP32-P-525 (CFWL) (Weight: 1.04 g typ)  
 TSOP32-P-0820 (CFTL) (Weight: 0.32 g typ)

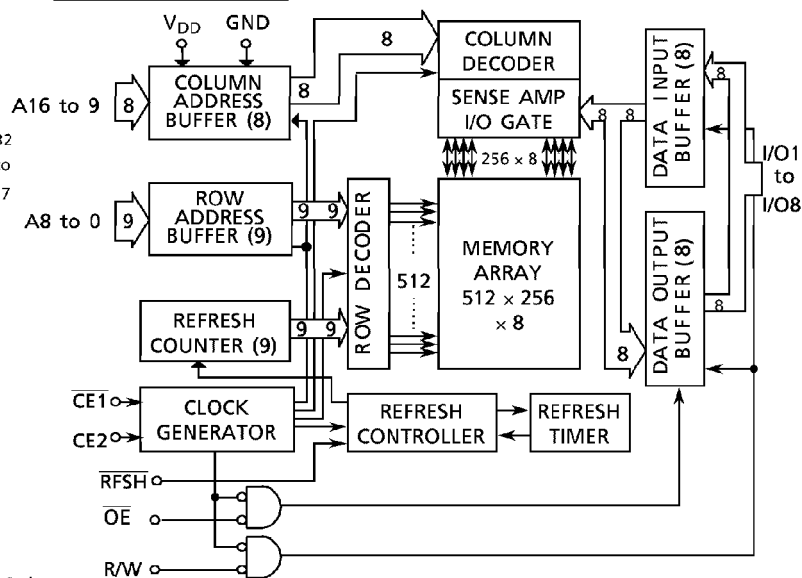
	TC518128C Family		
	-70	-80	-10
t <sub>CEA</sub> CE Access Time	70 ns	80 ns	100 ns
t <sub>OEA</sub> OE Access Time	25 ns	30 ns	40 ns
t <sub>RC</sub> Cycle Time	115 ns	130 ns	160 ns
Power Dissipation	385 mW	330 mW	275 mW
Self Refresh Current	100 $\mu$ A (L version) 50 $\mu$ A (LL version)		

#### PIN ASSIGNMENT (TOP VIEW)

RFSH	1	32	V <sub>DD</sub>
A16	2	31	A15
A14	3	30	CE2
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE1
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

TC518128CPL/CFL/CSPL/CFWL

#### BLOCK DIAGRAM



#### PIN NAMES

A0 to A16	Address Inputs
R/W	Read/Write Control
OE	Output Enable
RFSH	Refresh Input
CE1, CE2	Chip Enable
I/O1 to I/O8	Data Inputs/Outputs
V <sub>DD</sub>	Power
GND	Ground

(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	CE2	A <sub>15</sub>	V <sub>DD</sub>	RFSH	A <sub>16</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	CE1	A <sub>10</sub>	OE

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TC518128CPL - 1

1996 - 09 - 02

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# INTEGRATED CIRCUIT

## TOSHIBA

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#### TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 to A16	I/O1 to 8	CONDITION
L	H	L	H	×	×	OUT	Read
L	H	×	L	×	×	IN	Write
L	H	H	H	×	×	HZ	CE Only Refresh
H	×	×	×	L	×	HZ	Auto/Self Refresh
×	L	×	×	L	×	HZ	Auto/Self Refresh
H	×	×	×	H	×	HZ	Stand by
×	L	×	×	H	×	HZ	Stand by

H ... High Level Input ( $V_{IN} = 6.5\text{ V}$  to  $V_{IH}$  min)

L ... Low Level Input ( $V_{IN} = V_{IL}$  max to  $-1.0\text{ V}$ )

×

×

HZ ... High Impedance

#### ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT	NOTE
$V_{IN}$	Input Voltage	- 1.0 to 7.0	V	1
$V_{OUT}$	Output Voltage	- 1.0 to 7.0	V	
$V_{DD}$	Power Supply Voltage	- 1.0 to 7.0	V	
$T_{OPR}$	Operating Temperature	0 to 70	°C	
$T_{STG}$	Storage Temperature	- 55 to 150	°C	
$T_{SOLDER}$	Soldering Temperature (10 s)	260	°C	
$P_D$	Power Dissipation	600	mW	
$I_{OUT}$	Short Circuit Output Current	50	mA	

#### DC RECOMMENDED OPERATING CONDITIONS ( $T_a = 0^\circ$ to $70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4	-	6.5	V	
$V_{IL}$	Input Low Voltage	- 1.0	-	0.8	V	

TC518128CPL-2

1996-09-02

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#### DC CHARACTERISTICS ( $V_{DD} = 5V \pm 10\%$ , $T_a = 0^\circ$ to $70^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
$I_{DDO}$	Operating Current (Average Power Supply) $\overline{CE1}$ , CE2, Address Cycling: $t_{RC} = t_{RC \text{ min}}$	70 ns version	-	50	70	mA 3, 4
		80 ns version	-	40	60	
		100 ns version	-	35	50	
$I_{DD51}$	Standby Current $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ , $\overline{RFSH} = V_{IH}$	-	-	1	mA	
$I_{DD52}$	Standby Current, $\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ $\overline{RFSH} = V_{DD} - 0.2V$	L version	-	50	100	$\mu\text{A}$
		LL version	-	35	50	
$I_{DDF1}$	Self Refresh Current (Average) $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ , $\overline{RFSH} = V_{IL}$	-	-	1	mA	
$I_{DDF2}$	Self Refresh Current (Average) $\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ , $\overline{RFSH} = 0.2V$	L version	-	50	100	$\mu\text{A}$
		LL version	-	35	50	
$I_{DDF3}$	Auto Refresh Current (Average) (RFSH Cycling: $t_{FC} = t_{FC \text{ min}}$ )	-	-	2	mA	
$I_{DDF4}$	CE Only Refresh Current (Average) ( $\overline{CE1}$ , CE2, Address Cycling: $t_{RC} = t_{RC \text{ min}}$ )	70 ns version	-	50	70	mA 3
		80 ns version	-	40	60	
		100 ns version	-	35	50	
$I_{(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$ , All Other Inputs Not Under Test = $0V$	- 10	-	10	$\mu\text{A}$	
$I_{O(L)}$	Output Leakage Current Output Disable ( $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $R/W = V_{IL}$ ), $0V \leq V_{OUT} \leq V_{DD}$	- 10	-	10	$\mu\text{A}$	
$V_{OH}$	Output High Level $I_{OH} = -1 \text{ mA}$	2.4	-	-	V	
$V_{OL}$	Output Low Level $I_{OL} = 2.1 \text{ mA}$	-	-	0.4	V	

Note: For  $I_{DD51}$  and  $I_{DDF1}$  with  $\overline{CE1} = V_{IH}$  ( $CE2 = V_{IL}$ ), these specification limits are guaranteed for the condition  $CE2 = V_{IH}$  or  $CE2 = V_{IL}$  ( $\overline{CE1} = V_{IH}$  or  $\overline{CE1} = V_{IL}$ ). For  $I_{DD52}$  and  $I_{DDF2}$  with  $\overline{CE1} \geq V_{DD} - 0.2V$  ( $CE2 \leq 0.2V$ ), these specification are guaranteed for the condition  $CE2 \geq V_{DD} - 0.2V$  or  $CE2 \leq 0.2V$  ( $\overline{CE1} \geq V_{DD} - 0.2V$  or  $\overline{CE1} \leq 0.2V$ ).

#### CAPACITANCE ( $V_{DD} = 5V$ , $f = 1 \text{ MHz}$ , $T_a = 25^\circ\text{C}$ )

SYMBOL	PARAMETER	MIN	MAX	UNIT
$C_{11}$	Input Capacitance (A0 to A16)	-	5	pF
$C_{12}$	Input Capacitance ( $\overline{CE1}$ , CE2, $\overline{OE}$ , R/W, $\overline{RFSH}$ )	-	7	pF
$C_{10}$	Input/Output Capacitance	-	7	pF

Note: This parameter is periodically sampled and is not 100% tested.

TC518128CPL-3
1996-09-02
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#### AC CHARACTERISTICS ( $V_{DD} = 5V \pm 10\%$ , $T_a = 0^\circ$ to $70^\circ\text{C}$ ) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
$t_{RC}$	Random Read or Write Cycle Time	115	–	130	–	160	–	ns	
$t_{RMW}$	Read-Modify-Write Cycle Time	160	–	180	–	220	–	ns	
$t_{CE}$	CE Pulse Width	70	10,000	80	10,000	100	10,000	ns	13
$t_p$	CE Precharge Time	35	–	40	–	50	–	ns	
$t_{CEA}$	CE Access Time	–	70	–	80	–	100	ns	
$t_{OEA}$	$\overline{OE}$ Access Time	–	25	–	30	–	40	ns	
$t_{CLZ}$	CE to Output in Low-Z	20	–	20	–	20	–	ns	
$t_{OLZ}$	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
$t_{WLZ}$	Output Active from End of Write	0	–	0	–	0	–	ns	
$t_{CHZ}$	Chip Disable to Output in High-Z	0	20	0	20	0	25	ns	9
$t_{OHZ}$	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	0	25	ns	9
$t_{WHZ}$	Write Enable to Output in High-Z	0	25	0	25	0	30	ns	9
$t_{ODS}$	$\overline{OE}$ Output Disable Setup Time	0	–	0	–	0	–	ns	
$t_{ODH}$	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
$t_{RCS}$	Read Command Setup Time	0	–	0	–	0	–	ns	
$t_{RCH}$	Read Command Hold Time	0	–	0	–	0	–	ns	
$t_{WP}$	Write Pulse Width	20	–	25	–	30	–	ns	
$t_{WCH}$	Write Command Hold Time	35	10,000	40	10,000	50	10,000	ns	
$t_{CWL}$	Write Command to CE Lead Time	20	10,000	25	10,000	30	10,000	ns	
$t_{DSW}$	Data Setup Time from R/W	15	–	20	–	25	–	ns	10
$t_{DSC}$	Data Setup Time from CE	15	–	20	–	25	–	ns	10
$t_{DHW}$	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
$t_{DHC}$	Data Hold Time from CE	0	–	0	–	0	–	ns	10
$t_{ASC}$	Address Setup Time	0	–	0	–	0	–	ns	11
$t_{AHC}$	Address Hold Time	20	–	25	–	30	–	ns	11
$t_{RHC}$	RFSH Command Hold Time	15	–	15	–	15	–	ns	
$t_{FC}$	Auto Refresh Cycle Time	115	–	130	–	160	–	ns	
$t_{RFD}$	RFSH Delay Time from CE	35	–	40	–	50	–	ns	
$t_{FAP}$	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
$t_{FP}$	RFSH Precharge Time	30	–	30	–	30	–	ns	12
$t_{FAS}$	RFSH Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
$t_{FRS}$	CE Delay Time from RFSH (Self Refresh)	160	–	160	–	190	–	ns	12
$t_{REF}$	Refresh Period (512 cycles, A0 to A8)	–	8	–	8	–	8	ms	
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
$t_{CES}$	CE2 Low Setup Time	5	–	5	–	5	–	ns	14
$t_{CEH}$	CE2 Low Hold Time	5	–	5	–	5	–	ns	14

TC518128CPL – 4

1996 - 09 - 02

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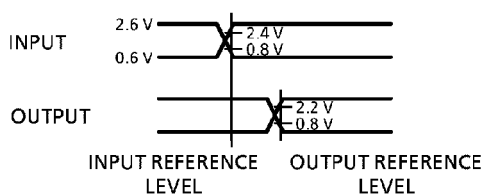
#### Notes:

- 1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
- 2) All voltage are referenced to GND.
- 3)  $I_{DDO}$  and  $I_{DDF4}$  depend on cycle rate.
- 4)  $I_{DDO}$  depends on output loading. Specified values are obtained with the output open.
- 5) An initial pause of 100  $\mu$ s with  $\overline{CE1}$  High or CE2 Low is required after power-up before proper device operation is achieved.
- 6) AC measurements assume  $t_T = 5$  ns.
- 7) Timing reference levels

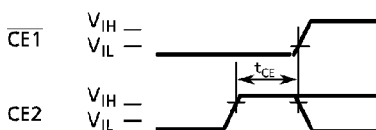
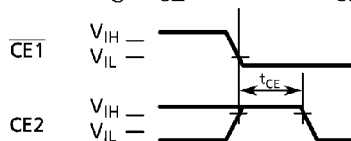
Input Level :  $V_{IH} = 2.6$  V  
 $V_{IL} = 0.6$  V

Input Reference Level :  $V_{IH} = 2.4$  V  
 $V_{IL} = 0.8$  V

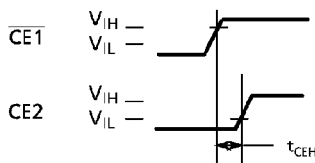
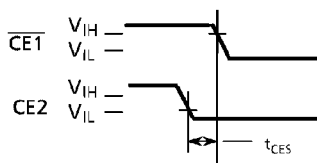
Output Reference Level:  $V_{OH} = 2.2$  V  
 $V_{OL} = 0.8$  V



- 8) Measured with a load equivalent to 1 TTL load and 100 pF.
- 9) Parameters  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) In write cycles, input data is latched at the earlier of the R/W or  $\overline{CE1}$  rising edge and CE2 falling edge. Therefore, input data must be valid during the setup time ( $t_{DSW}$  or  $t_{DSC}$ ) and hold time ( $t_{DHW}$  or  $t_{DHC}$ ).
- 11) All address inputs are latched on the falling edge of  $\overline{CE1}$  and the rising edge of CE2. Therefore, all address inputs must be valid during  $t_{ASC}$  and  $t_{AHC}$ .
- 12) Two refresh operations—auto refresh and self refresh—are defined by the  $\overline{RFSH}$  pulse width under the condition  $\overline{CE1} = V_{IH}$  or  $CE2 = V_{IL}$ .  
 Auto refresh:  $\overline{RFSH}$  pulse width  $\leq t_{FAP}$  (max)  
 Self refresh :  $\overline{RFSH}$  pulse width  $\geq t_{FAS}$  (min)  
 The timing parameter ( $t_{FRS}$ ) must be observed for proper device operation in accordance with the following conditions.
  - After self refresh
  - When  $\overline{RFSH} = "L"$  after power-up
- 13) The timings  $t_{CE}$  (min) and  $t_{CE}$  (max) must be observed for proper device operation as follows.



- 14) The timings  $t_{CES}$  (min) and  $t_{CEH}$  (min) must be observed for using  $\overline{CE1}$  and CE2 on the same clock as follows.



TC518128CPL - 5

1996 - 09 - 02

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# INTEGRATED CIRCUIT

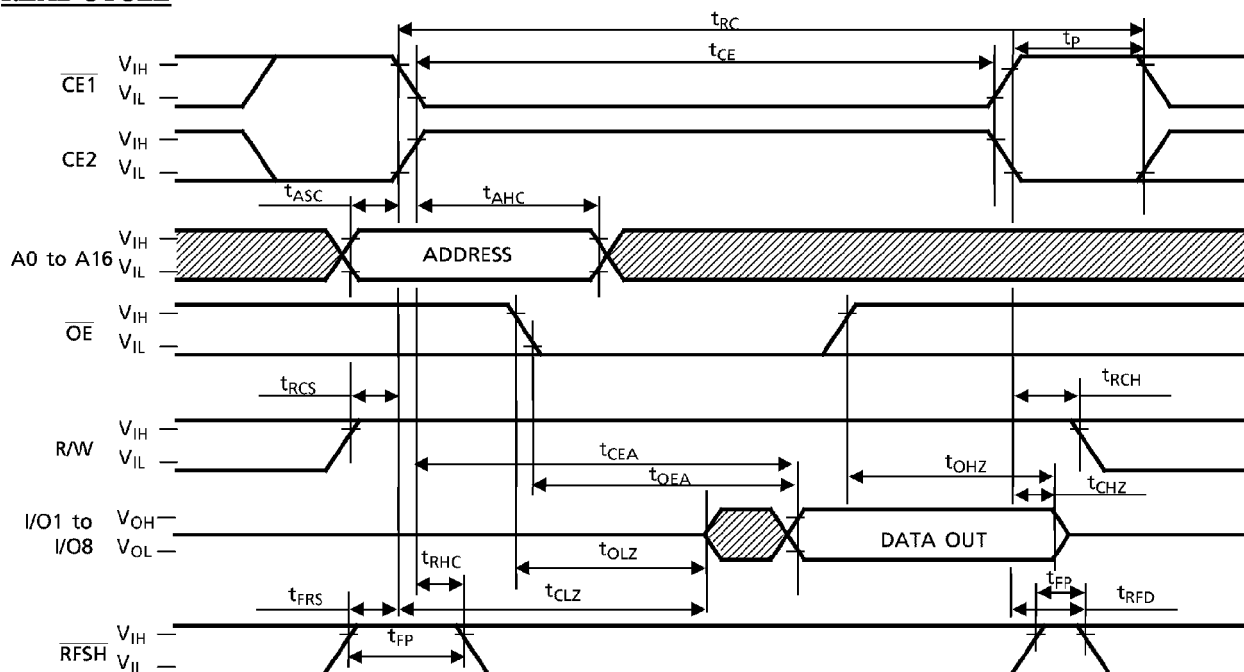
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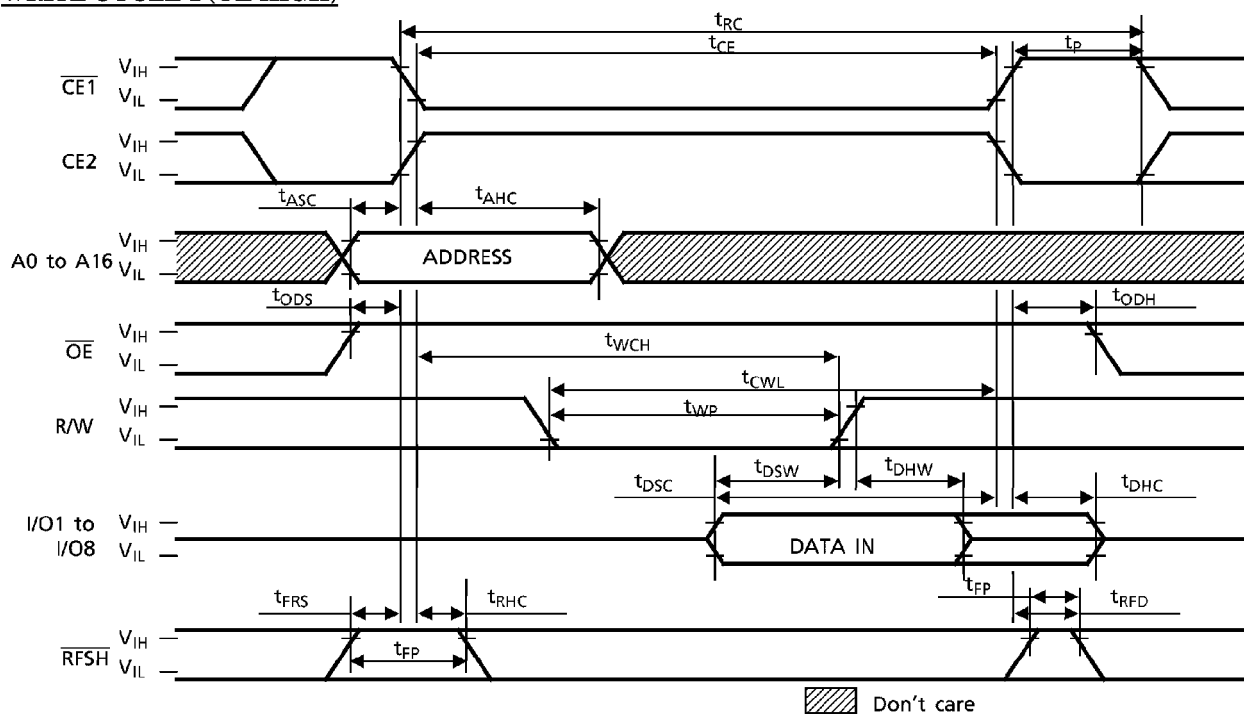
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### TIMING DIAGRAMS

#### READ CYCLE



#### WRITE CYCLE 1 (OE HIGH)



Note: The device can be operated by cycling the  $\overline{CE1}$  (or  $\overline{CE2}$ ) pin only, provided that  $\overline{CE2}$  (or  $\overline{CE1}$ ) is set to the  $V_{IH}$  (or  $V_{IL}$ ) level.

TC518128CPL - 6

1996 - 09 - 02

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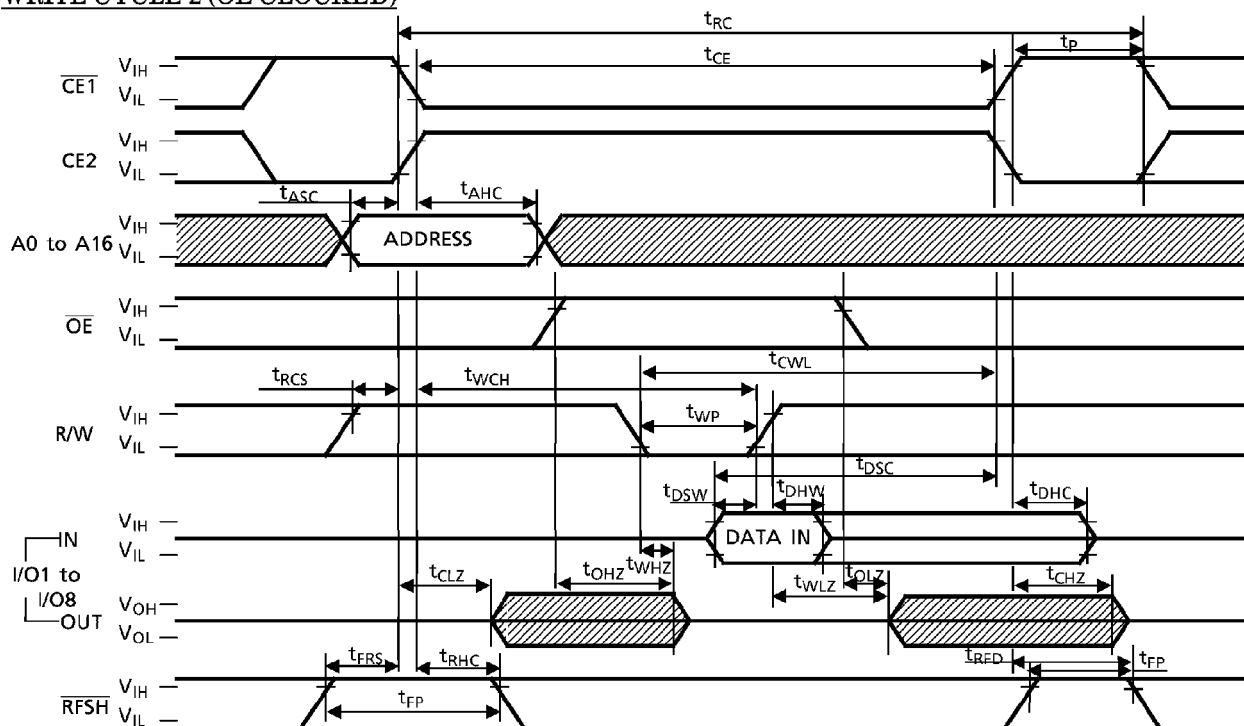
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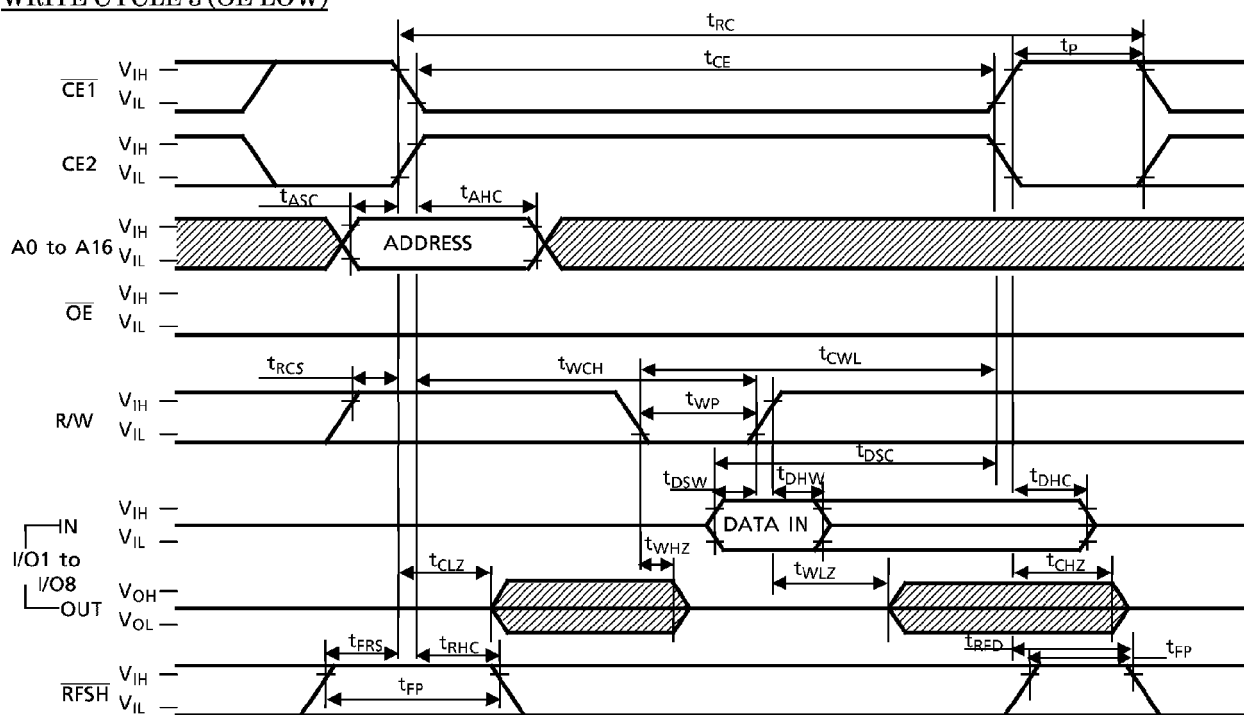
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#### WRITE CYCLE 2 ( $\overline{OE}$ CLOCKED)



#### WRITE CYCLE 3 ( $\overline{OE}$ LOW)



Don't care

Note: The device can be operated by cycling the  $\overline{CE1}$  (or  $\overline{CE2}$ ) pin only, provided that  $\overline{CE2}$  (or  $\overline{CE1}$ ) is set to the  $V_{IH}$  (or  $V_{IL}$ ) level.

TC518128CPL-7

1996-09-02

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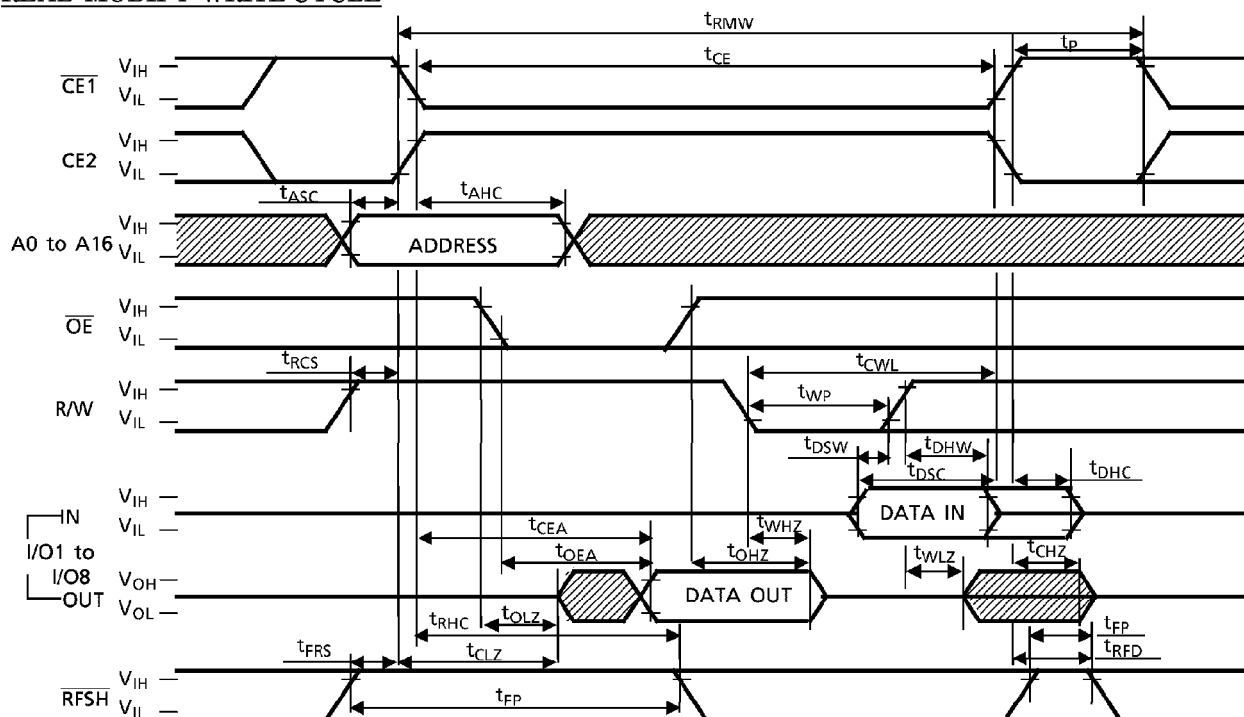
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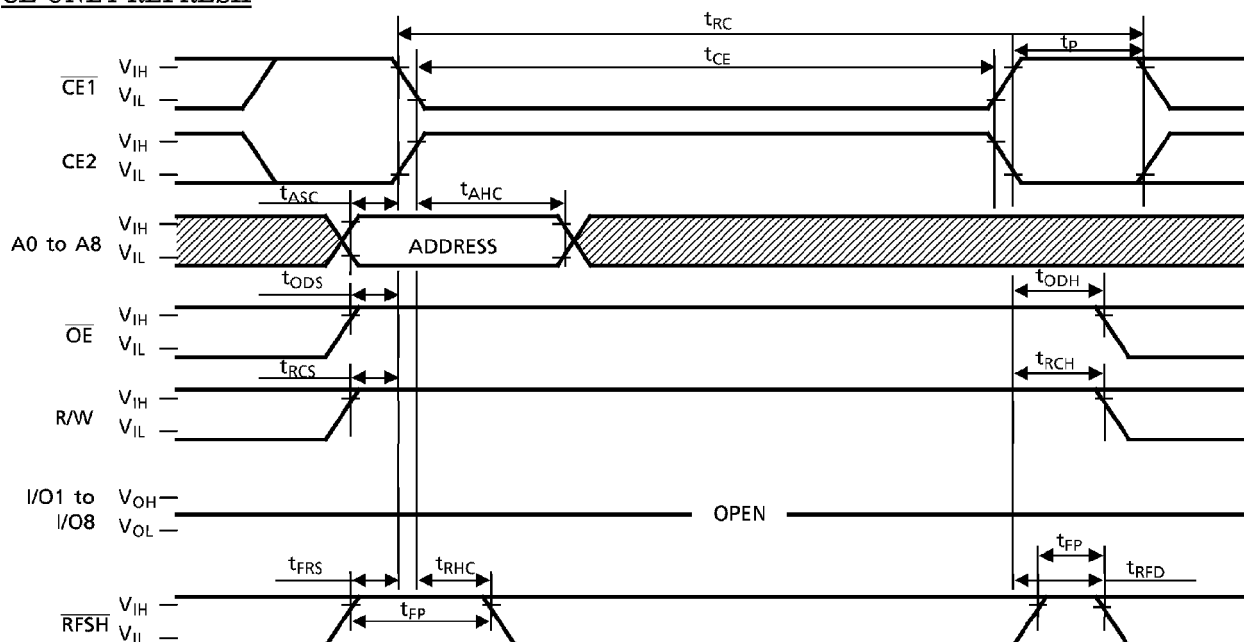
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#### READ-MODIFY-WRITE CYCLE



#### CE-ONLY REFRESH



Note: A9 to A16 = Don't care.

Don't care

Note: The device can be operated by cycling the  $\overline{CE1}$  (or CE2) pin only, provided that CE2 (or CE1) is set to the  $V_{IH}$  (or  $V_{IL}$ ) level.

TC518128CPL-8

1996-09-02

TOSHIBA CORPORATION



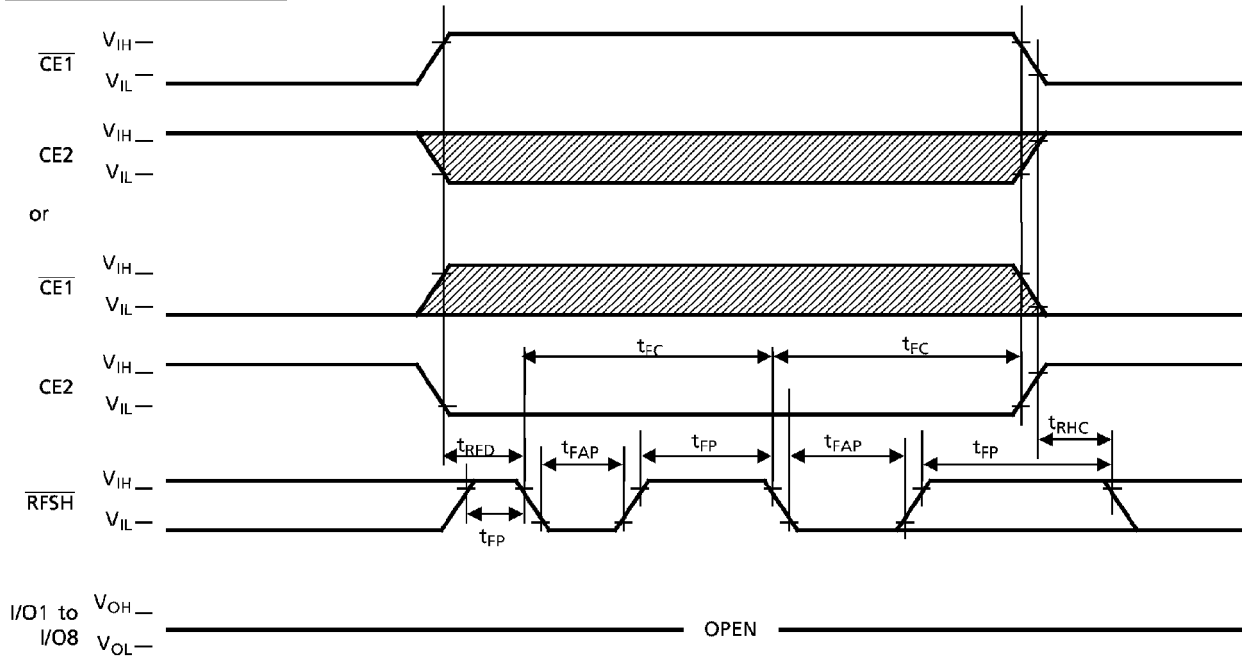
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TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70L  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80L, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10L

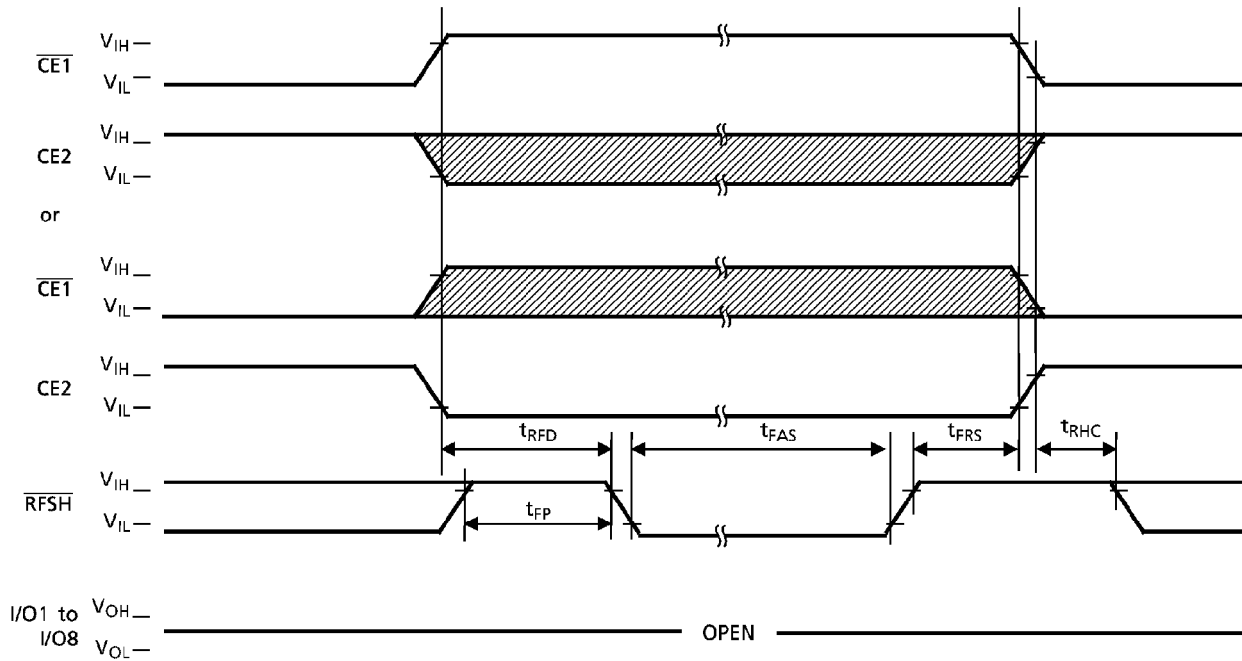
#### RFSH AUTO REFRESH



Note:  $\overline{OE}$ , R/W, A0 to A16 = Don't care.

Don't care

#### SELF REFRESH



Note:  $\overline{OE}$ , R/W, A0 to A16 = Don't care.

Don't care

TC518128CPL-9
1996-09-02
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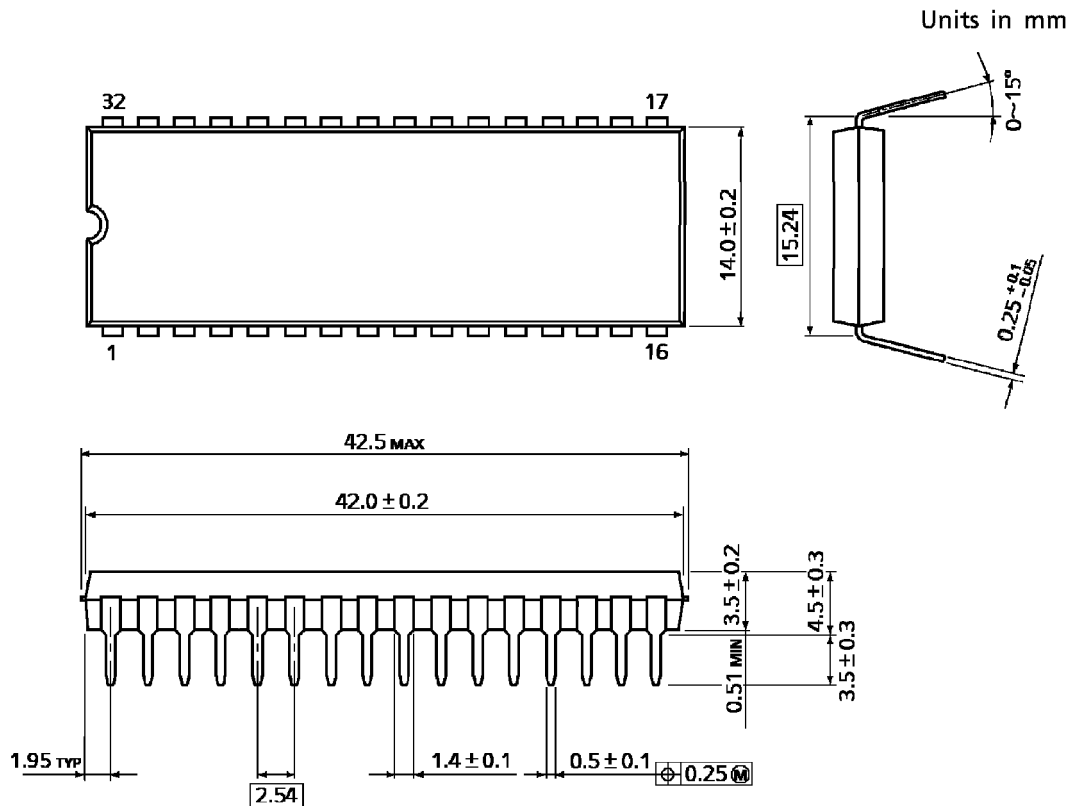
# INTEGRATED CIRCUIT

## TOSHIBA

### TECHNICAL DATA

TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70L  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80L, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10L

#### PACKAGE DIMENSIONS (DIP32-P-600)



Weight: 4.45 g (typ)

TC518128CPL-70, -70L  
 TC518128CPL-80, -80L  
 TC518128CPL-10, -10L

TC518128CPL-10
1996-09-02
<b>TOSHIBA CORPORATION</b>

# INTEGRATED CIRCUIT

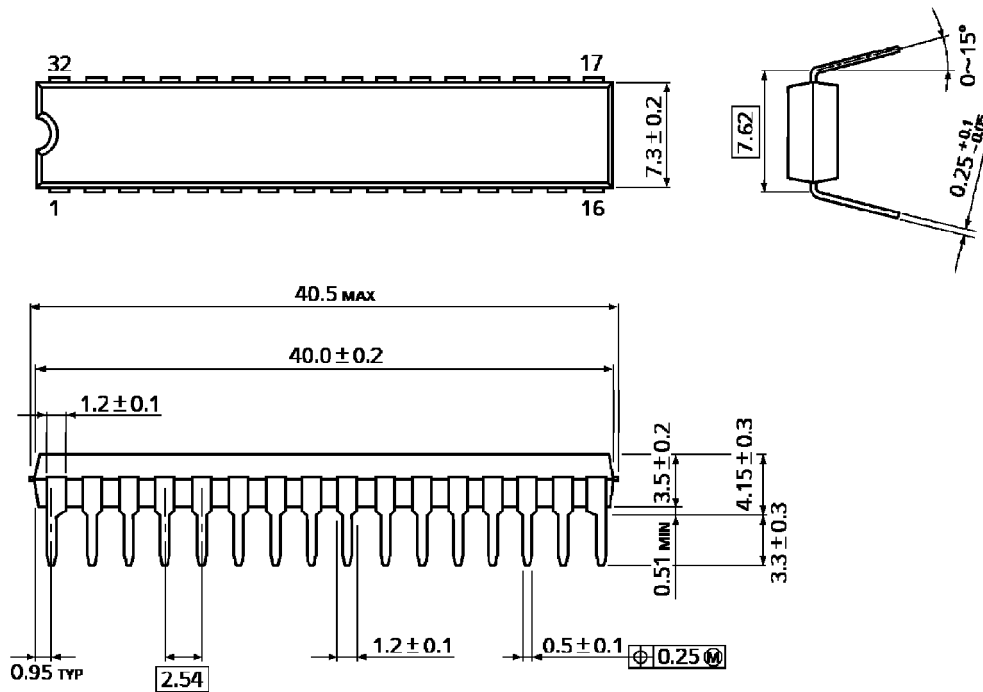
## TOSHIBA

### TECHNICAL DATA

TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70L  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80L, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10L

#### PACKAGE DIMENSIONS (DIP32-P-300)

Units in mm



Weight: 2.34 g (typ)

TC518128CSPL-70, -70L  
 TC518128CSPL-80, -80L  
 TC518128CSPL-10, -10L

TC518128CPL-11

1996-09-02

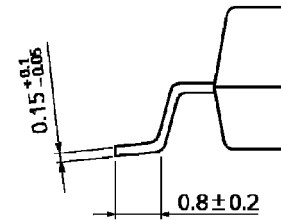
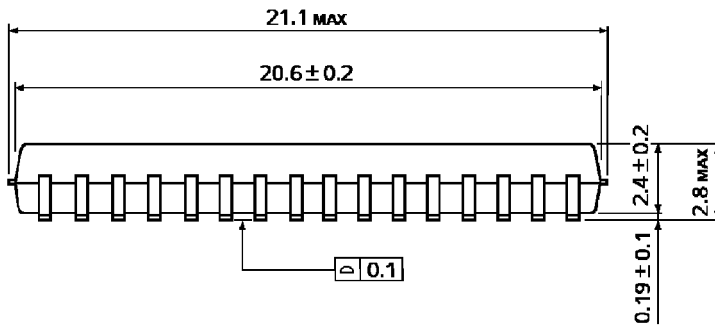
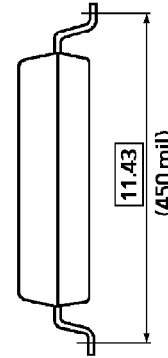
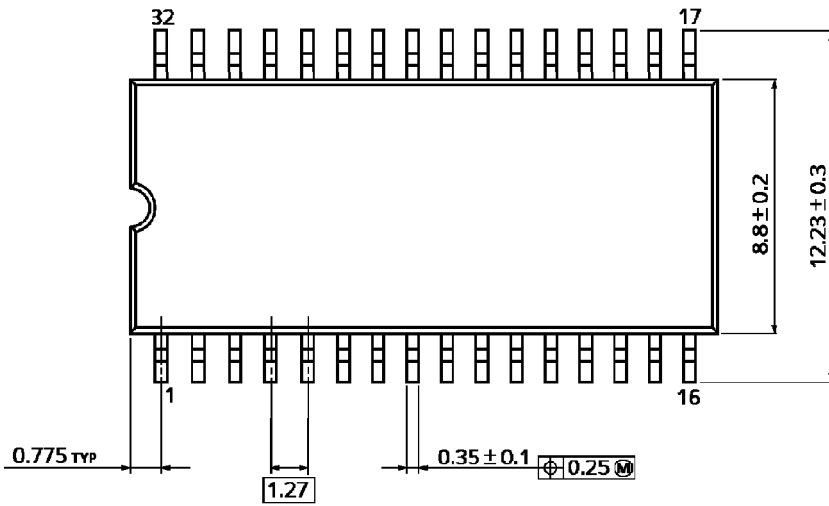
TOSHIBA CORPORATION

**TOSHIBA**  
**INTEGRATED CIRCUIT**  
 TECHNICAL DATA

TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70L  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80L, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10L

**PACKAGE DIMENSIONS (SOP32-P-450)**

Units in mm



Weight: 0.86 g (typ)

TC518128CFL-70, -70L  
 TC518128CFL-80, -80L  
 TC518128CFL-10, -10L

TC518128CPL-12
1996-09-02
<b>TOSHIBA CORPORATION</b>

# INTEGRATED CIRCUIT

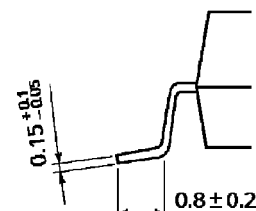
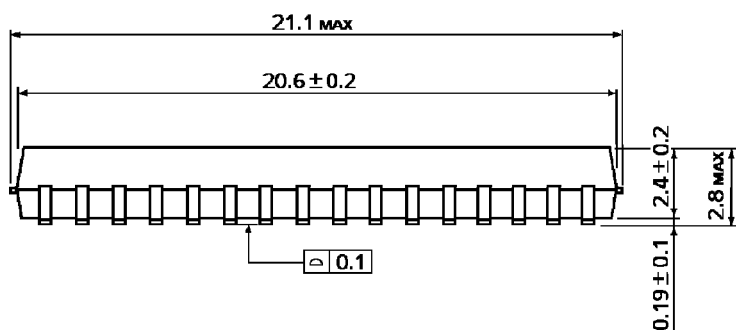
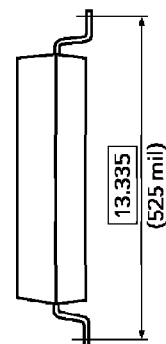
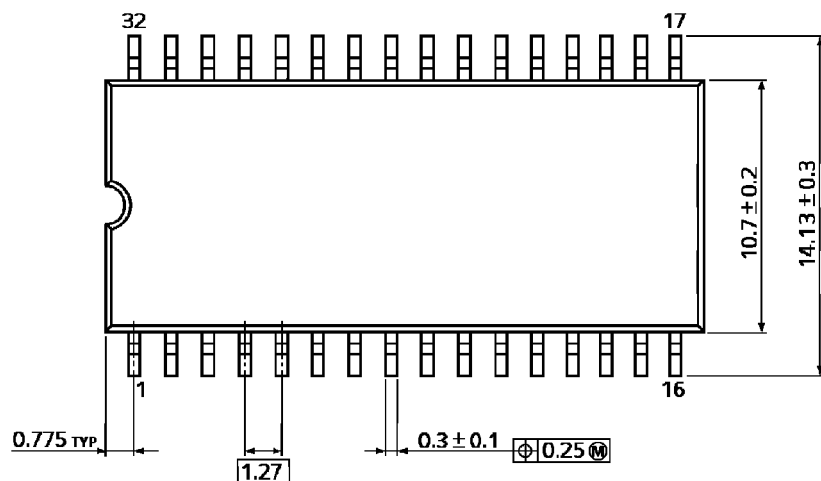
## TOSHIBA

### TECHNICAL DATA

TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 70L  
 TC518128 CPL / CSPL / CFL / CFWL / CFTL - 80L, TC518128 CPL / CSPL / CFL / CFWL / CFTL - 10L

#### PACKAGE DIMENSIONS (SOP32-P-525)

Units in mm



Weight: 1.04 g (typ)

TC518128CFWL-70, -70L

TC518128CFWL-80, -80L

TC518128CFWL-10, -10L

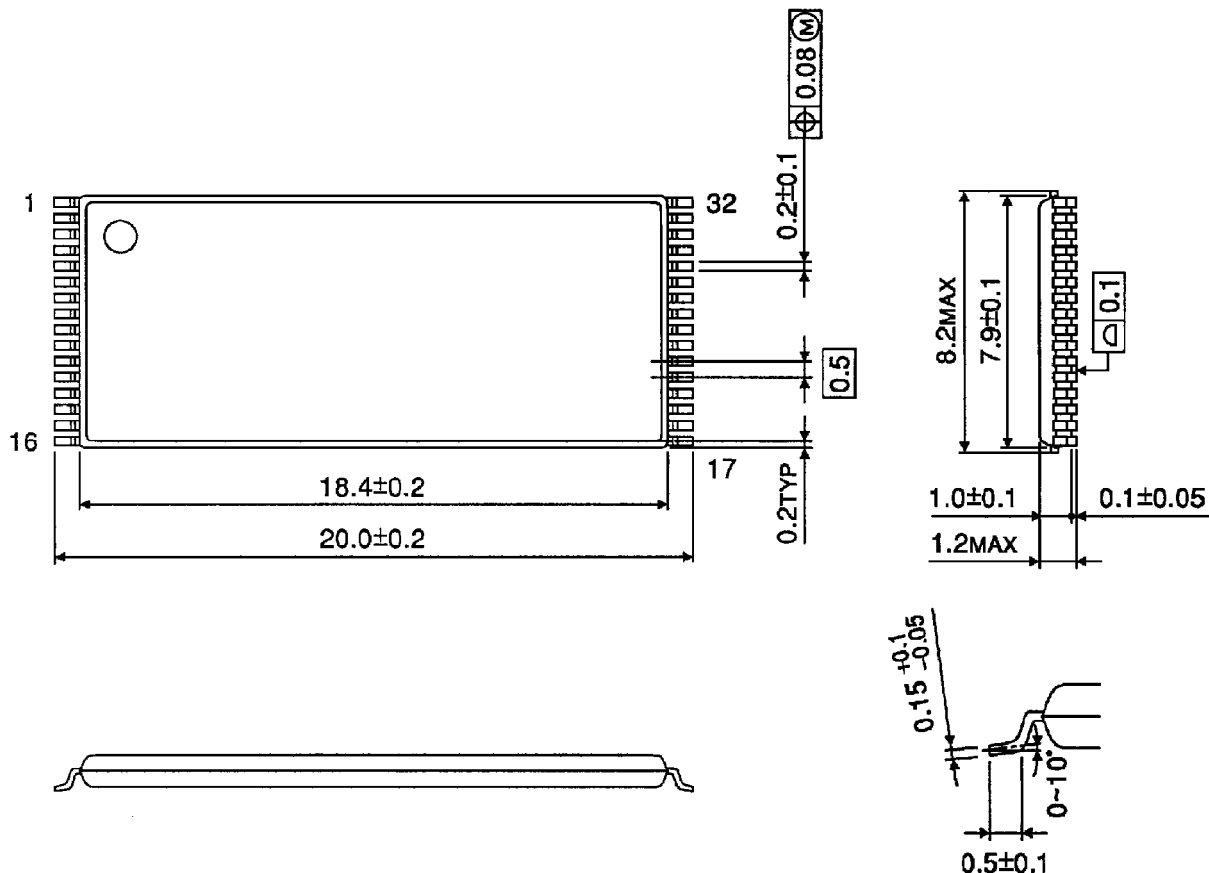
TC518128CPL-13

1996-09-02

TOSHIBA CORPORATION

PACKAGE DIMENSIONS (TSOP32-P-0820)

Units in mm



Weight: 0.32 g (typ)

TC518128CFTL-70, -70L  
TC518128CFTL-80, -80L  
TC518128CFTL-10, -10L

TC518128CPL - 14*
1996 - 09 - 02
<b>TOSHIBA CORPORATION</b>