TOSHIBA

TC51832AP/ASP/AF-70/85/10
TC51832APL/ASPL/AFL-70/85/10

SILICON GATE CMOS

32,768 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC51832AP is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832AP utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC51832AP operates from a single 5V power supply. Refreshing is supported by a refresh ($\overline{RFSH}$) input which enables two types of refreshing - auto refresh and self refresh. The TC51832AP features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC51832AP is pin-compatible with the 256K bit CMOS static RAM JEDEC standard and is available in a 28-pin, 0.6 inch and 0.3 inch width plastic DIP, and a small outline plastic flat package.

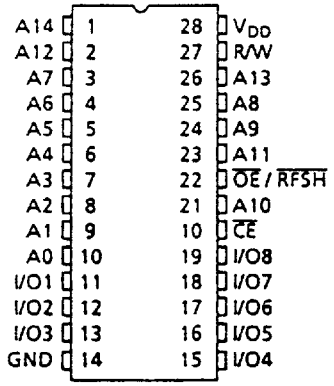
Features

- Organization: 32,768 words x 8 bits
- Single 5V power supply
- Fast access time

	TC51832A Family		
	-70	-85	-10
t_{CEA} CE Access Time	70ns	85ns	100ns
t_{OEA} OE Access Time	30ns	35ns	40ns
t_{RC} Cycle Time	115ns	135ns	160ns
Power Dissipation	385mW	303mW	248mW
Self Refresh Current	1mA/100μA		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 256 refresh cycles/4ms
- Pin compatible: 256K SRAM (JEDEC)
- Package
  - TC51832AP/APL : DIP28-P-600
  - TC51832ASP/ASPL : DIP28-P-300B
  - TC51832AF/AFL : SOP28-P-450

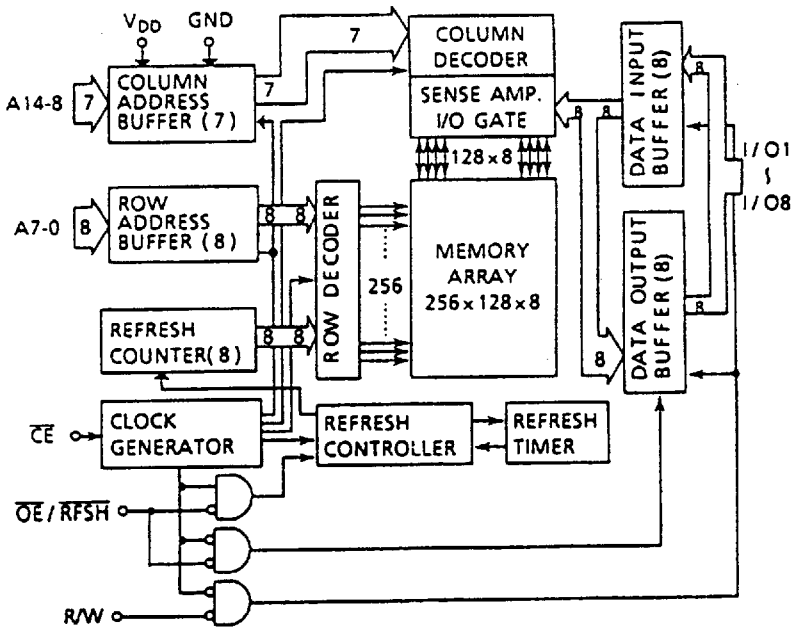
Pin Connection (Top View)



Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Block Diagram



Operating Mode

MODE \ PIN	$\overline{CE}$	$\overline{OE}$/ $\overline{RFSH}$	R/W	A0 ~ A14	I/O1 ~ 8
Read	L	L	H	V*	OUT
Write	L	H	L	V*	IN
$\overline{CE}$ only Refresh	L	H	H	V*	HZ
Auto/Self Refresh	H	L	*	*	HZ
Standby	H	H	*	*	HZ

H = High level input (V_{IH})
L = Low level input (V_{IL})
* = V_{IH} or V_{IL}
V* = At the falling edge of $\overline{CE}$, all address inputs are latched. At all other times, the address inputs are "*".
HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	V_{DD} + 1.0	V	
V_{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	70ns version	–	35	70	mA	3,4
		85ns version	–	30	55		
		100ns version	–	25	45		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IH}	TC1832AP/ASP/AF	–	–	1	mA	
		TC1832APL/ASPL/AFL	–	–	1		
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} - 0.2V, $\overline{OE}$/$\overline{RFSH}$ = V_{DD} - 0.2V	TC1832AP/ASP/AF	–	–	1	mA	
		TC1832APL/ASPL/AFL	–	–	100	µA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IL}	TC1832AP/ASP/AF	–	–	1	mA	
		TC1832APL/ASPL/AFL	–	–	1		
I_{DDF2}	Self Refresh Current (Average) $\overline{CE}$ = V_{DD} - 0.2V, $\overline{OE}$/$\overline{RFSH}$ = 0.2V	TC1832AP/ASP/AF	–	–	1	mA	
		TC1832APL/ASPL/AFL	–	60	100	µA	
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		–	–	±10	µA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE}$ = V_{IH} or $\overline{OE}$/$\overline{RFSH}$ = V_{IH} or R/W = V_{IL}) 0V ≤ V_{OUT} ≤ V_{DD}		–	–	±10	µA	
V_{OH}	Output High Level I_{OH} = -1mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 2.1mA		–	–	0.4	V	

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A14)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	–	7	
C_{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-85		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	–	135	–	160	–		
t_{RMW}	Read Modify Write Cycle Time	175	–	190	–	220	–		
t_{CE}	$\overline{CE}$ Pulse Width	70	10,000	85	10,000	100	10,000		
t_P	$\overline{CE}$ Precharge Time	35	–	40	–	50	–		
t_{CEA}	$\overline{CE}$ Access Time	–	70	–	85	–	100		
t_{OEA}	$\overline{OE}$ Access Time	–	30	–	35	–	40		
t_{CLZ}	$\overline{CE}$ to Output in Low -Z	20	–	20	–	20	–		
t_{OLZ}	$\overline{OE}$ to Output in Low -Z	0	–	0	–	0	–		
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–		
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	25	0	30		9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	25	0	30		9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t_{OSC}	$\overline{OE}$ Setup Time Referenced to $\overline{CE}$	10	–	10	–	10	–		9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–		9
t_{RCS}	Read Command Setup Time	0	–	0	–	0	–		
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	25	–	25	–	25	–		
t_{WCH}	Write Command Hold Time	40	–	40	–	40	–		
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	25	–	25	–	25	–		
t_{DSW}	Data Setup Time from R/W	20	–	20	–	20	–		10
t_{DSC}	Data Setup Time from $\overline{CE}$	20	–	20	–	20	–		10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–		10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	0	–		10
t_{ASC}	Address Setup Time	0	–	0	–	0	–		11
t_{AHC}	Address Hold Time	20	–	20	–	20	–		11
t_{FC}	Auto Refresh Cycle Time	115	–	135	–	160	–		
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	35	–	40	–	50	–		
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000		12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–		12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–		12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	115	–	135	–	160	–		12
t_{REF}	Refresh Period (256 cycles, A0 ~ A7)	–	4	–	4	–	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DDO} depends on the cycle time.

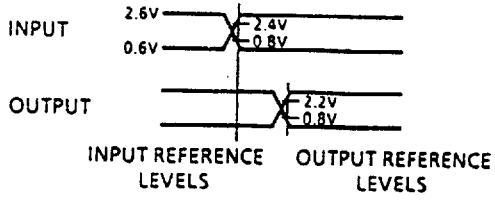
4) I_{DDO} depends on the output loading. Specified values are obtained with the outputs open.

5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up before proper device operation is achieved.

6) AC measurements assume t_T = 5ns.

7) Timing reference levels

Input Levels	:	V_{IH} = 2.6V V_{IL} = 0.6V
Input Reference Levels	:	V_{IH} = 2.4V V_{IL} = 0.8V
Output Reference Levels	:	V_{OH} = 2.2V V_{OL} = 0.8V



8) Measured with a load equivalent to 1 TTL load and 100pF.

9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) For write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

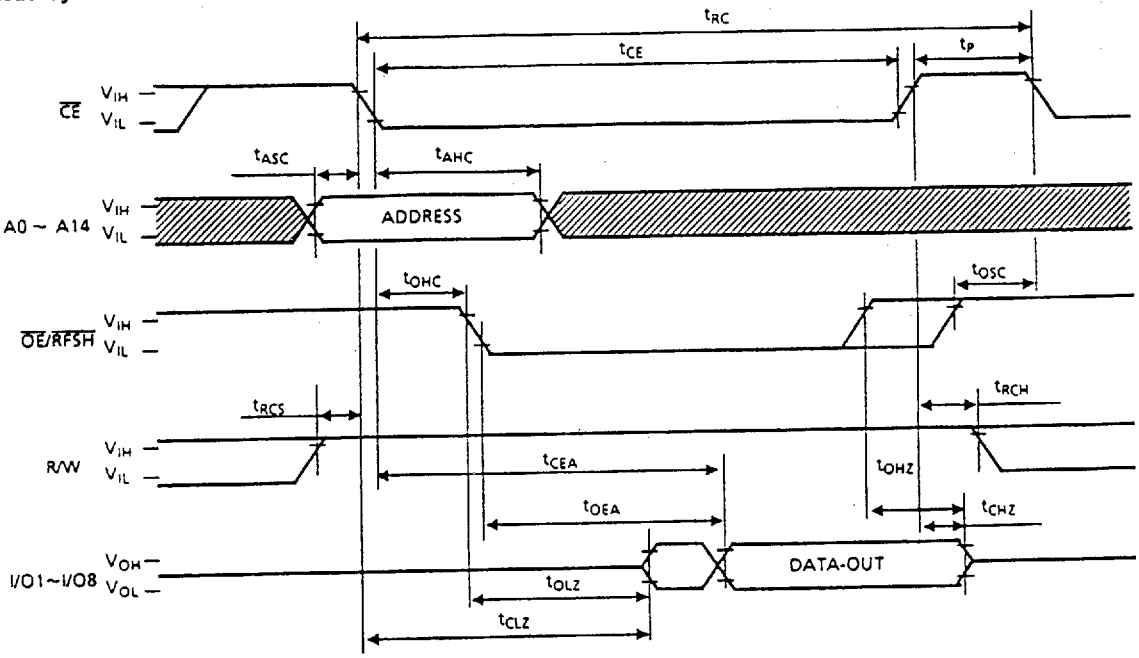
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC}.

12) The two refresh operations, auto refresh and self refresh, are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE}$ = V_{IH}.
Auto refresh : $\overline{RFSH}$ pulse width ≤ t_{FAP} (max.)
Self refresh : $\overline{RFSH}$ pulse width ≥ t_{FAS} (min.)

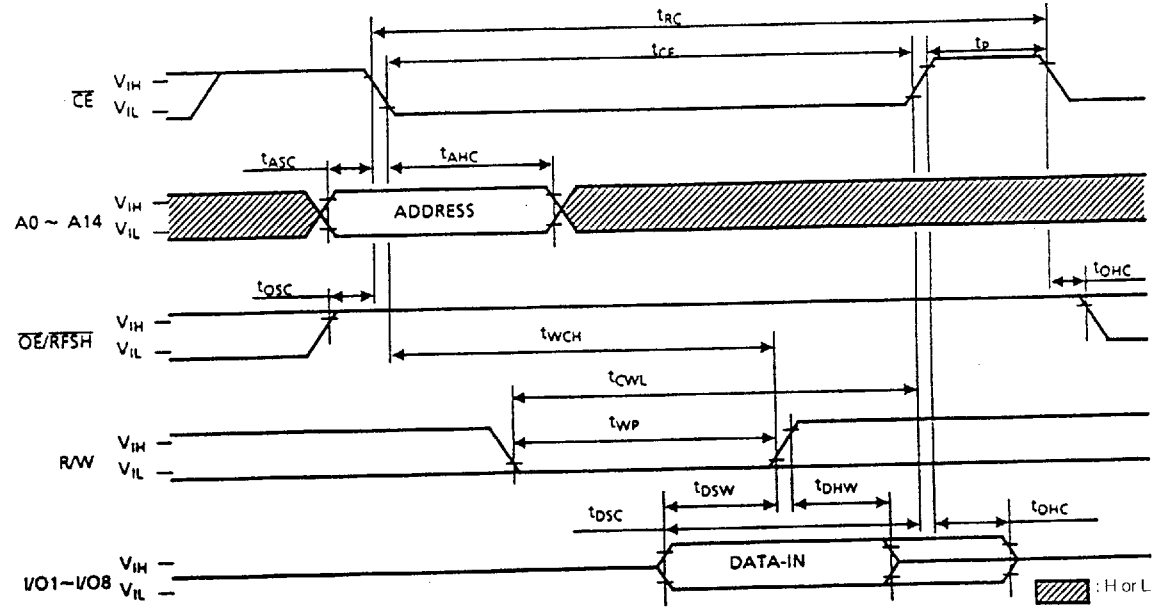
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:
- after self refresh
- if $\overline{RFSH}$ = "L" after power-up

Timing Waveforms

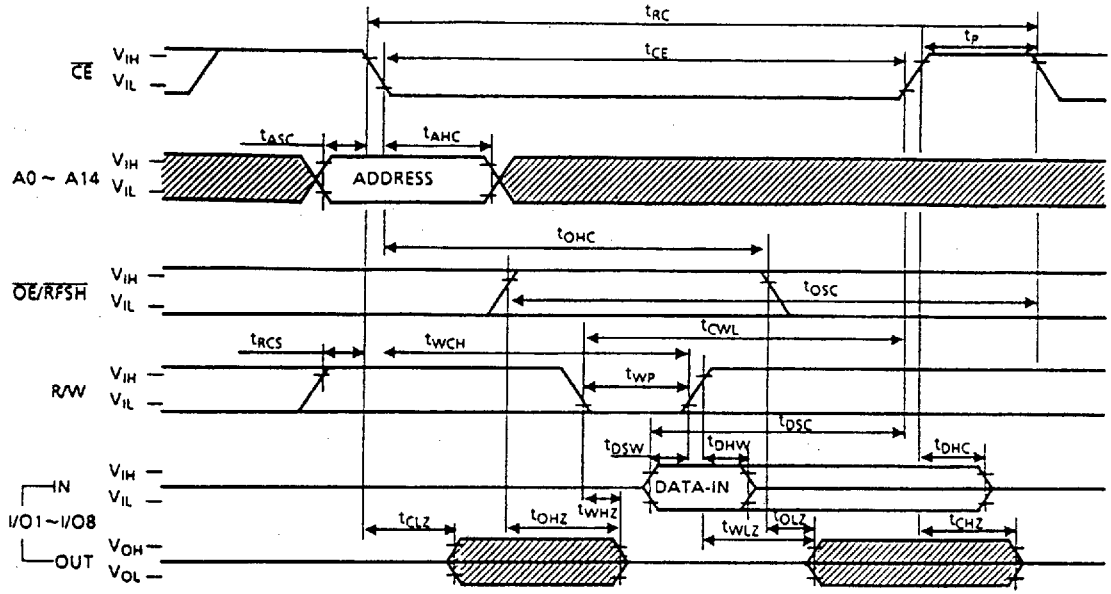
Read Cycle



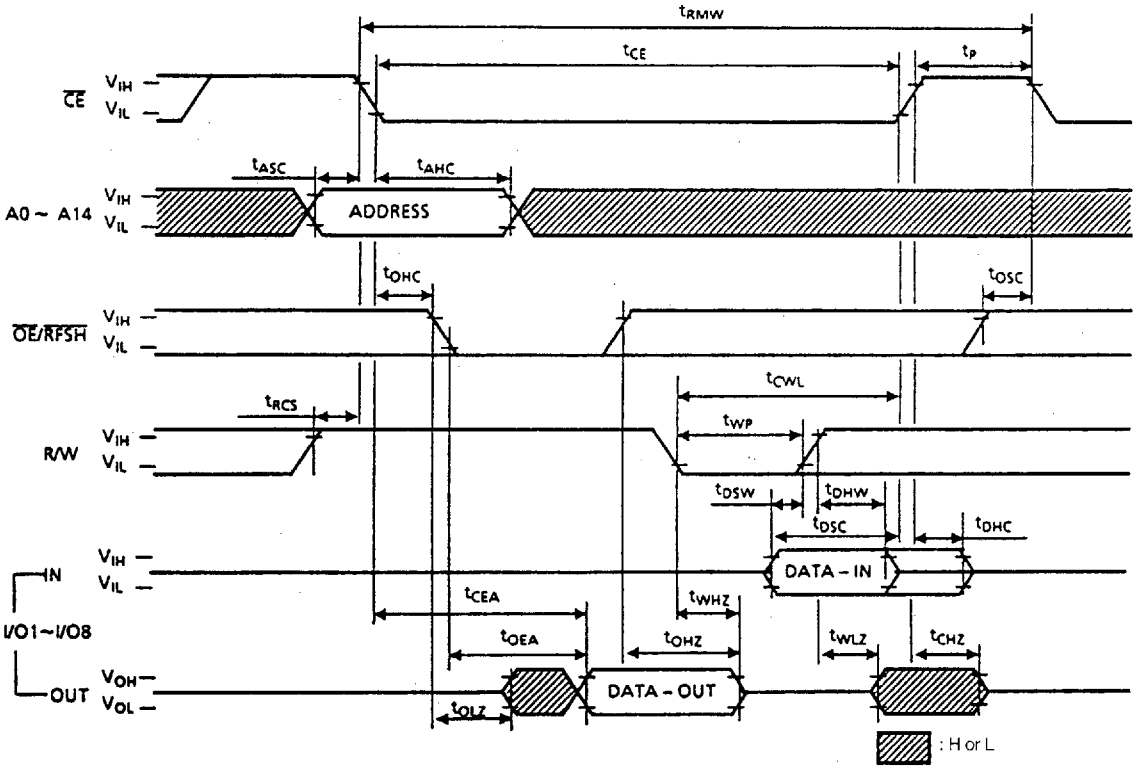
Read Modify Write Cycle



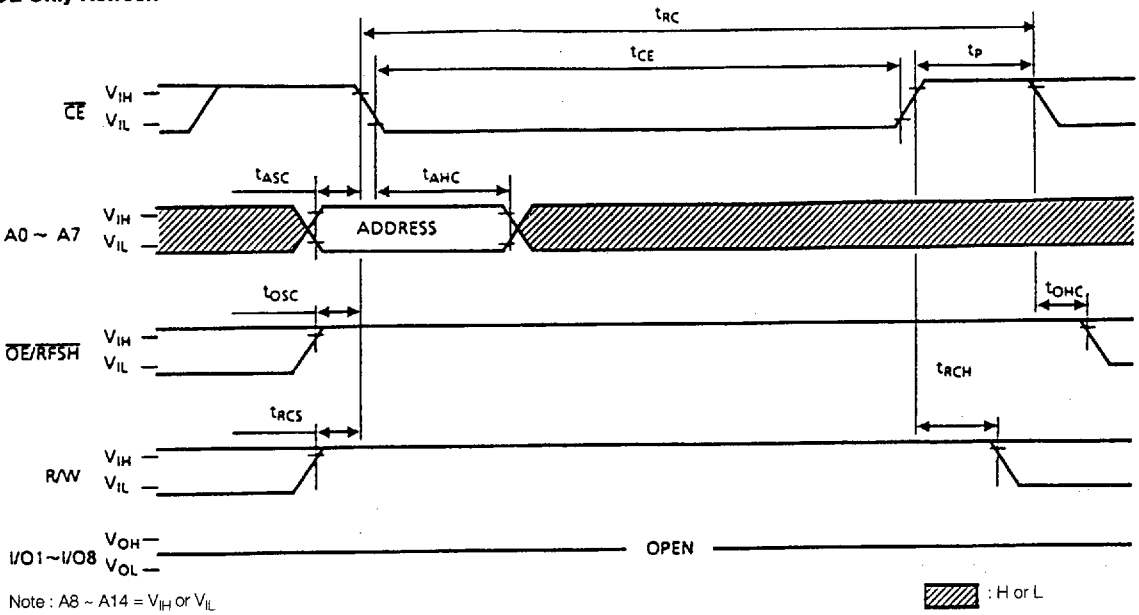
Write Cycle 2 ($\overline{OE}$ Clocked)



Read Modify Write Cycle

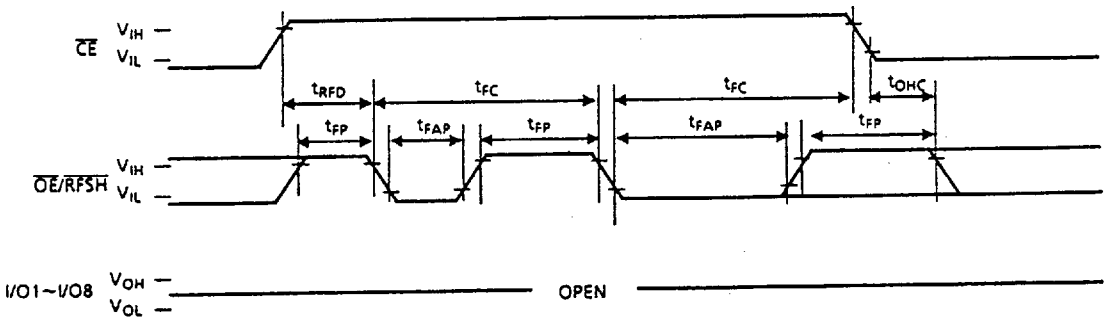


$\overline{CE}$ Only Refresh



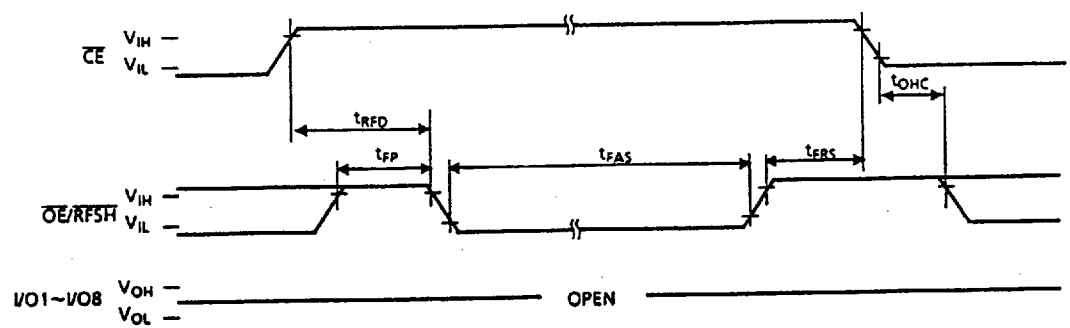
Note : A8 ~ A14 = V_{IH} or V_{IL}

Auto Refresh



Note : R/W, A0 ~ A14 = V_{IH} or V_{IL}

Self Refresh



Note : R/W, A0 ~ A14 = V_{IH} or V_{IL}