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7400 TTL Cells

CMOS Gate Array and Standard Cell Library

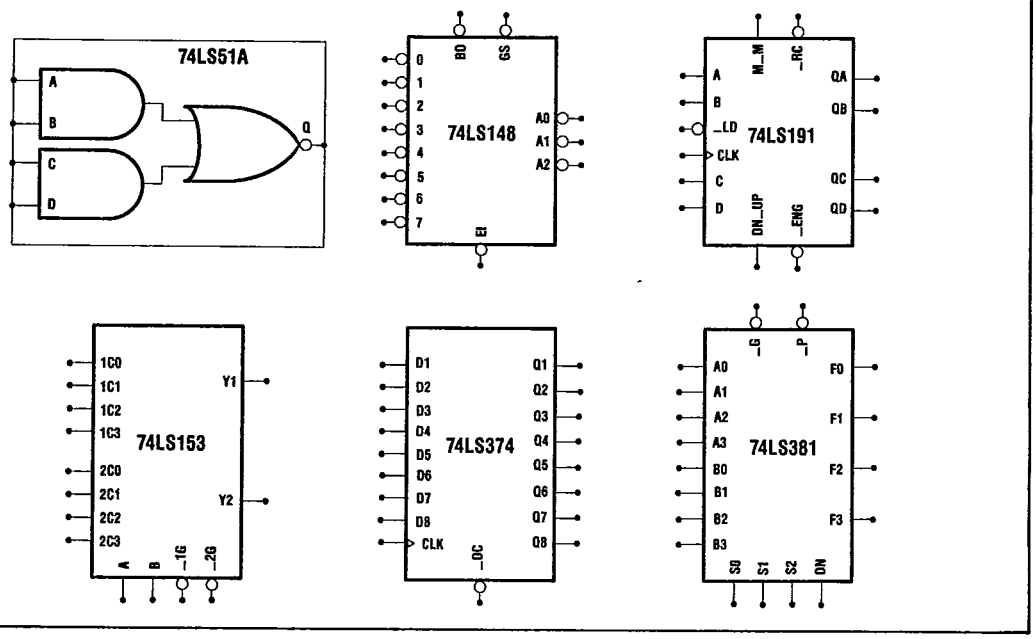
Features

- Over 200 functions available.
- Uses Daisy and Mentor standard parts libraries directly.
- Eases development cycle.
  —Design with familiar 7400 functions.
  —Direct breadboarding is optional.
  —Automatic conversion and simulation with timing for ASIC primitives on workstation.
- Standardized cells allow design first, select process and implementation later.
- Available for Gate Array, Standard Cell, and Analog/Digital Cell implementations.
- Works with 3.0, 2.0, and 1.2 Micron CMOS processes.

General Description

7400 TTL Cells, a member of Gould's EXPERT ASIC™ family of design support tools, are Gould models for all useable 7400 functions resident on the Daisy and Mentor workstations. These models map the 7400 functions into Gould basic functions which are then simulated with the precise timing of the ASIC device that will later be fabricated in silicon. The main advantage of using 7400 TTL Cells is the reduced design time for most system designers that results from familiarity with the 7400 functions. When coupled with Gould's Gate Gobbler™ system for circuit optimization, 7400 TTL Cells give the system designer both short design times and efficient ASIC circuits. Designing with the 7400 TTL Cells, the system designer also has the option to simulate the circuit using the standard part timing and then to verify the design in the system using a breadboard.

Figure 1. Typical 7400 Workstation Symbols



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The basic functions which make up the Gould 7400 TTL Cells are transparent to the Daisy or Mentor workstation user. Schematic capture is done using symbols from the standard parts library on the users workstation. The system designer then determines which simulations, for the standard parts or for the basic ASIC functions or for both, should be done and in what order. When the design is complete, the netlister resident on the Daisy or Mentor Workstation outputs a netlist and test vectors in Gould compatible format which can then be made into prototypes.

The 7400 TTL Cells are available on all Gould process technologies and ASIC implementations, including Gate Array, Standard Cell, and Analog/Digital Cell. The 7400 TTL Cells can also be combined into a schematic and simulated with other Gould library functions including basic functions, MSI functions, Cell Compilers, Analog and Digital Megacells.

Benefits

Gould's 7400 TTL Cells provide the designer with a familiar and extensive set of digital logic functions to use in design. The functions available are de-facto standards in the industry. The symbols for the 7400 TTL Cells are resident on the Daisy or Mentor workstations so the system designer will be using logic elements commonly used for system level design. All this means that there is a minimum of learning time required.

Another aspect is that the designer can have direct assurance that the circuit will work in the system. This is accomplished by simulating with the standard parts on the workstation, then building and testing a breadboard integrated with the rest of the system. This reduces the risk that the ASIC circuit, while performing correctly to its design specification, still fails in the application.

An important advantage of Gould's 7400 TTL Cells is that the design need not be committed to a specific process or to a specific ASIC implementation (Gate Array, Standard Cell, etc.) from the start. System designers can design their circuits first, simulate with the standard parts to verify functionality, and simulate with Gould 7400 TTL Cells to verify timing for ASIC parts.

Table 1. 7400 TTL Functions

Functions	Cells
Simple Gates	15
Complex Gates	7
Non-Inverting and Inverting Drivers	10
Internal Tri-State Drivers	31
Latches	13
Memory	1
Flip Flops	29
Registers	26
Binary Counters	12
Up/Down Counters	12
Miscellaneous Counters	7
Multiplexers	18
Decoders	10
Adders	7
ALU	1
Comparators	4
Priority Encoders	3
Parity Detectors	2
Clock Prescalers	1
Total	209

Since Gould has Gate Array, Standard Cell, and Analog/Digital Cell implementations in several CMOS process technologies (3.0, 2.0 and 1.2-Micron drawn rules), the system designer can simulate in several technologies to insure that a variety of price/performance alternatives are practical for the design. The last step is for the system designer to commit to the specific process and implementation of choice.

Designs with 7400 TTL Cells (alone or in combination with other cells or macros) may be passed through the Gate Gobbler Design System. This is another tool available in Gould's EXPERT ASIC™ family of support tools. Gate Gobbler optimizes the design by reducing gate counts without affecting functionality or performance.

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Table 2. 7400 TTL Cells Available

74LS00	74LS73A	74LS109A	74LS157	74LS190	74LS258B	74LS366	74LS576
74LS02	74LS74	74LS112	74LS158	74LS191	74LS259	74LS366A	74LS577
74LS04	74LS74A	74LS112A	74LS160	74LS192	74LS260	74LS367	74LS595
74LS08	74LS75	74LS113	74LS160A	74LS193	74LS273	74LS367A	74LS597
74LS10	74LS76	74LS113A	74LS161	74LS194	74LS276	74LS368	74LS640
74LS11	74LS76A	74LS114	74LS161A	74LS194A	74LS279	74LS368A	74LS643
74LS13	74LS77	74LS114A	74LS162	74LS195	74LS279A	74LS373	74LS645
74LS14	74LS78	74LS116	74LS162A	74LS195A	74LS279B	74LS374	74LS646
74LS20	74LS82	74LS125	74LS163	74LS196	74LS280	74LS375	74LS648
74LS21	74LS83	74LS125A	74LS163A	74LS197	74LS283	74LS376	74LS651
74LS24	74LS83A	74LS126	74LS164	74LS198	74LS286	74LS377	74LS652
74LS25	74LS85	74LS126A	74LS165	74LS226	74LS290	74LS378	74LS668
74LS27	74LS86	74LS133	74LS166	74LS240	74LS293	74LS379	74LS669
74LS28	74LS90	74LS137	74LS168	74LS241	74LS295	74LS381	74LS670
74LS30	74LS91	74LS138	74LS168A	74LS242	74LS298	74LS390	74LS671
74LS32	74LS92	74LS139	74LS169	74LS243	74LS299	74LS393	74LS672
74LS37	74LS93	74LS139A	74LS169A	74LS244	74LS322	74LS398	74LS684
74LS40	74LS94	74LS147	74LS173	74LS245	74LS323	74LS521	74LS688
74LS42	74LS95	74LS148	74LS173A	74LS251	74LS340	74LS533	74LS697
74LS43	74LS95B	74LS150	74LS174	74LS253	74LS344	74LS534	74LS699
74LS51	74LS96	74LS151	74LS175	74LS256	74LS348	74LS540	74LS805
74LS51A	74LS97	74LS152	74LS176	74LS257	74LS352	74LS541	74LS808
74LS51B	74LS99	74LS153	74LS177	74LS257A	74LS353	74LS544	74LS882
74LS54	74LS107	74LS154	74LS179	74LS257B	74LS363	74LS548	74LS1000
74LS55	74LS107A	74LS155	74LS182	74LS258	74LS365	74LS573	74LS1004
74LS64	74LS109	74LS155A	74LS183	74LS258A	74LS365A	74LS574	74LS1034
74LS73							

This is an important consideration since the 7400 standard parts may contain features which go unused in the ASIC design making it use more silicon area than necessary. The combination of Gould's 7400 TTL Cells and Gate Gobbler provide the system designer with the best of both worlds: Designing with familiar functions and very efficient circuits.

Operation

When the schematic is entered on the workstation, 7400 library elements from the Daisy 7400 TTL Series Library or the Mentor Combined TTL Libraries (LS_LIB) are used alone or combined with library elements from any Gould supplied library to form the ASIC. Typically, workstation software utilities are then invoked to check the integrity of the netlist and report on various characteristics of the design prior to timing simulation. Next, for Mentor workstations, the design is translated and compiled into one of the Gould technologies with a short set of commands that change the library references and add a parameter during EXPAND. For Daisy workstations, the design is compiled during DANCE and DRINK with a user change of pointer in the PROFILE file. Timing simulation then proceeds for either Daisy or Mentor using the workstation supplied utility as with a design captured completely from a Gould supplied library. If the system designer wishes to evaluate the design in another implementation, e.g., in a gate array instead of a standard cell, the steps after schematic capture described above are repeated. When the design is complete, the system designer invokes the Gould Bolt netlister resident on the workstation and it outputs a netlist which can be fabricated into prototype devices by Gould Semiconductor Division.

Specifications

All of the 7400 functions applicable to CMOS ASIC's now available in the Daisy and Mentor standard parts libraries have been included in this release of Gould's 7400 TTL Cells. The 7400 functions not included are

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ASIC CONTINUUM

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those that cannot be included within CMOS core designs, such as circuits with open collector outputs or schmitt trigger inputs. These functions usually have CMOS compatible alternatives which are available. The 7400 functions available as Gould 7400 TTL Cells are listed in Table 2.

Application

7400 TTL Cells are applicable to Gate Array, Standard Cell, and the digital portion of Analog/Digital Cell designs. The Gould 7400 TTL Cells are available on Daisy and Mentor workstations. They can be used alone or together with any other Gould supplied library including Gate Array, Standard Cell, Analog/Digital Cell, Analog Megacells and Digital Megacells. The 7400 TTL Cells can be used with other Gould EXPERT ASIC tools for CAE including NETRANS™ and Gate Gobbler.

Further Information

Information about Gould Semiconductor Division's Standard Products, PEELs, Gate Arrays, Standard Cells, Analog/Digital Cells, and Custom Capabilities is available from your Gould Representative. Contact your Gould representative or Gould Semiconductor Division headquarters for information on the EXPERT ASIC tools including Gate Gobbler and NETRANS.