CS8352

Multi–Function Triple Regulator/Controller with $\overline{\text{RESET}}$

This multiple output voltage regulator/controller is intended for use in microprocessor based automotive, instrumentation systems which utilize serial gauge drivers. The device contains a 5.0 V, 50 mA standby voltage regulator, a 14 V predriver which controls an external P–Channel MOSFET pass transistor, a 5.0 V predriver which controls an external PNP pass transistor, and a low side driver which may be used to drive an external PNP. The device also contains several I/O ports and a low voltage $\overline{\text{RESET}}$ function which senses the output voltage of the 5.0 V standby regulator.

The $\overline{\text{RESET}}$ monitor point differentiates this part from the CS8351.

Features

- 5.0 V ± 2%, 50 mA Voltage Regulator
- 5.0 V ± 4% Controller
- 14 V ± 4% Controller
- 5.0 V $\overline{\text{RESET}}$
- I/O Buffers
- Thermal Protection
- Overvoltage Shutdown
- Low Side Driver
- Low Quiescent Current

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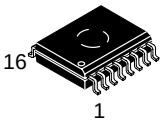
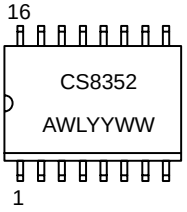


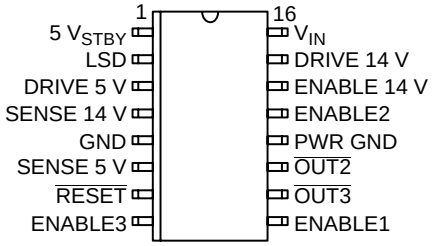
SO–16L
DW SUFFIX
CASE 751G

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS8352XDW16	SO–16L	46 Units/Rail
CS8352XDWR16	SO–16L	1000 Tape & Reel

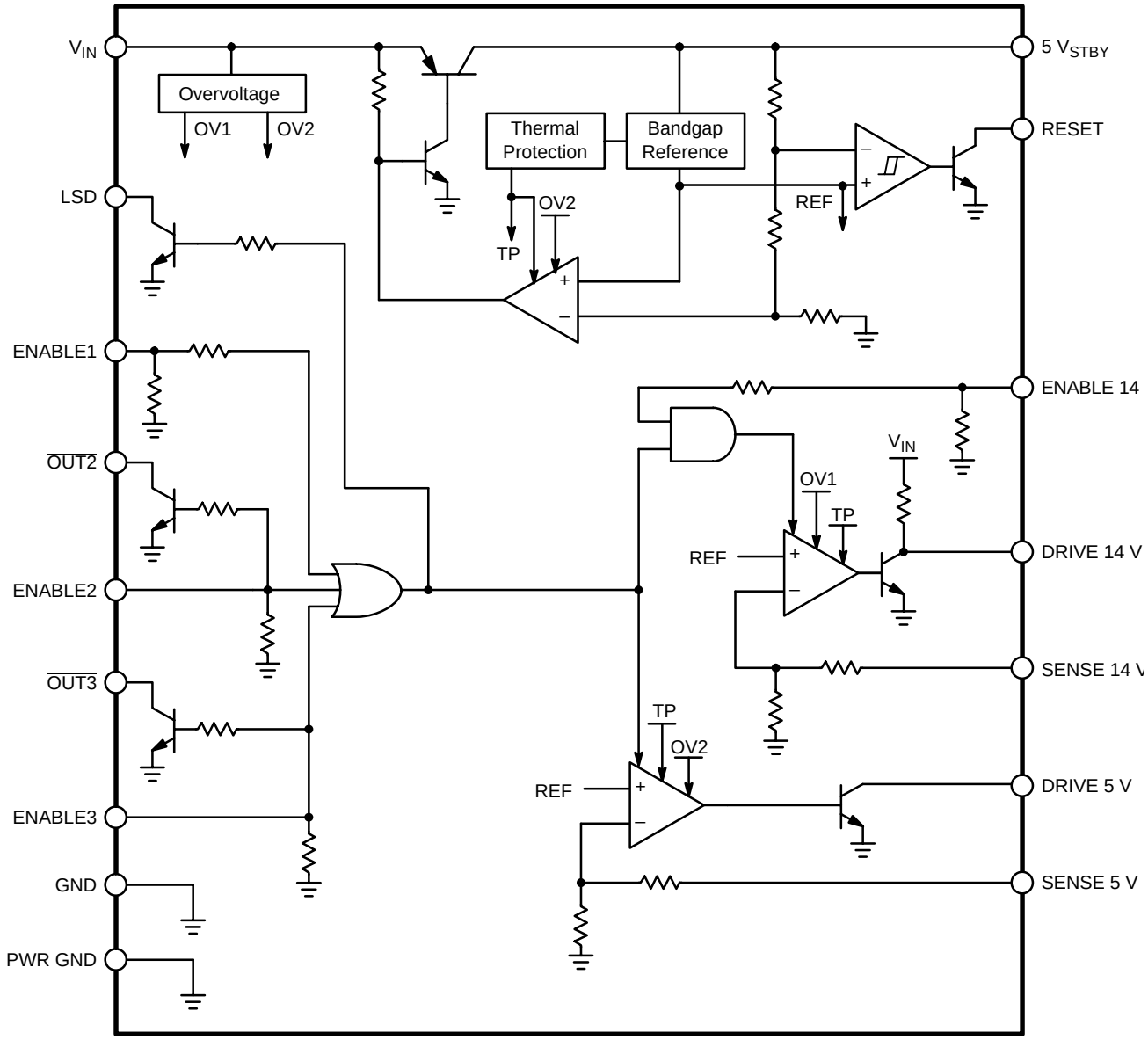


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
V_{IN}, ENABLE2, ENABLE3, DRIVE 14 V, DRIVE 5 V, OUT1, OUT2, OUT3	–0.3 to 45	V
SENSE 14 V	–0.3 to 18	V
5 V_{STBY}, ENABLE1, ENABLE 14 V, $\overline{RESET}$, SENSE 5 V	–0.3 to 7.0	V
Maximum Junction Temperature	–40 to +150	°C
ESD (Human Body Model)	2.0	kV
Θ_{JA} (16 lead, 300 mil, SOIC)	105	°C/W
P_D @ T_A = 105°C	429	mW
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1.)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +105°C, 9.0 V ≤ V_{BAT} ≤ 16 V; unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
General					
Supply Current	Active	–	4.0	10	mA
Supply Current	Standby Mode, I(5 V_{STBY}) = 100 μA	–	125	250	μA
5.0 V Standby Regulator					
Output Voltage	I_{OUT} ≤ 50 mA, 7.0 V ≤ V_{IN} ≤ 26 V	4.9	5.0	5.1	V
Current Limit	–	50	150	225	mA
Thermal Protection	–	160	–	–	°C
Overvoltage Shutdown (OV2)	–	30	34	38	V
Line Regulation	I_{OUT} = 1.0 mA	–	–	50	mV
Load Regulation	V_{IN} = 14 V, 50 μA ≤ I_{OUT} ≤ 50 mA	–	–	50	mV
PSRR	V_{IN} = 14 V + 1.0 V_{PP} @ 120 Hz	60	–	–	dB
Dropout Voltage	I_{OUT} ≤ 50 mA	–	–	0.6	V
5.0 V Pre–Regulator					
Sense Regulation Voltage	–	4.8	5.0	5.2	V
Sense Input Impedance	Note 2.	–	20	–	kΩ
5.0 V Drive Current	–	–	–	–12	mA
Overvoltage Shutdown (OV2)	–	30	34	38	V
14 V Pre–Regulator					
Sense Regulation Voltage	–	13.4	14	14.6	V
14 V Sense Input Impedance	Note 2.	–	16.75	–	kΩ
Drive 14 V Output High	I_{OH} = 100 μA	V_{BAT} – 0.5	–	–	V
Drive 14 V Output Low	I_{OL} = –100 μA	–	–	1.5	V
Overvoltage Shutdown (OV1)	–	16.9	17.75	18.6	V
$\overline{\text{RESET}}$ Function (5 V_{STBY})					
$\overline{\text{RESET}}$ Threshold	–	4.5	–	4.85	V
$\overline{\text{RESET}}$ Hysteresis	–	10	20	50	mV
Output Low Voltage	I_{OL} = –8.0 mA, SENSE 5 V = 4.0 V I_{OL} = –2.0 mA, SENSE 5 V = 4.0 V I_{OL} = –100 μA, SENSE 5 V = 1.0 V I_{OL} = –100 μA, SENSE 5 V ≥ 1.8 V, V_{DD} ≤ 1.0 V	– – – –	– – – –	1.0 0.4 0.4 0.4	V V V V
Low Side Driver (LSD)					
Output Low Voltage	I_{OL} = –50 mA	–	–	1.5	V
Overvoltage Shutdown	–	30	34	38	V
ENABLE Functions (ENABLE1, ENABLE2, ENABLE3, ENABLE 14 V)					
Threshold High	–	2.5	–	–	V
Threshold Low	–	–	–	0.8	V
Input Current	V_{ENABLE} = 2.5 V	–	25	50	μA
Pulldown Resistance	Note 2.	–	160	–	kΩ
Output Buffers ($\overline{\text{OUT2}}$, $\overline{\text{OUT3}}$)					
Output Low Voltage	I_{OL} = –1.0 mA	–	–	0.5	V

2. Not production tested, for information only.

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SO–16L	PIN SYMBOL	FUNCTION
1	5 V_{STBY}	5.0 V Standby regulator output voltage.
2	LSD	Low side driver (may be used to drive an external PNP).
3	DRIVE 5 V	5.0 V Pre–regulator's output which provides bias to an external PNP transistor.
4	SENSE 14 V	14 V Pre–regulator's feedback input which senses the drain voltage on the external P–Channel MOSFET.
5	GND	Ground reference.
6	SENSE 5 V	5.0 V Pre–regulator's feedback input which senses the collector voltage on the external PNP.
7	$\overline{\text{RESET}}$	Open collector output which is activated when the 5 V_{STBY} voltage drops below the reset threshold voltage.
8	ENABLE3	Input which enables the OUT3 output, the 5.0 V pre–regulator, and the LSD.
9	ENABLE1	Input which enables the 5.0 V pre–regulator and the LSD.
10	$\overline{\text{OUT3}}$	Open collector output controlled by ENABLE3.
11	$\overline{\text{OUT2}}$	Open collector output controlled by ENABLE2.
12	PWR GND	Ground reference for high current portions of the chip.
13	ENABLE2	Input which enables the OUT2 output, the 5.0 V pre–regulator, and the LSD.
14	ENABLE 14 V	Enable input for the 14 V pre–regulator. Note: ENABLE1, ENABLE2, or ENABLE3 must also be asserted to enable the 14 V pre–regulator.
15	DRIVE 14 V	14 V Pre–regulator's output which provides drive to an external P–Channel MOSFET.
16	V_{IN}	Input supply voltage.

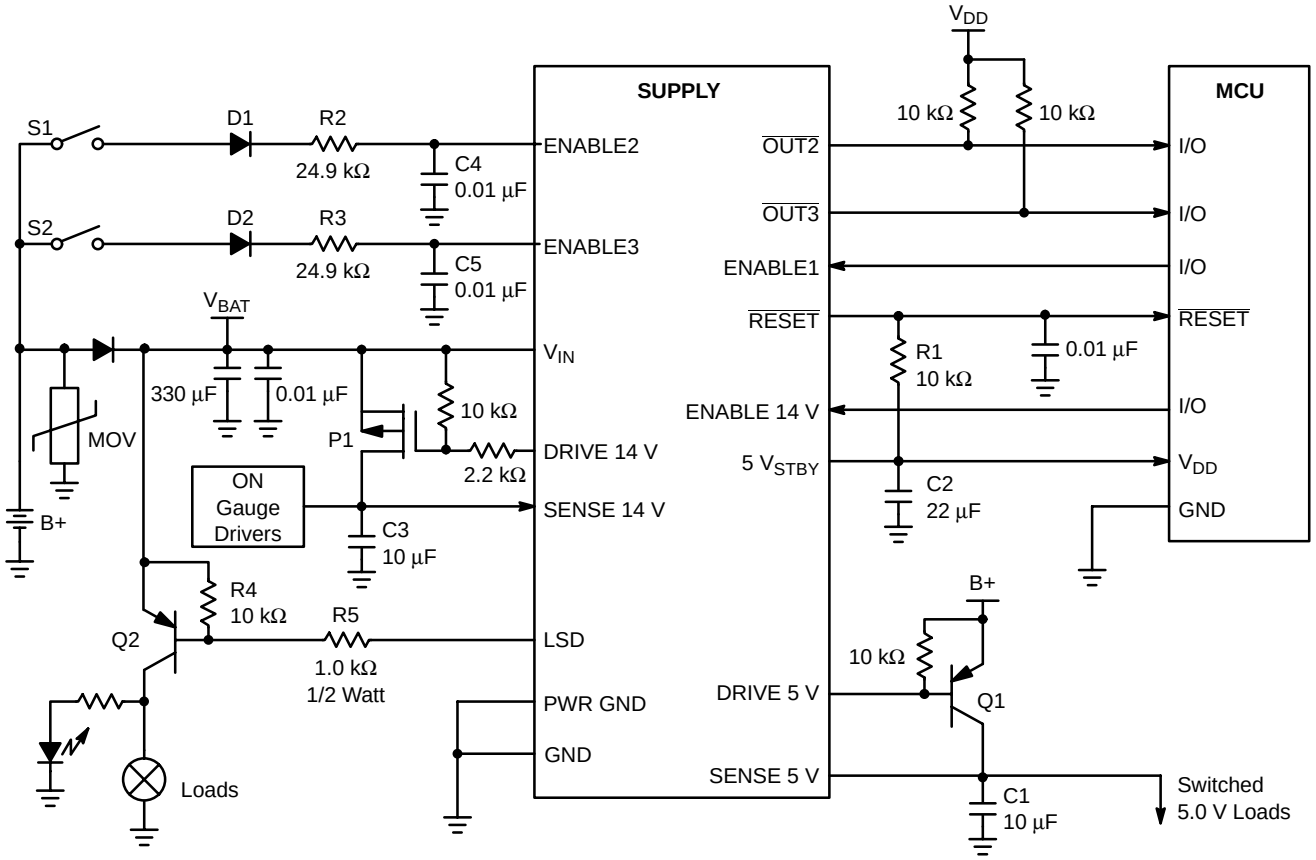


Figure 2. Application Diagram. Note: Fast Recovery Diodes (D1 and D2) Are Needed to Insure Proper Operation During Negative EMC Transients If the Inputs Are Switched Battery Inputs.

CIRCUIT DESCRIPTION

5.0 V, 50 mA Standby Regulator

The standby regulator operates continuously when power is applied to V_{IN}. It is suitable for continuous battery connection since it only consumes 250 µA with a 100 µA load and will withstand a 45 V load dump condition. It contains overvoltage shutdown (30 V), current limit and thermal protection. The low voltage reset function is configured to monitor this output voltage.

5.0 V Pre–Regulator

The 5.0 V pre–regulator contains all the necessary circuitry to implement a series pass regulator with the exception of the external PNP pass transistor. The pre–regulator provides a minimum of 12 mA of base drive to the external PNP. It includes a precise resistor divider to monitor the output voltage and the error amplifier to compare the divided voltage to an internal precision voltage reference. The pre–regulator is enabled by either ENABLE1, ENABLE2, or ENABLE3. Its overvoltage shutdown is set to 30 V (minimum).

14 V Pre–Regulator

This pre–regulator contains all the necessary circuitry to implement a series pass regulator with the exception of an external P–Channel MOSFET. The overvoltage shutdown threshold is set to 16.9 V (minimum). The ENABLE 14 V input activates this regulator while DRIVE 14 V provides the drive to the gate. Note: ENABLE1, ENABLE2, or ENABLE3 must also be asserted to enable the 14 V pre–regulator.

Low Voltage Reset

The low voltage reset function is configured to monitor the 5.0 V standby regulator's output voltage. It provides an active low open collector output when the regulator's voltage is below the reset threshold (typically 4.7 V).

As an alternative, the CS8351 offers a low voltage reset function to monitor the output voltage of the 5.0 V controller.

50 mA Low Side Driver

An open collector Darlington output is provided to bias an external power transistor. This stage is activated when ENABLE1, ENABLE2 or ENABLE3 is asserted. The output is disabled during an overvoltage condition (30 V minimum).

Input/Output Buffers

Two level shifting buffers are provided to convert a logic state referenced to battery to a logic state referenced to 5.0 V. OUT2 is controlled by ENABLE2. OUT3 is controlled by ENABLE3. The ENABLE2 and ENABLE3 inputs each have an internal 160 kΩ (typical) pull down resistor. An external resistor divider can be connected to the input to elevate the threshold of the buffer.

APPLICATIONS INFORMATION

5.0 V Standby Regulator

The standby regulator will require a capacitor connected between its output and Ground.

Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start–up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

A 10 μF capacitor should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in Step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat Steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in Step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in Step 3 above.

5.0 V Pre–Regulator

Since this stage is a pre–regulator, an external pass transistor must be selected to deliver the desired output current, withstand the maximum expected input voltage, and dissipate the resulting power. The base of the external PNP is connected to the DRIVE 5 V lead. The emitter is connected to the battery supply. The collector is connected to the SENSE 5 V input to feedback the output voltage to the error amplifier.

The base drive output current at DRIVE 5 V will be inversely proportional to the output voltage sensed 5 V. A capacitor is also required between SENSE 5 V and ground to provide a stable output voltage. The same procedure can be used to select the capacitor as outlined in the standby regulator section. A pull up resistor is also required between the base and emitter of the PNP. This resistor prevents the external PNP from leaking while the pre–regulator is disabled. It also improves the turn off of the PNP during an overvoltage transient.

14 V Pre–Regulator

An external pass transistor is required for this regulator. For automotive applications where the input voltage is typically 14 V, an external P–Channel MOSFET is recommended for the pass transistor since it will usually operate as a saturated switch. This occurs when the regulator operates in dropout (i.e., the input voltage falls below the intended regulation voltage). If a PNP were used, excessive base drive current would be required to support the load current since the gain of a saturated PNP is low. The excessive base current needed would develop excessive

power dissipation across the CS8352. Therefore, the P–Channel MOSFET is recommended.

Most P–Channel MOSFETs have a maximum gate to source voltage rating of 15 V. Therefore, a resistor divider should be added to the gate as shown in the application diagram. Since the CS8352 will disable the 14 V pre–regulator when the input voltage reaches 18.6 V (maximum), the resistor divider should be selected to limit $V_{GS} \leq 15$ V at $V_{IN} = 18.6$ V while providing sufficient gate drive when V_{IN} is low.

A capacitor is required between SENSE 14 V and Ground to provide a stable output voltage. The same procedure can be used to select the capacitor as outlined in the standby regulator section. If regulation at 14 V is not required this output may be configured as a high side driver by shorting the SENSE 14 V pin to ground. This configuration allows the removal of the output capacitor. The overvoltage shutdown circuit will continue to function normally in this mode.

Low Voltage Reset, $\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up or when V_{OUT} drops out of regulation. A hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

An external RC network on the $\overline{\text{RESET}}$ lead (Figure 3) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT}C_{RST} = \left[\frac{-t_{Delay}}{\ln\left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}}\right)}\right]$$

where:

$R_{TOT} = R_{RST}$ in parallel with R_{IN}

$R_{IN} = \mu$P port impedance

$C_{RST} = \overline{\text{RESET}}$ Delay capacitor

t_{Delay} = desired delay time

$V_{RST} = V_{SAT}$ of $\overline{\text{RESET}}$ lead (0.7 V @ turn – ON)

$V_T = \mu$P logic threshold voltage

$R_{RST} \geq 2.7$ kΩ

Adding C_{RST} will slightly increase the time $\overline{\text{RESET}}$ goes low since the $\overline{\text{RESET}}$ output will have to discharge the energy stored on C_{RST}.

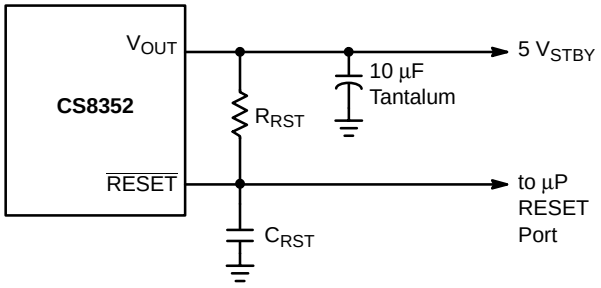
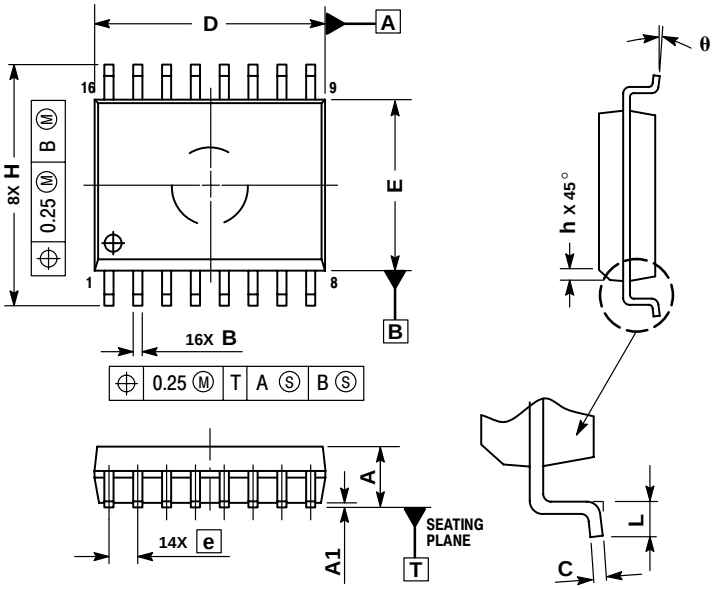


Figure 3. RC Network for $\overline{\text{RESET}}$ Delay

PACKAGE DIMENSIONS

SO–16L
DWF SUFFIX
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PACKAGE THERMAL DATA

Parameter		SO–16L	Unit
$R_{\Theta JC}$	Typical	23	°C/W
$R_{\Theta JA}$	Typical	105	°C/W

PUBLICATION ORDERING INFORMATION

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