DESCRIPTION

Preliminary

The Hynix HY5V26C(L/S)F is a 134,217,728bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY5V26C(L/S)F is organized as 4banks of 2,097,152x16

HY5V26C(L/S)F is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8, or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

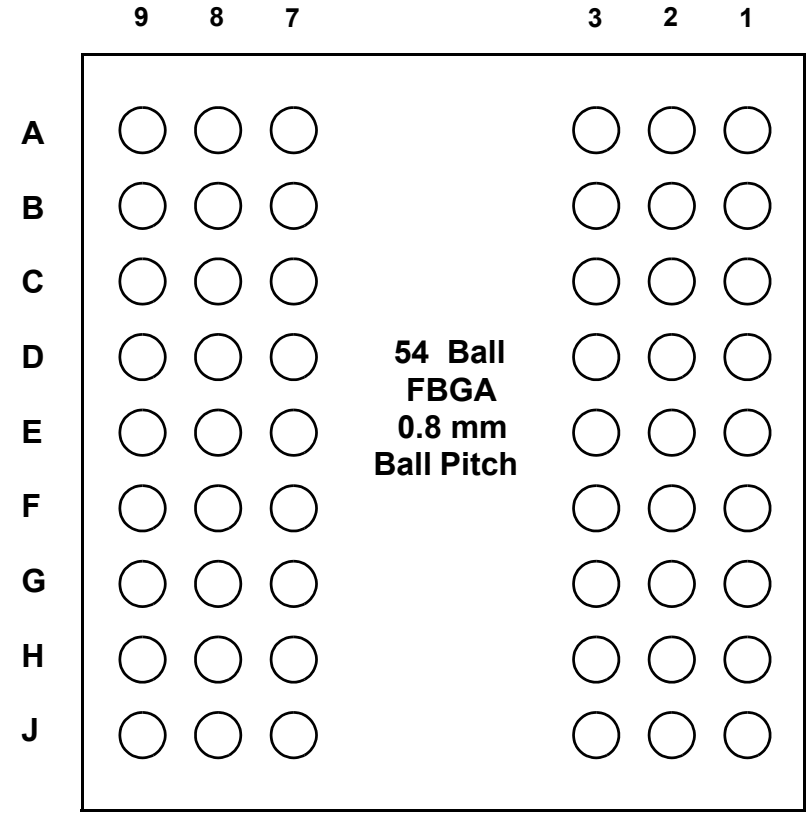
FEATURES

- Single 3.3±0.3V power supply
- All device balls are compatible with LVTTL interface
- 54Ball FBGA (10.5mm x 8.3mm)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

ORDERING INFORMATION

Part No.	Clock Frequency	Power	Organization	Interface	Package
HY5V26CF-6	166MHz	Normal	4Banks x 2Mbits x16	LVTTL	54ball FBGA
HY5V26CF-K	133MHz				
HY5V26CF-H	133MHz				
HY5V26CF-8	125MHz				
HY5V26CF-P	100MHz				
HY5V26CF-S	100MHz				
HY5V26C(L/S)F-6	166MHz	Low power			
HY5V26C(L/S)F-K	133MHz				
HY5V26C(L/S)F-H	133MHz				
HY5V26C(L/S)F-8	125MHz				
HY5V26C(L/S)F-P	100MHz				
HY5V26C(L/S)F-S	100MHz				

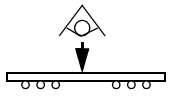
BALL CONFIGURATION



< Bottom View >

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
NC	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

< Top View >

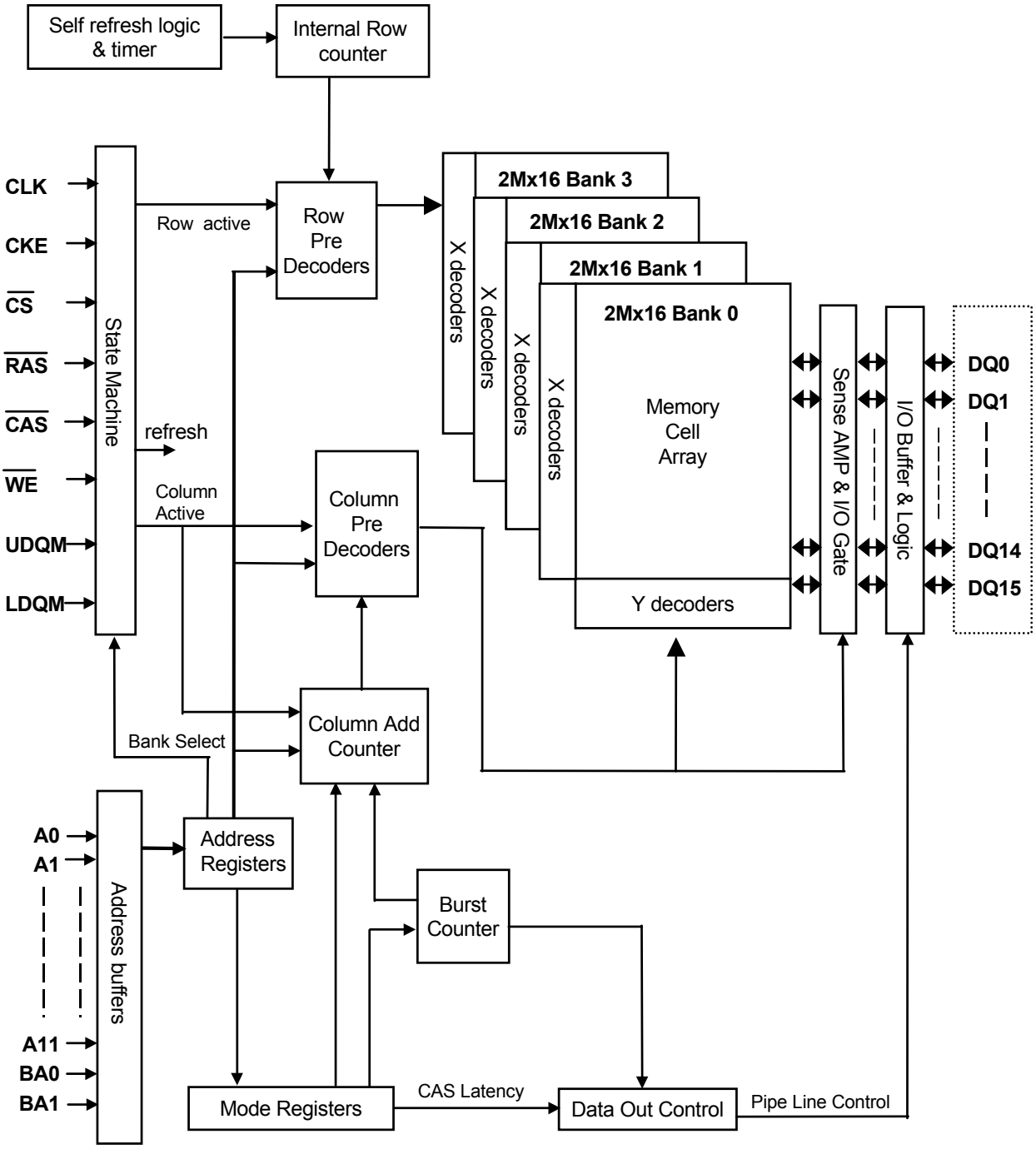


BALL DESCRIPTION

BALL OUT	SYMBOL	TYPE	DESCRIPTION
F2	CLK	INPUT	Clock : The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
F3	CKE	INPUT	Clock Enable : Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
G9	$\overline{CS}$	INPUT	Chip Select : Enables or disables all inputs except CLK, CKE, UDQM and LDQM
G7,G8	BA0, BA1	INPUT	Bank Address : Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0 ~ A11	INPUT	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA8 Auto-precharge flag : A10
F8, F7, F9	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
F1, E8	UDQM, LDQM	INPUT	Data Mask:Controls output buffers in read mode and masks input data in write mode
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0 ~ DQ15	I/O	Data Input/Output:Multiplexed data input/output ball
A9, E7, J9, A1, E3, J1	VDD/VSS	SUPPLY	Power supply for internal circuits
A7, B3, C7, D3, A3, B7, C3, D7	VDDQ/ VSSQ	SUPPLY	Power supply for output buffers
E2, G1	NC	-	No connection

FUNCTIONAL BLOCK DIAGRAM

2Mbit x 4banks x 16 I/O Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any ball relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability.

DC OPERATING CONDITION (T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	1
Input High voltage	V_{IH}	2.0	3.0	V_{DDQ} + 0.3	V	1,2
Input Low voltage	V_{IL}	-0.3	0	0.8	V	1,3

Note :
1.All voltages are referenced to V_{SS} = 0V
2.V_{IH}(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.V_{IL}(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

AC OPERATING TEST CONDITION (T_A=0 to 70°C, V_{DD}=3.3±0.3V, V_{SS}=0V)

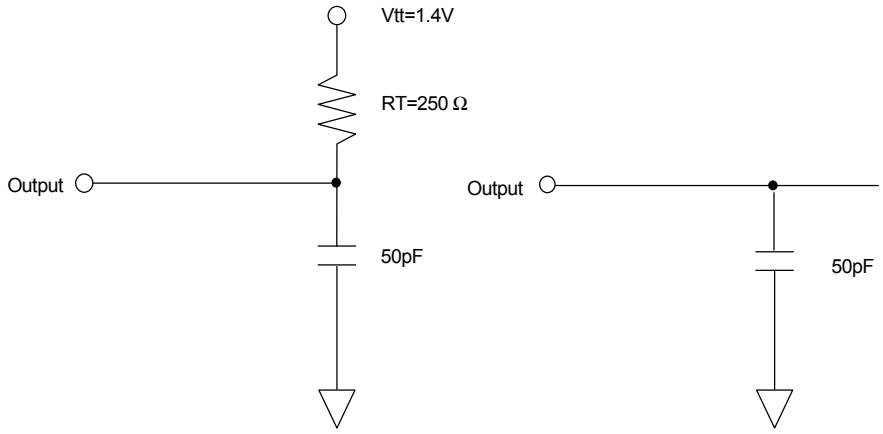
Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	V_{IH} / V_{IL}	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	C_L	50	pF	1

Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	ball	Symbol	-6/K/H		-8/P/S		Unit
			Min	Max	Min	Max	
Input capacitance	CLK	C_{I1}	2.5	3.5	2.5	4.0	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM	C_{I2}	2.5	3.8	2.5	5.0	pF
Data input / output capacitance	DQ0 ~ DQ15	$C_{I/O}$	4.0	6.5	4.0	6.5	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit AC Output Load Circuit

DC CHARACTERISTICS I (TA=0 to 70°C, V_{DD}=3.3±0.3V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	I_{LI}	-1	1	uA	1
Output Leakage Current	I_{LO}	-1	1	uA	2
Output High Voltage	V_{OH}	2.4	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +2mA

Note :
1.V_{IN} = 0 to 3.6V, All other balls are not tested under V_{IN} =0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6

DC CHARACTERISTICS II (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

Parameter	Symbol	Test Condition		Speed						Unit	Note
				-6	-K	-H	-8	-P	-S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		130	120	120	120	110	110	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns		2						mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		1							
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 30ns. All other balls ≥ VDD-0.2V or ≤ 0.2V		15						mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		15							
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns		5						mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		5							
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 30ns. All other balls ≥ VDD-0.2V or ≤ 0.2V		30						mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		20							
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	CL=3	150	130	130	130	110	110	mA	1
			CL=2	160	140	140	140	120	120		
Auto Refresh Current	IDD5	tRRC ≥ tRRC(min), All banks active		240	220	220	200	200	200	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		2						mA	3
				800						uA	4
				500						uA	5

Note :

1.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2.Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II
3.HY5V26CF-6/K/H/8/P/S
4.HY5V26CLF-6/K/H/8/P/S
5.HY5V26CSF-6/K/H/8/P/S

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-K		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	tCK3	6	1000	7.5	1000	7.5	1000	8	1000	10	1000	10	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	10		7.5		10		10		10		12		ns	
Clock High Pulse Width		tCHW	2.5	-	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	2.5	-	2.5	-	3	-	3	-	3	-	ns	1
Access Time From Clock	$\overline{CAS}$ Latency = 3	tAC3	-	5.4	-	5.4	-	5.4	-	6	-	6	-	6	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	6	-	5.4	-	6	-	6	-	6	-	6	ns	
Data-Out Hold Time		tOH	2.7	-	2.7	-	2.7	-	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	1.5	-	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	0.8	-	1	-	1	-	1	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	1	-	1	-	1	-	1	-	ns	
CLK to Data Output in High-Z Time	$\overline{CAS}$ Latency = 3	tOHZ3	2.7	5.4	2.7	5.4	2.7	5.4	3	6	3	6	3	6	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	2.7	5.4	2.7	5.4	3	6	3	6	3	6	3	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns
If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter

2.Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

AC CHARACTERISTICS II

Parameter		Symbol	-6		-K		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time	Operation	tRC	60	-	60	-	65	-	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	60	-	65	-	65	-	68	-	70	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	18	-	15	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ Active Time		tRAS	42	100K	45	100K	45	100K	48	100K	50	100K	50	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	18	-	15	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	12	-	15	-	15	-	16	-	20	-	20	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	2	-	2	-	2	-	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	5	-	4	-	5	-	4	-	3	-	3	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	3	-	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	2	-	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	1	-	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	-	64	ms	

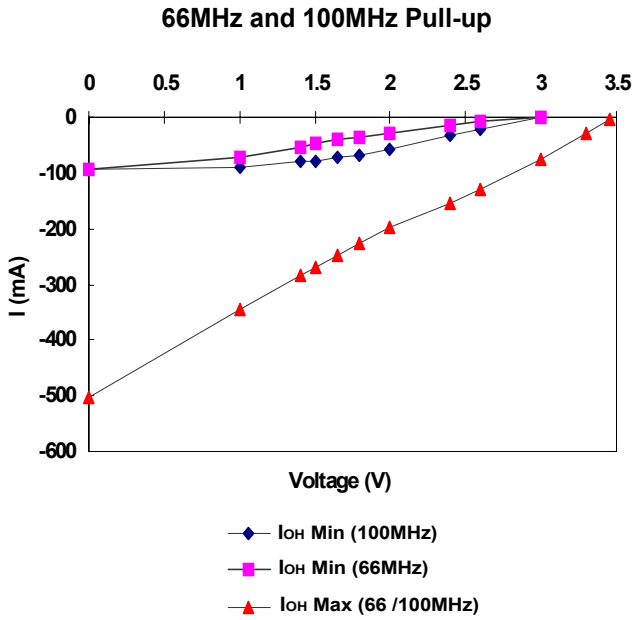
Note :

1. A new command can be given tRRC after self refresh exit

IBIS SPECIFICATION

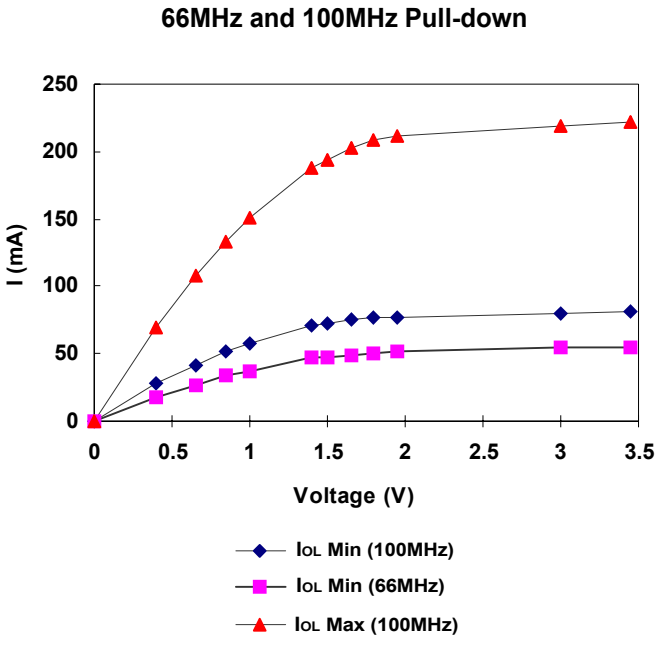
IOH Characteristics (Pull-up)

Voltage	100MHz (Min)	100MHz (Max)	66MHz (Min)
(V)	I(mA)	I(mA)	I(mA)
3.45		-2.4	
3.3		-27.3	
3.0	0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73	-248	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0	-93	-502.4	-93



IOL Characteristics (Pull-down)

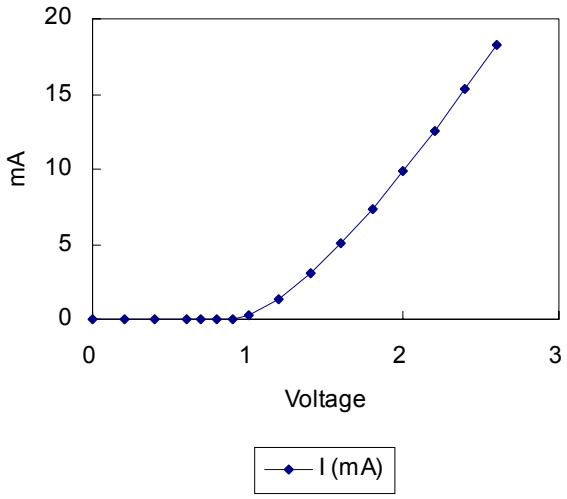
Voltage	100MHz (Min)	100MHz (Max)	66MHz (Min)
(V)	I(mA)	I(mA)	I(mA)
0	0	0	0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9



VDD Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VDD (V)	I(mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

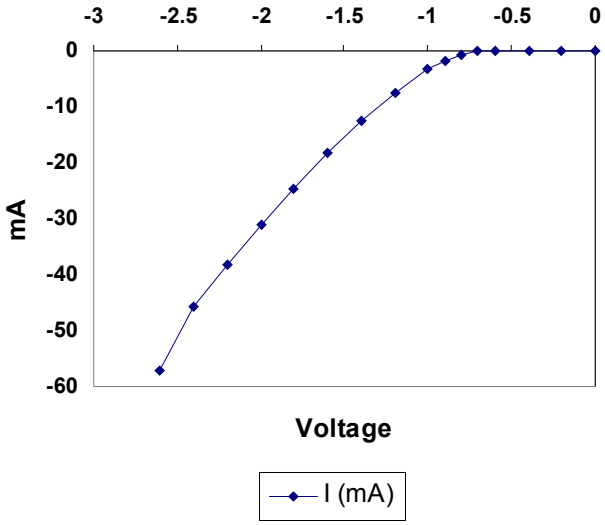
Minimum VDD clamp current (Referenced to VDD)



Vss Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

VSS (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum Vss clamp current



DEVICE OPERATING OPTION TABLE

HY5V26C(L/S)F-6

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
166MHz(6ns)	3CLKs	3CLKs	7CLKs	10CLKs	3CLKs	5.4ns	2.7ns
143MHz(7ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
133MHz(7.5ns)	2CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns

HY5V26C(L/S)F-K

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	2CLKs	2CLKs	6CLKs	8CLKs	2CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY5V26C(L/S)F-H

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
133MHz(7.5ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	5.4ns	2.7ns
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns

HY5V26C(L/S)F-8

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz(8ns)	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HY5V26C(L/S)F-P

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HY5V26C(L/S)F-S

	CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz(10ns)	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz(12ns)	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz(15ns)	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	H	X	A9 ball High (Other balls OP code)			
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :
1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

PACKAGE INFORMATION

54 Ball 0.8mm pitch 8.3mm x 10.5mm FBGA