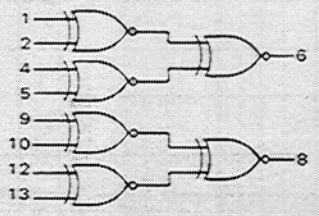
DUAL 4-BIT PARITY-TREE

MC4310
MC4010

JULY 1971

Add Suffix F for TO-86 ceramic package (Case 607).
Suffix L for TO-116 ceramic package (Case 632).
Suffix P for TO-116 plastic package (Case 605) MC4010 only.



V_{CC} = Pin 14
Gnd = Pin 7

Positive Logic:
6 = 1⊙2⊙4⊙5
where $X \odot Y = (\overline{X} \cdot \overline{Y}) + (X \cdot Y)$

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 125 mW typ/pkg

Three Exclusive NOR gates are connected together to form each of the two 4-bit parity trees in the package. An even number of logic "1" states on the inputs will result in a logic "1" output state. An odd parity checker can be made by connecting an inverter to the output of the device.

TYPICAL PROPAGATION DELAY TIMES

FIGURE 1 – DELAY versus TEMPERATURE

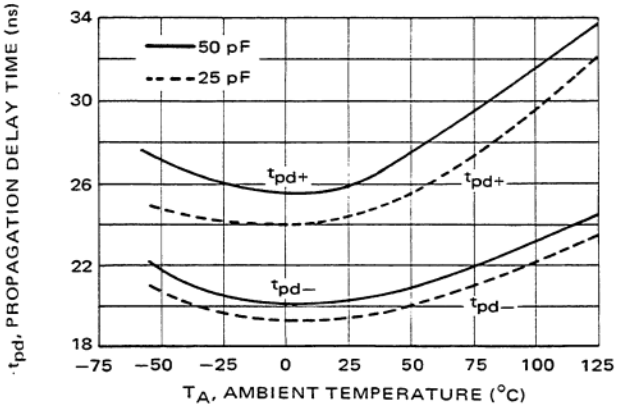


FIGURE 2 – DELAY versus LOAD CAPACITANCE

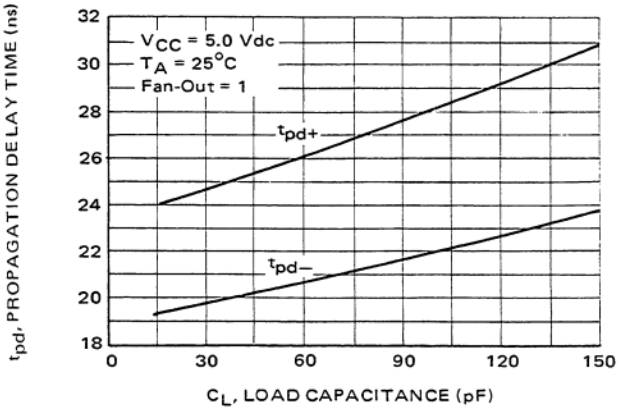
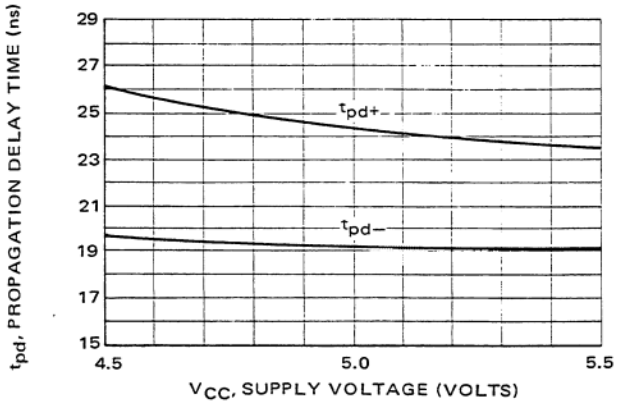
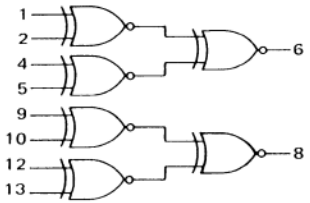


FIGURE 3 – DELAY versus SUPPLY VOLTAGE



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input and one output. Test other inputs and output in the same manner. To complete testing, test all input-output combinations according to the logic equation.



	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}
MC4310	−55°C	16	18.4	−1.6	–	–	1.1	2.0	0.4	2.4	4.0	–	5.0	4.5	5.5	–
	+25°C	16	18.4	−1.6	1.0	−10	1.1	1.8	0.4	2.4	4.0	7.0	5.0	4.5	5.5	2.4
	+125°C	16	18.4	−1.6	–	–	0.8	1.8	0.4	2.4	4.0	–	5.0	4.5	5.5	–
MC4010	0°C	16	17.6	−1.6	–	–	1.1	2.0	0.4	2.5	4.0	–	5.0	4.75	5.25	–
	+25°C	16	17.6	−1.6	1.0	−10	1.1	1.8	0.4	2.5	4.0	7.0	5.0	4.75	5.25	2.4
	+75°C	16	17.6	−1.6	–	–	0.9	1.8	0.4	2.5	4.0	–	5.0	4.75	5.25	–

Characteristic	Symbol	Pin Under Test	MC4310 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4010 Test Limits 0°C Min	0°C Max	+25° Min	+25° Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	I_{in}	I_D	V_{IL}	V_{IH}	V_F	V_R	V_{RH}	V_{max}	V_{CC}	V_{CCL}	V_{CCH}	V_{IHX}	Gnd
Input																														
Forward Current	I_F	1	–	−3.2	–	−3.2	–	−3.2	–	−3.2	–	−3.2	–	−3.2	mAdc	–	–	–	–	–	–	–	1	–	2	–	–	–	14	–	7
Leakage Current	I_R	1	–	80	–	80	–	80	–	80	–	80	–	80	μAdc	–	–	–	–	–	–	–	–	1	–	–	–	–	14	–	2,7
Breakdown Voltage	BV_{in}	1	–	–	5.5	–	–	–	–	–	5.5	–	–	–	Vdc	–	–	–	1	–	–	–	–	–	–	–	–	–	14	–	2,7
Clamp Voltage	V_D	1	–	–	–	−1.5	–	–	–	–	–	1.5	–	–	Vdc	–	–	–	–	1	–	–	–	–	–	–	–	14	–	–	7
Output																														
Output Voltage	V_{OL}	6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	6	–	–	–	–	1,4,5	2	–	–	–	–	–	–	14	–	7
		6	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	Vdc	–	6	–	–	–	1,4,5	2	–	–	–	–	–	14	–	–	7
	V_{OH}	6	2.4	–	2.4	–	2.4	–	2.5	–	2.5	–	2.5	–	Vdc	–	–	6	–	–	1,2,4,5	–	–	–	–	–	–	14	–	–	7
Short-Circuit Current	I_{SC}	6	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	−20	−65	mAdc	–	–	–	–	–	1,2,4,5	–	–	–	–	–	–	14	–	–	6,7
Power Requirements (Total Device)																														
Maximum Power Supply Current	I_{max}	14	–	–	–	55	–	–	–	–	–	55	–	–	mAdc	–	–	–	–	–	–	–	–	–	2,4,5 10,12,13	14	–	–	–	–	1,7,9
Power Supply Drain	I_{PD}	14	–	–	–	44	–	–	–	–	–	44	–	–	mAdc	–	–	–	–	–	–	–	–	–	2,4,5 10,12,13	–	14	–	–	–	1,7,9
Switching Parameters																Pulse In		Pulse Out													
Turn-On Delay	t_{pd-1}	1,6	–	–	–	35	–	–	–	–	–	35	–	–	ns	1		6		–	–	–	–	–	–	–	14	–	–	2,4,5,10,12,13	7
Turn-Off Delay	t_{pd+1}	1,6	–	–	–	35	–	–	–	–	–	35	–	–	ns	1		6		–	–	–	–	–	–	–	14	–	–	2,4,5,10,12,13	7

INPUT AND OUTPUT LOADING FACTORS
with respect to MTTL and MDTL families

FAMILY	MC4310 INPUT LOADING FACTOR	MC4310 OUTPUT LOADING FACTOR
MC4300	1.0	10
MC500	1.2	12
MC2100	0.8	8
MC3100	0.8	8
MC5400	1.0	10
MC930	1.0*	10

FAMILY	MC4010 INPUT LOADING FACTOR	MC4010 OUTPUT LOADING FACTOR
MC4000	1.0	10
MC400	1.0	10
MC2000	0.67	6
MC3000	0.7	8
MC7400	1.0	10
MC830	1.15*	12

*Applies only when input is being driven by MDTL gate with 2.0 kilohm pullup resistor. Logic "1" state drive limitations of gates with 6.0 kilohm pullup resistors reduce drive capability to fan-out of 3.

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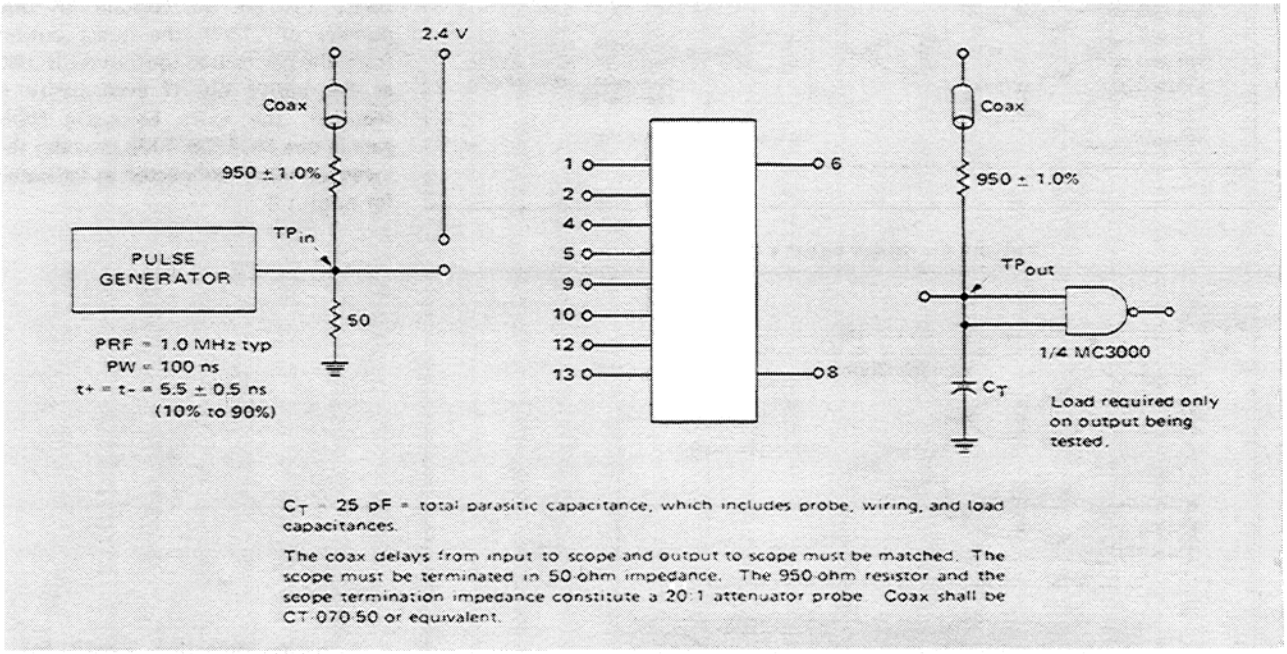
SWITCHING TIME TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS

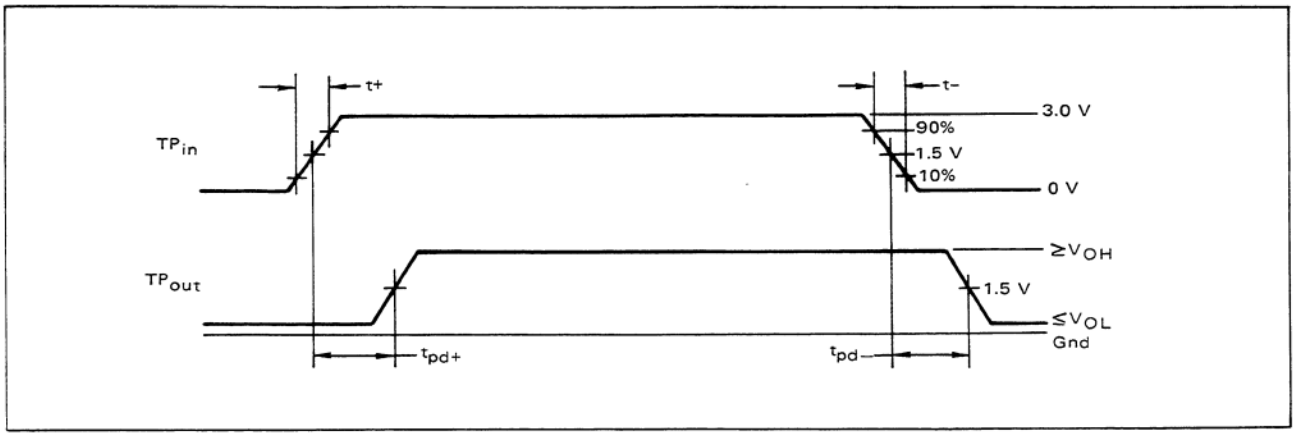
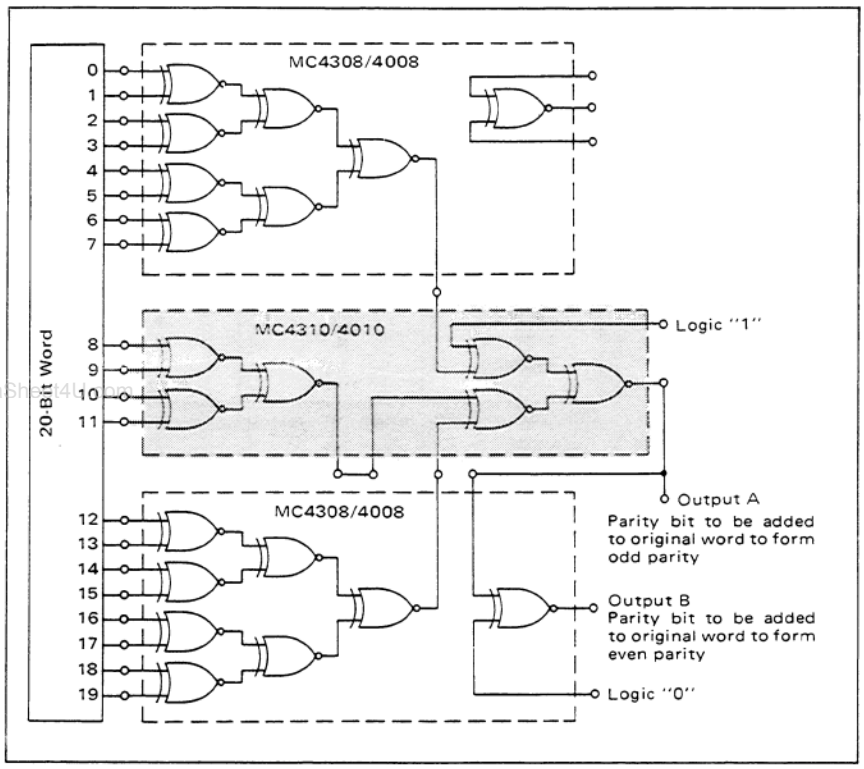


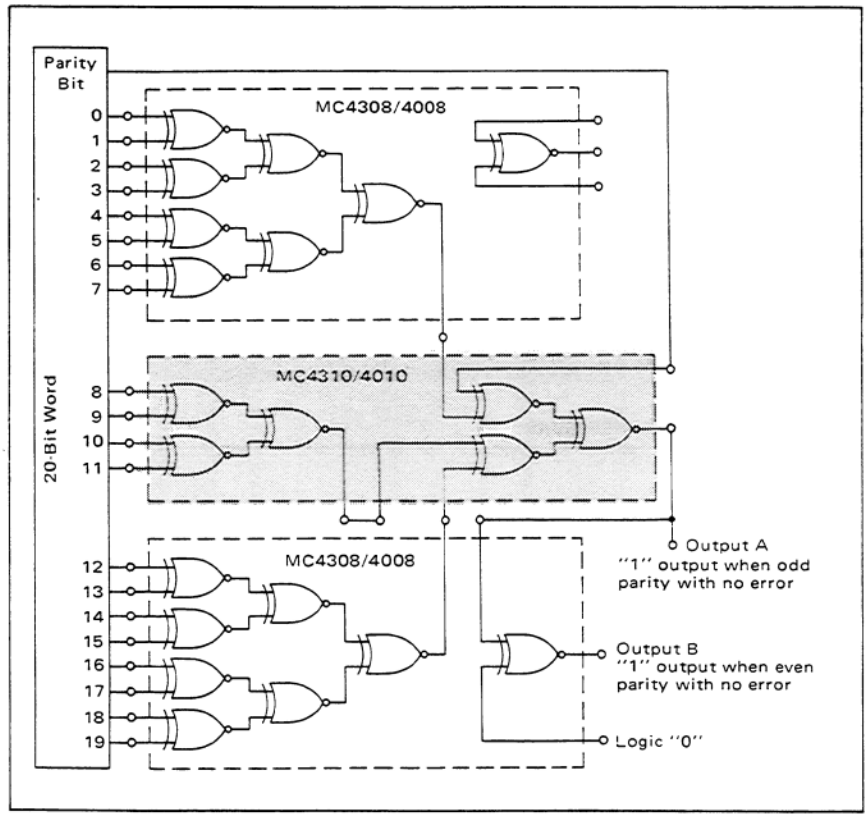
FIGURE 4 – 20-BIT PARITY GENERATOR



APPLICATIONS INFORMATION

A parity generation tree (simple parity) for a 20-bit word is shown in Figure 4. It uses two MC4308/4008 8-bit parity trees and one MC4310/4010 dual 4-bit parity tree. If a parity word containing odd parity is required (i.e., the 20-bit word plus the parity bit are to contain an odd number of "1's"), the direct output from the parity tree (output A) is used as the parity bit. If even parity is required, the extra Exclusive NOR gate in one MC4308/4008 provides the inversion when connected as indicated for output B.

FIGURE 5 – 20-BIT PARITY DETECTOR



A parity detection circuit for a 20-bit word is shown in Figure 5. The 20-bit word is connected to a two-stage parity tree identical to that used for the 20-bit parity generator; however, for the detection circuit the output of the tree must be compared with the input parity bit. The parity bit serves as an input to the second stage of the tree. For odd parity detection, output A will be a logic "1" if no error has occurred. For even parity detection, a logic "1" will appear at output B if no error has been introduced. Longer word lengths can be examined in a similar manner.

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MC4310/D