NSTB1002DXV5T1G, NSTB1002DXV5T5G

Preferred Devices

Dual Common Base-Collector Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSTB1002DXV5T1G series, two complementary devices are housed in the SOT−553 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- These are Pb−Free Devices

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Rating	Symbol	Value Q1	Value Q2	Unit
Collector-Base Voltage	V_{CBO}	−40	50	Vdc
Collector-Emitter Voltage	V_{CEO}	−40	50	Vdc
Collector Current	I_C	−200	100	mAdc

THERMAL CHARACTERISTICS

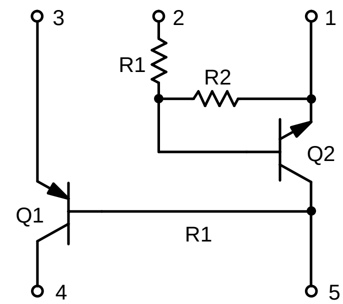
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance − Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/°C
Thermal Resistance − Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

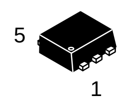
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR−4 @ Minimum Pad

ON Semiconductor®

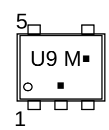
http://onsemi.com





SOT−553
CASE 463B

MARKING DIAGRAM



U9 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NSTB1002DXV5T1G	SOT−553 (Pb−Free)	4 mm pitch 4000/Tape & Reel
NSTB1002DXV5T5G	SOT−553 (Pb−Free)	2 mm pitch 8000/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

January, 2006 − Rev. 0

Publication Order Number:
NSTB1002DXV5/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

Q1 TRANSISTOR: PNP
OFF CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Breakdown Voltage (Note 2)	$V_{(BR)CEO}$	−40	−	Vdc
Collector−Base Breakdown Voltage	$V_{(BR)CBO}$	−40	−	Vdc
Emitter−Base Breakdown Voltage	$V_{(BR)EBO}$	−5.0	−	Vdc
Base Cutoff Current	I_{BL}	−	−50	nAdc
Collector Cutoff Current	I_{CEX}	−	−50	nAdc

ON CHARACTERISTICS (Note 2)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc) (I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc) (I_C = −10 mAdc, V_{CE} = −1.0 Vdc) (I_C = −50 mAdc, V_{CE} = −1.0 Vdc) (I_C = −100 mAdc, V_{CE} = −1.0 Vdc)	h_{FE}	 60 80 100 60 30	 − − 300 − −	−
Collector−Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{CE(sat)}$	 − −	 −0.25 −0.4	Vdc
Base−Emitter Saturation Voltage (I_C = −10 mAdc, I_B = −1.0 mAdc) (I_C = −50 mAdc, I_B = −5.0 mAdc)	$V_{BE(sat)}$	 −0.65 −	 −0.85 −0.95	Vdc

SMALL−SIGNAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Current−Gain − Bandwidth Product	f_T	250	−	MHz
Output Capacitance	C_{obo}	−	4.5	pF
Input Capacitance	C_{ibo}	−	10.0	pF
Input Impedance (V_{CE} = −10 Vdc, I_C = −1.0 mAdc, f = 1.0 kHz)	h_{ie}	2.0	12	kΩ
Voltage Feedback Ratio (V_{CE} = −10 Vdc, I_C = −1.0 mAdc, f = 1.0 kHz)	h_{re}	0.1	10	X 10^{-4}
Small−Signal Current Gain (V_{CE} = −10 Vdc, I_C = −1.0 mAdc, f = 1.0 kHz)	h_{fe}	100	400	−
Output Admittance (V_{CE} = −10 Vdc, I_C = −1.0 mAdc, f = 1.0 kHz)	h_{oe}	3.0	60	μmhos
Noise Figure (V_{CE} = −5.0 Vdc, I_C = −100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	nF	−	4.0	dB

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = −3.0 Vdc, V_{BE} = 0.5 Vdc)	t_d	−	35	ns
Rise Time	(I_C = −10 mAdc, I_{B1} = −1.0 mAdc)	t_r	−	35	
Storage Time	(V_{CC} = −3.0 Vdc, I_C = −10 mAdc)	t_s	−	225	ns
Fall Time	(I_{B1} = I_{B2} = −1.0 mAdc)	t_f	−	75	

Q2 TRANSISTOR: NPN

OFF CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	−	−	100	nAdc
Collector-Emitter Cutoff Current (V_{CB} = 50 V, I_B = 0)	I_{CEO}	−	−	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0, I_C = 5.0 mA)	I_{EBO}	−	−	0.1	mAdc

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	−	−	Vdc
Collector-Emitter Breakdown Voltage (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	−	−	Vdc
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	h_{FE}	80	140	−	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)	$V_{CE(SAT)}$	−	−	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	−	−	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	V_{OH}	4.9	−	−	Vdc
Input Resistor	R1	33	47	61	kΩ
Resistor Ratio	R1/R2	0.8	1.0	1.2	

2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

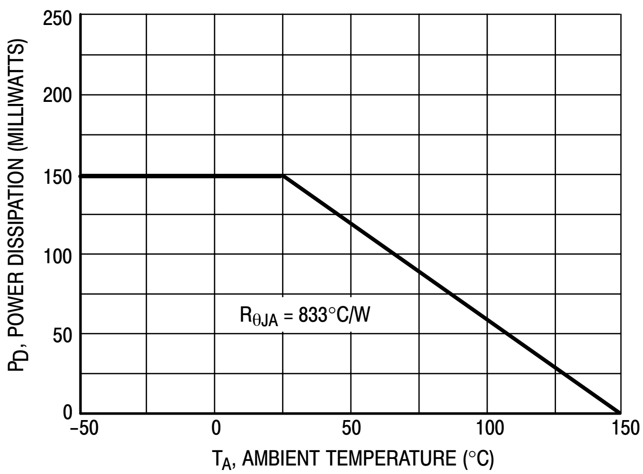


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS — PNP TRANSISTOR

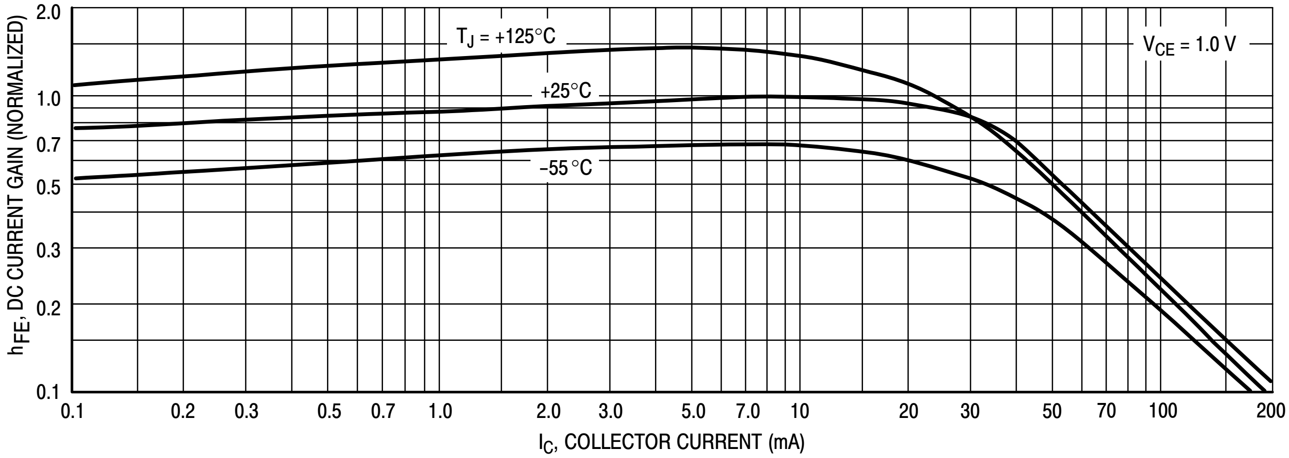


Figure 2. DC Current Gain

TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

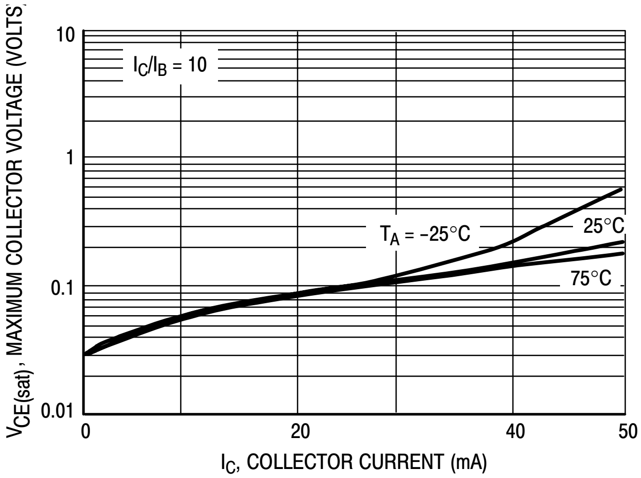


Figure 3. $V_{CE(sat)}$ versus I_C

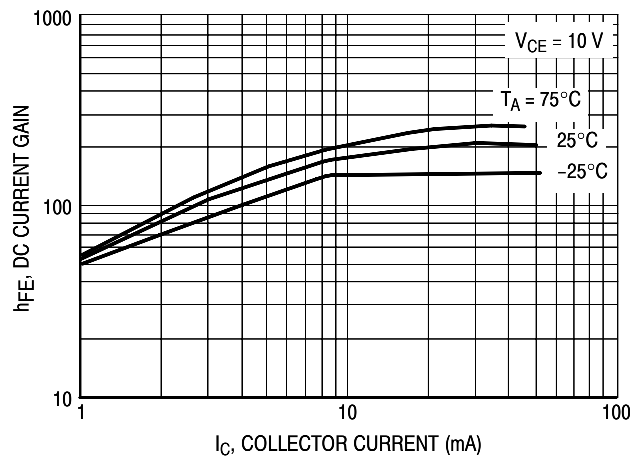


Figure 4. DC Current Gain

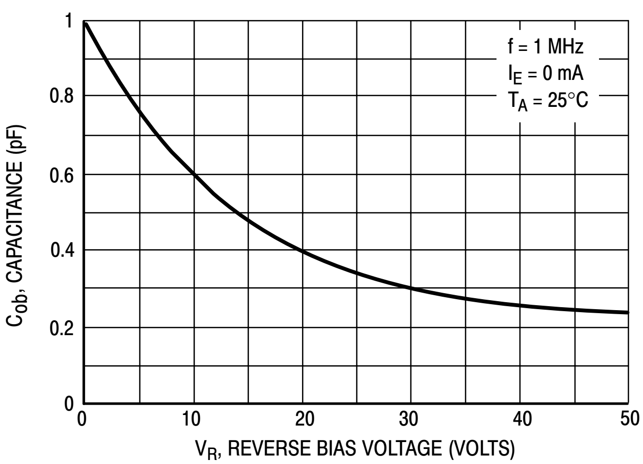


Figure 5. Output Capacitance

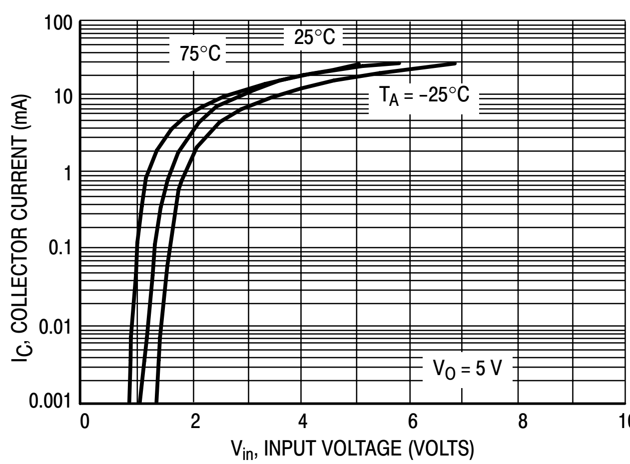


Figure 6. Output Current versus Input Voltage

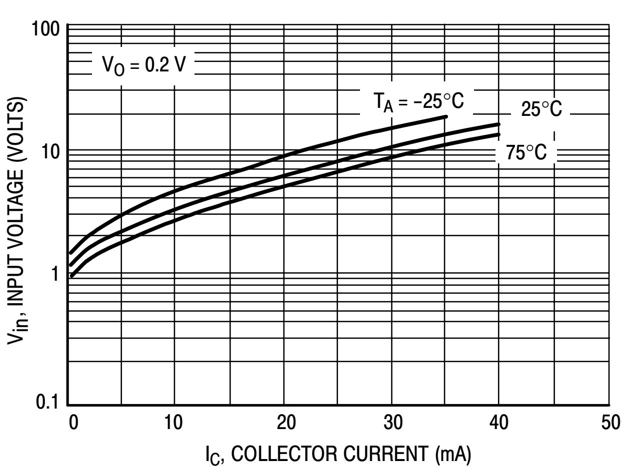
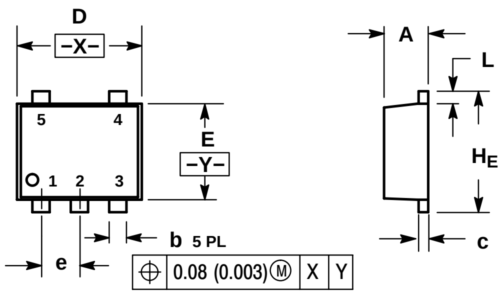


Figure 7. Input Voltage versus Output Current

PACKAGE DIMENSIONS

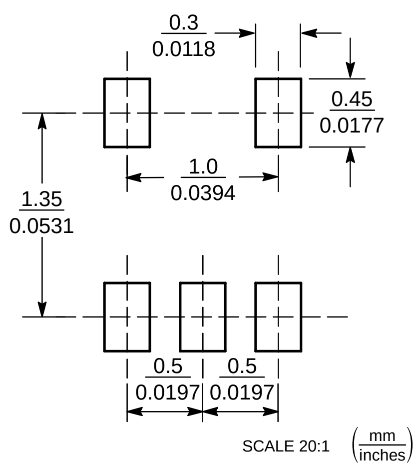
SOT−553
XV5 SUFFIX
CASE 463B−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.063	0.067

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.