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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2727

Silicon N Channel MOS FET High Speed Power Switching

RENESAS

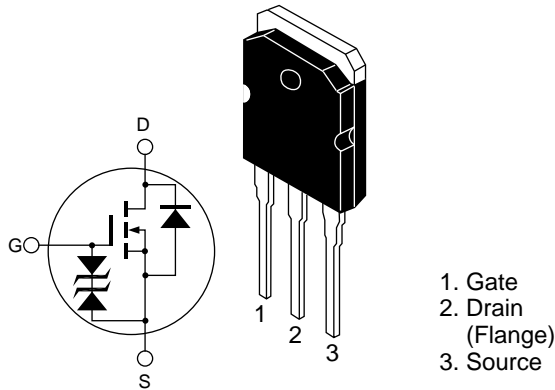
ADE-208-526A (Z)
2nd. Edition
Jul. 1997

Features

- Low on-resistance
- High speed switching
- Low drive current
- Avalanche ratings

Outline

TO-3P



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}^{*1}$	40	A
Body to drain diode reverse drain current	I_{DR}	10	A
Avalanche current	I_{AP}^{*3}	10	A
Avalanche energy	E_{AR}^{*3}	5.55	mJ
Channel dissipation	Pch^{*2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

- Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
 2. Value at $Tc = 25^\circ C$
 3. Value at $Tch = 25^\circ C$, $Rg \geq 50\Omega$

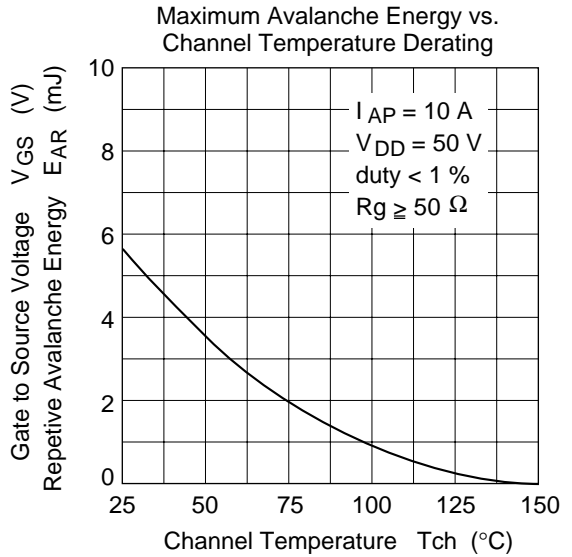
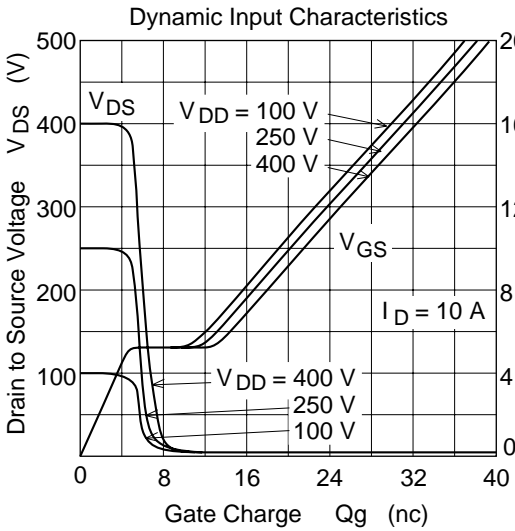
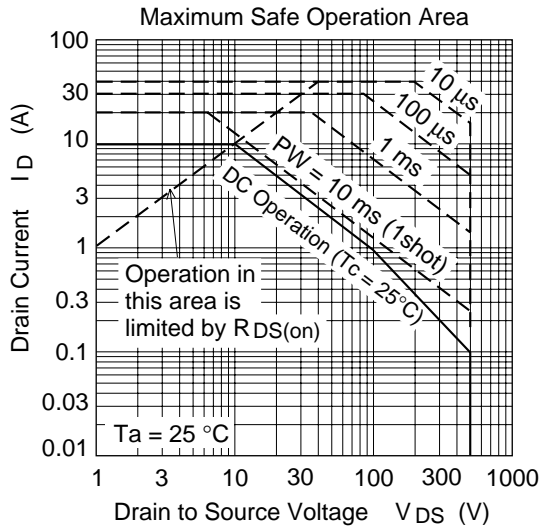
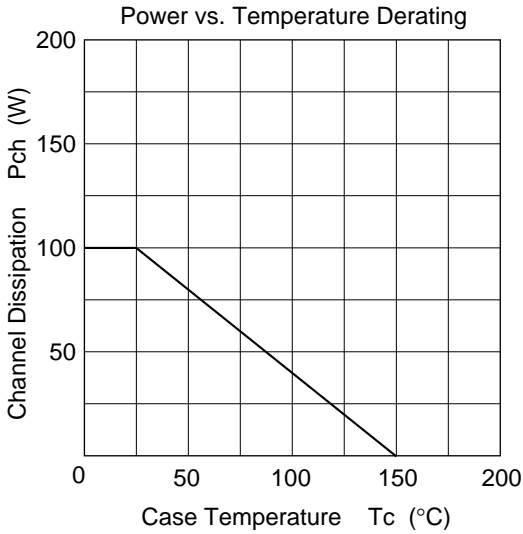
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 25\text{V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500\text{V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.5	—	3.5	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.75	0.95	Ω	$I_D = 5\text{A}$, $V_{GS} = 10\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	4.2	7.0	—	S	$I_D = 5\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	Ciss	—	1100	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	Coss	—	330	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	65	—	pF	f = 1MHz
Total gate charge	Qg	—	21	—	nc	$V_{DD} = 400\text{V}$
Gate to source charge	Qgs	—	5	—	nc	$V_{GS} = 10\text{V}$
Gate to drain charge	Qgd	—	8	—	nc	$I_D = 10\text{A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10\text{V}$, $I_D = 5\text{A}$
Rise time	t_r	—	70	—	ns	$R_L = 6\Omega$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	
Fall time	t_f	—	50	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	$I_D = 10\text{A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	300	—	ns	$I_F = 10\text{A}$, $V_{GS} = 0$ $diF/dt = 100\text{A}/\mu\text{s}$

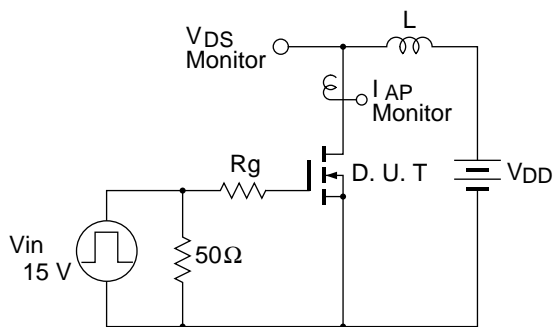
Note: 1. Pulse test

See characteristics curves of 2SK2726

Main Characteristics

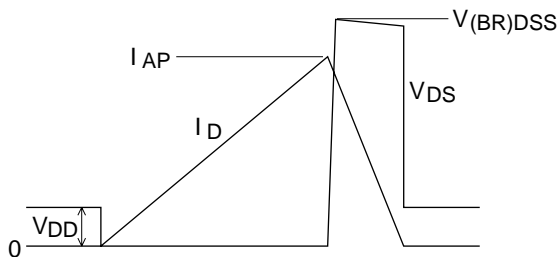


Avalanche Test Circuit

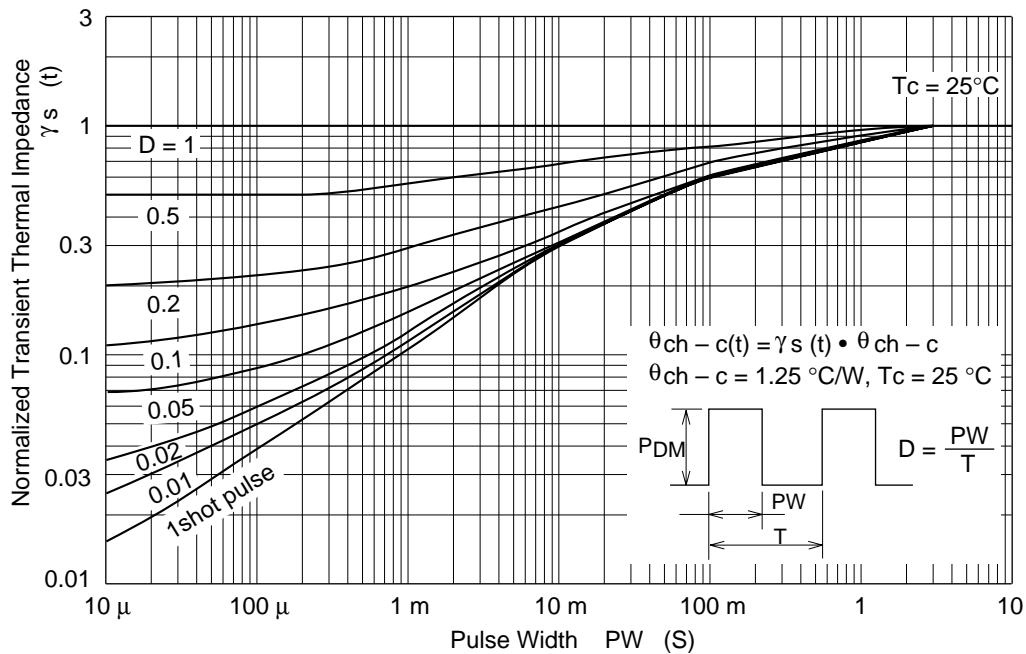


Avalanche Waveform

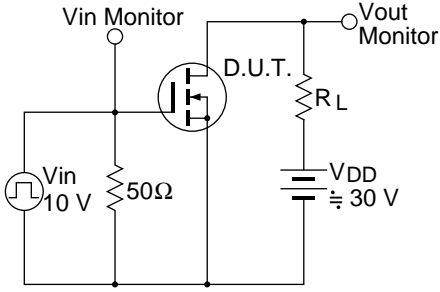
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



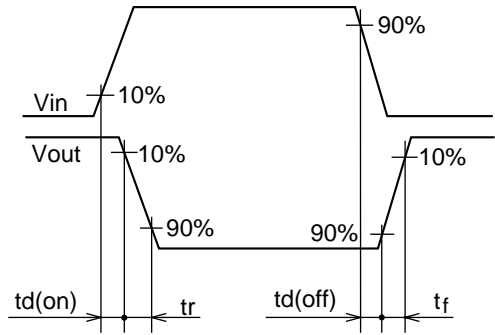
Normalized Transient Thermal Impedance vs. Pulse Width



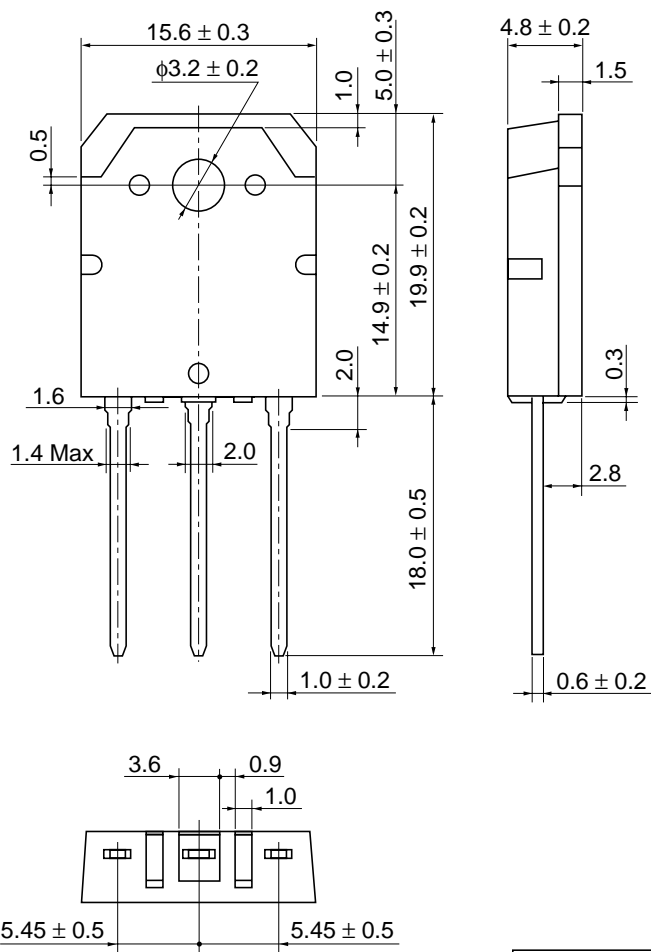
Switching Time Test Circuit



Switching Time Waveforms

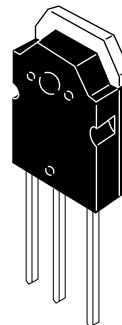


Package Dimensions



As of January, 2001

Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

Cautions

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