NEC

User's Manual

IE-V850E-MC-EM1-B, IE-V850E-MC-MM2 (Sold separately)

In-Circuit Emulator Option Boards

Target Device
V850E1 (NB85E Core)

Document No. U14482EJ2V0UM00 (2nd edition)
Date Published November 2000 N CP(K)

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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INTRODUCTION

Target Readers

This manual is intended for users who wish to design and develop application systems using the V850E1 (NB85E core).

Purpose

This manual is intended to give users an understanding of the basic specifications of the IE-V850E-MC-EM1-B and its correct usage method.

Organization

The contents of this manual are broadly divided into the following sections.

- Outline
- Parts and functions
- Cautions

How to Use This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical circuits, logic circuits, and microcontrollers. The IE-V850E-MC-EM1-B is used connected to the IE-V850E-MC-A in-circuit emulator. This manual describes the basic setup procedure and the IE-V850E-MC-EM1-B switch settings.
For the parts and functions of the IE-V850E-MC-A and details about the connection of component parts, refer to the **IE-V850E-MC-A User's Manual (U14487E)**.

To learn about the basic specifications and usage method:
→ Read in the order listed in **CONTENTS**.

To learn about software-related settings for the IE-V850-MC-A and IE-V850E-MC-EM1-B, including the operation procedure and command functions
→ Refer to the user's manual of the debugger (sold separately) to be used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary…xxxx or xxxxB
	Decimal…xxxx
	Hexadecimal…xxxxH

Prefixes representing a power of 2 (address space, memory capacity)

K (Kilo): $2^{10} = 1024$

M (Mega): $2^{20} = 1024^2$

Terms

The meanings of terms used in this manual are listed below.

Target device	This is the device to be emulated.
Target system	The system to be debugged (system created by user). This includes the target program and hardware created by the user.

Related Documents When using this manual, refer to the following manuals.
The related documents listed below may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
IE-V850E-MC, IE-V850E-MC-A (In-Circuit Emulator)		U14487E
IE-V850E-MC-EM1-B, IE-V850E-MC-MM2 (sold separately) (In-Circuit Emulator Option Boards)		This manual
CA830, CA850 (C compiler package)	Operation	U13998E
	C Language	U13997E
	Project Manager	U13996E
CA850 (C Compiler Package)	Assembly Language	U13828E
ID850 (Ver. 2.00 or later) (Integrated Debugger)	Operation Windows Based	U14217E
SM850 (Ver. 2.00 or later) (System Simulator)	Operation Windows Based	U13759E
RX850 (Real-Time OS)	Basics	U13430E
	Installations	U13410E
RX850 Pro (Real-Time OS)	Fundamental	U13773E
	Installations	U13774E
RD850 (Ver. 3.0) (Task Debugger)		U13737E
RD850 Pro (Ver. 3.0) (Task Debugger)		U13916E
AZ850 (System Performance Analyzer)		U14410E

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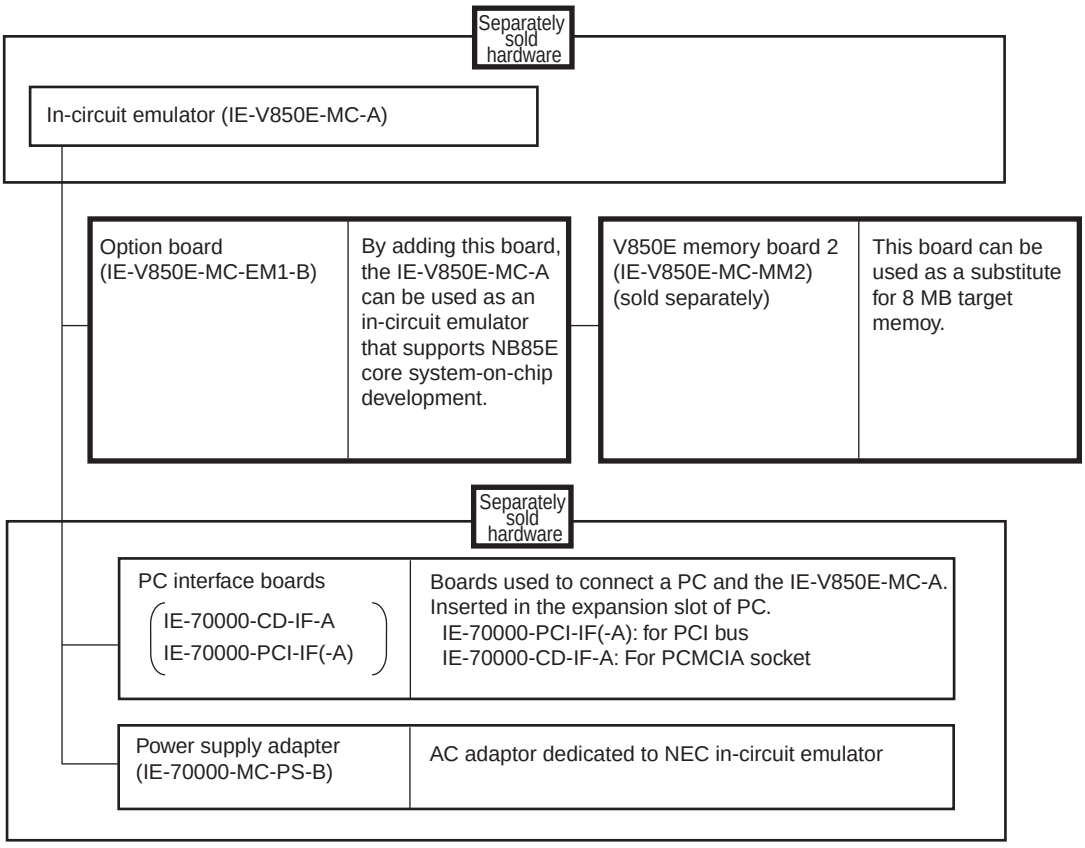
CHAPTER 1 OVERVIEW

The IE-V850E-MC-EM1-B is an option board for the IE-V850E-MC-A in-circuit emulator. Efficient hardware and software debugging can be performed during system development using the V850E1 by connecting the IE-V850E-MC-EM1-B to the IE-V850E-MC-A.

This manual describes the basic setup procedure, the switch settings for the IE-V850E-MC-EM1-B when it is connected to the IE-V850E-MC-A, and the IE-V850E-MC-MM2 (sold separately) settings. For the parts and functions of the IE-V850E-MC-A and details about the connection of component parts, refer to the **IE-V850E-MC-A User's Manual (U14487E)**.

1.1 Hardware Configuration



1.2 Features

○ System-on-chip emulation is possible by connecting the IE-V850E-MC-A, IE-V850E-MC-EM1-B, and UDL (User Design Logic) board.

○ Operating frequency: 40 MHz (MAX.)[Note]
A 20 MHz oscillator is mounted at shipment.

○ Extremely lightweight and compact

○ The following pins can be masked:
WAITZ, DCRESZ, HLDDRQZ, DCNMI0 to 2

Note The electrical specifications of the UDL interface must be considered during UDL/target board design. For the electrical specifications of the UDL interface, refer to **APPENDIX D ELECTRICAL SPECIFICATIONS OF UDL INTERFACE.**

1.3 Function Specifications (When Connected to IE-V850E-MC-A)

Item			Specifications
Emulation memory capacity	Internal ROM		1 MB
	External memory		4 MB (standard) + 8 MB (option)[Note]
Execution/pass detection coverage memory capacity	Internal ROM		1 MB
	External memory	In ROM-less mode	2 MB
		When using internal ROM	1 MB
Trace memory capacity			168 bits × 32 Kframes
Time measurement function			Measurement enabled with time tag and timer (3 channels)
External logic probe			8-bit external trace possible
			Trace/break event setting possible
Break function			Event break
			Step execution break
			Forced break
			Fail-safe break • Illegal access to peripheral I/O • Access to guard space • Write to ROM space

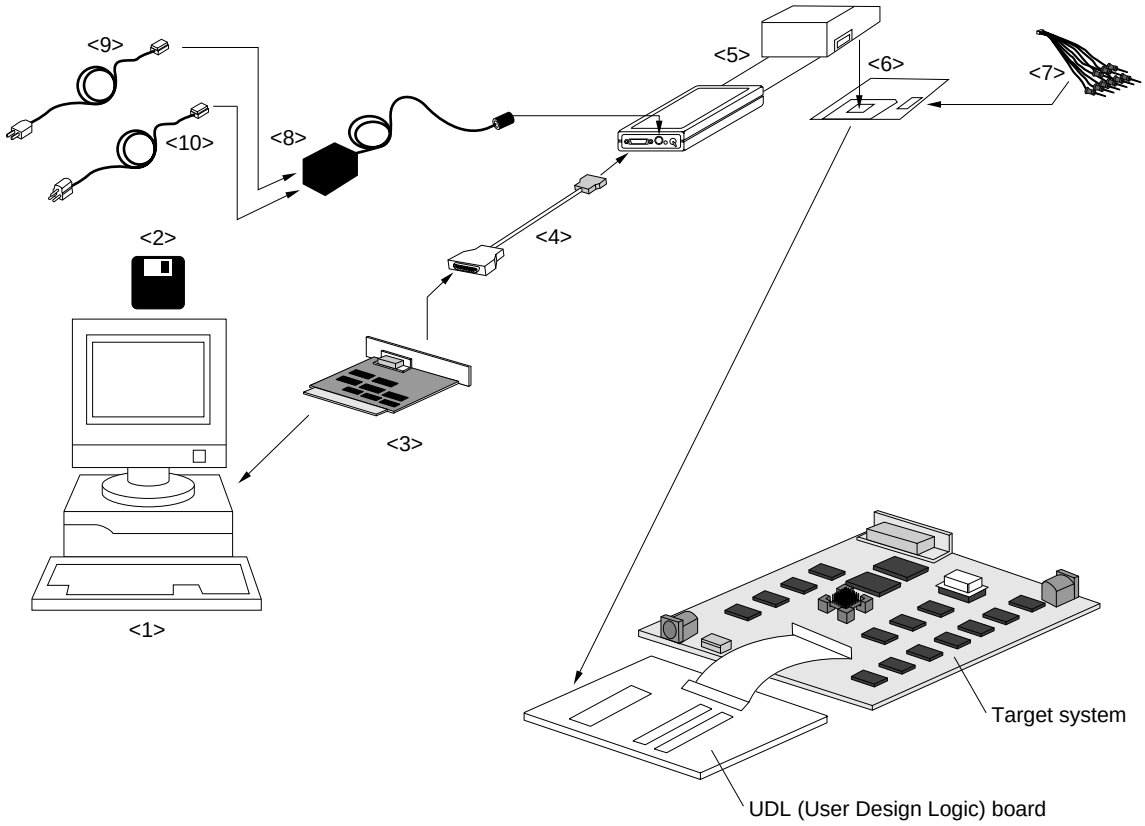
Note If the IE-V850E-MC-MM2 (sold separately) is mounted, an additional 8 MB can be substituted as target memory. However, the IE-V850E-MC-MM2 can be used only when a UDL board is connected.

Caution Some of the functions may not be supported, depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-V850E-MC-A to the IE-V850E-MC-EM1-B, which is then connected to a PC (PC-9800 series, PC/AT or compatibles) is illustrated below.

Figure 1-1. System Configuration



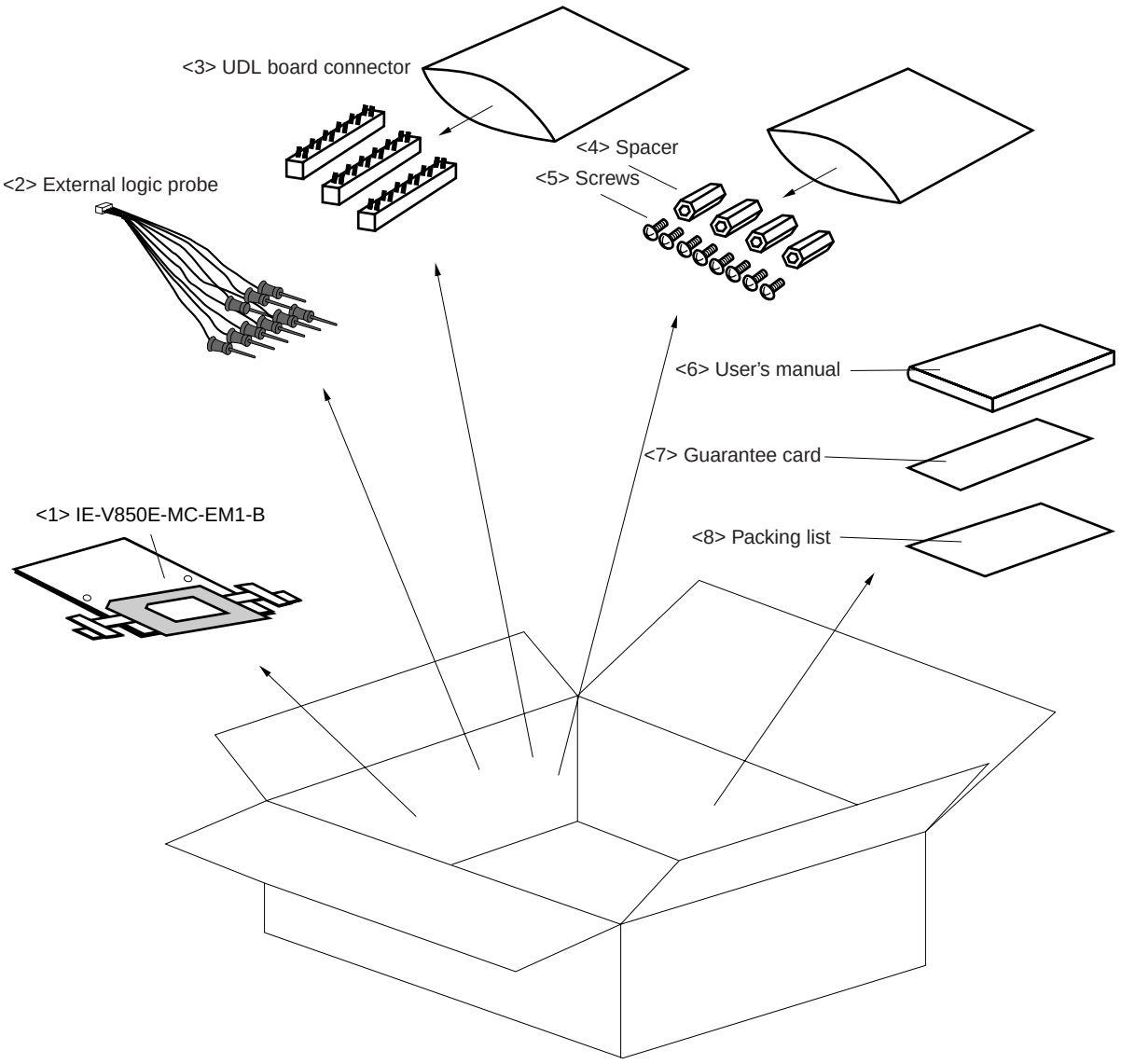
Remarks <1>: PC (PC-9800 series, PC/AT or compatibles)
<2>: Debugger (sold separately)
<3>: PC interface board
(IE-70000-PCI-IF(-A), IE-70000-CD-IF-A: Sold separately)
<4>: PC interface cable (provided with IE-V850E-MC-A)
<5>: In-circuit emulator (IE-V850E-MC-A: Sold separately)
<6>: In-circuit emulator option board (IE-850E-MC-EM1-B)
<7>: External logic probe (provided with IE-V850E-MC-EM1-B)
<8>: Power supply adapter (IE-70000-MC-PS-B: Sold separately)
<9>: AC100 V power cable (sold separately: Provided with IE-70000-MC-PS-B)
<10>: AC220 V power cable (sold separately: Provided with IE-70000-MC-PS-B)

1.5 Contents in Carton

The IE-V850E-MC-EM1-B carton contains the main unit, an external logic probe, UDL board connectors, spacers, screws, this manual, a guarantee card, and a packing list.

The spacers and screws are contained in the same envelope. If there are any missing or damaged items, contact an NEC sales representative or an NEC distributor.

Figure 1-2. Contents in Carton



<1> IE-V850E-MC-EM1-B:	1	<5> Screws:	8
<2> External logic probe:	1	<6> User's manual:	1
<3> UDL board connectors:	3	<7> Guarantee card:	1
(XH3A-0141-A (made by Omron))		<8> Packing list:	1
<4> Spacers:	4		

1.6 Connection of IE-V850E-MC-A and IE-V850E-MC-EM1-B

The procedure for connecting the IE-V850E-MC-A and IE-V850E-MC-EM1-B is described below.

Caution Be careful not to break or bend the connector pins when connecting.

<1> Remove the (upper and lower) pod covers of the IE-V850E-MC-A.
<2> Set the PGA socket lever of the IE-V850E-MC-EM1-B to the OPEN position shown in Figure 1-3 (b).
<3> Connect the PGA socket on the underside of the pod to the IE-V850E-MC-EM1-B. (Refer to **Figure 1-3 (c)**.) Keep the IE-V850E-MC-A and IE-V850E-MC-EM1-B in a horizontal position during connection.
<4> Set the PGA socket lever of the IE-V850E-MC-EM1-B to the CLOSE position shown in Figure 1-3 (b).
<5> Fix the rear of the pod cover (upper part) with the nylon rivets.

Figure 1-3. Connection of IE-V850E-MC-A and IE-V850E-MC-EM1-B (1/2)

(a) Connection outline

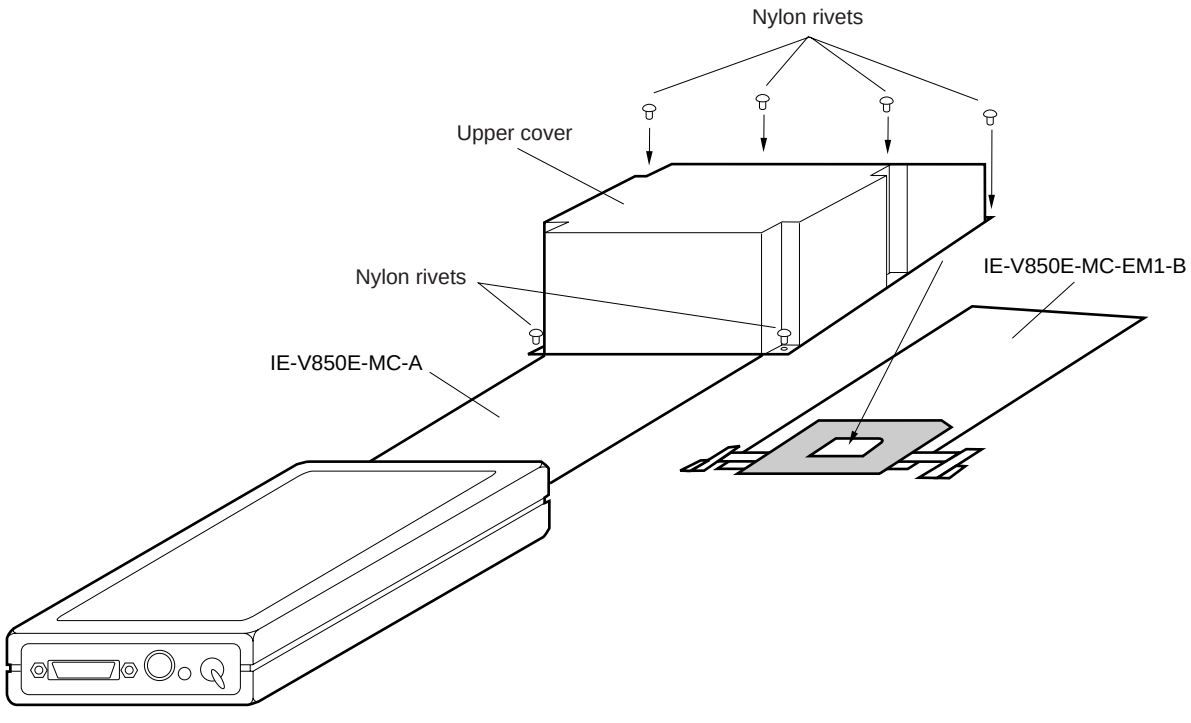
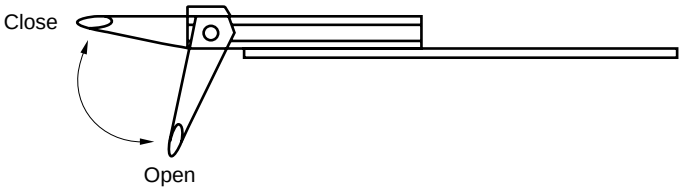
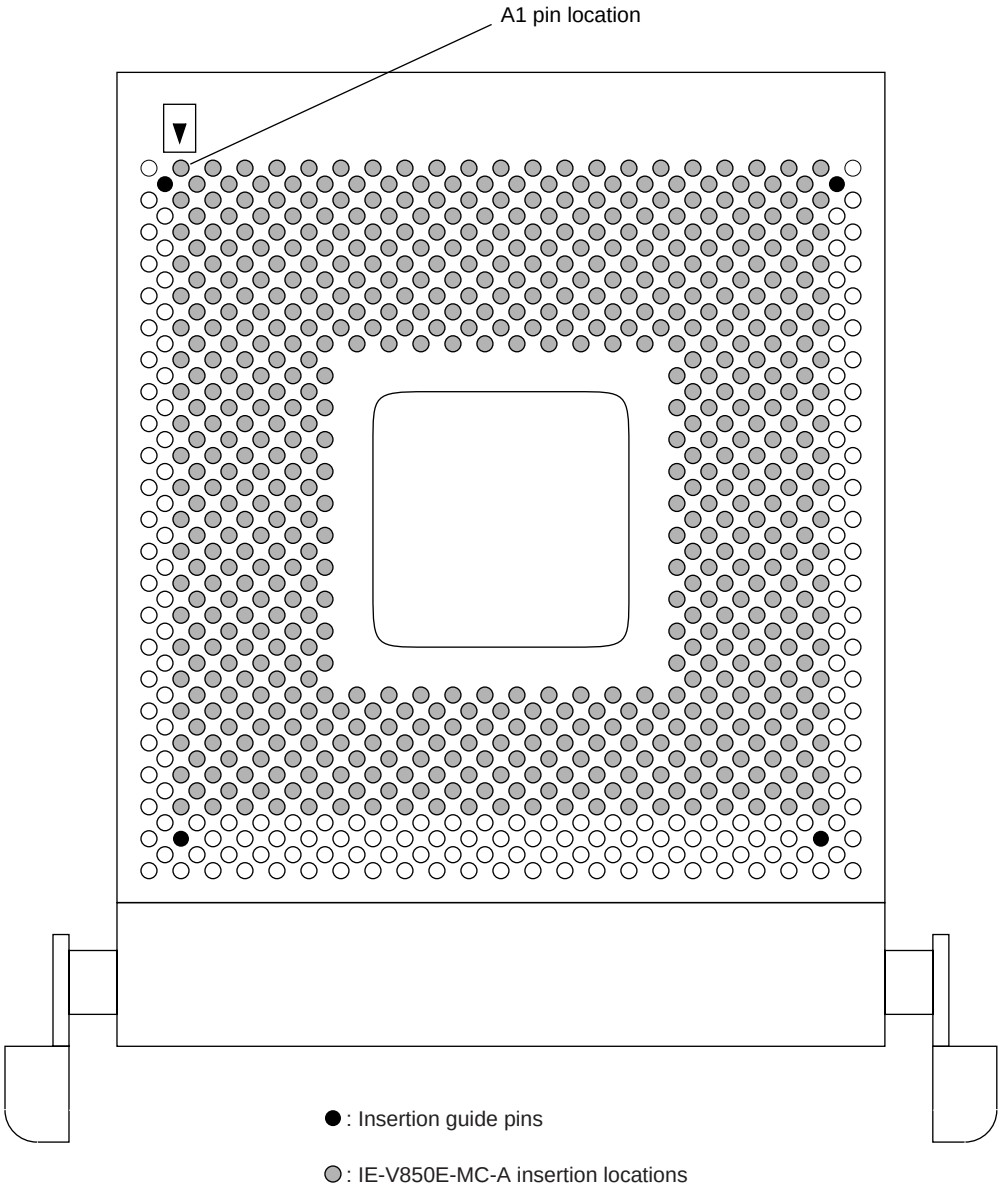


Figure 1-3. Connection of IE-V850E-MC-A and IE-V850E-MC-EM1-B (2/2)

(b) PGA socket lever of IE-V850E-MC-EM1-B



(c) Connection location (IE-V850E-MC-EM1-B)



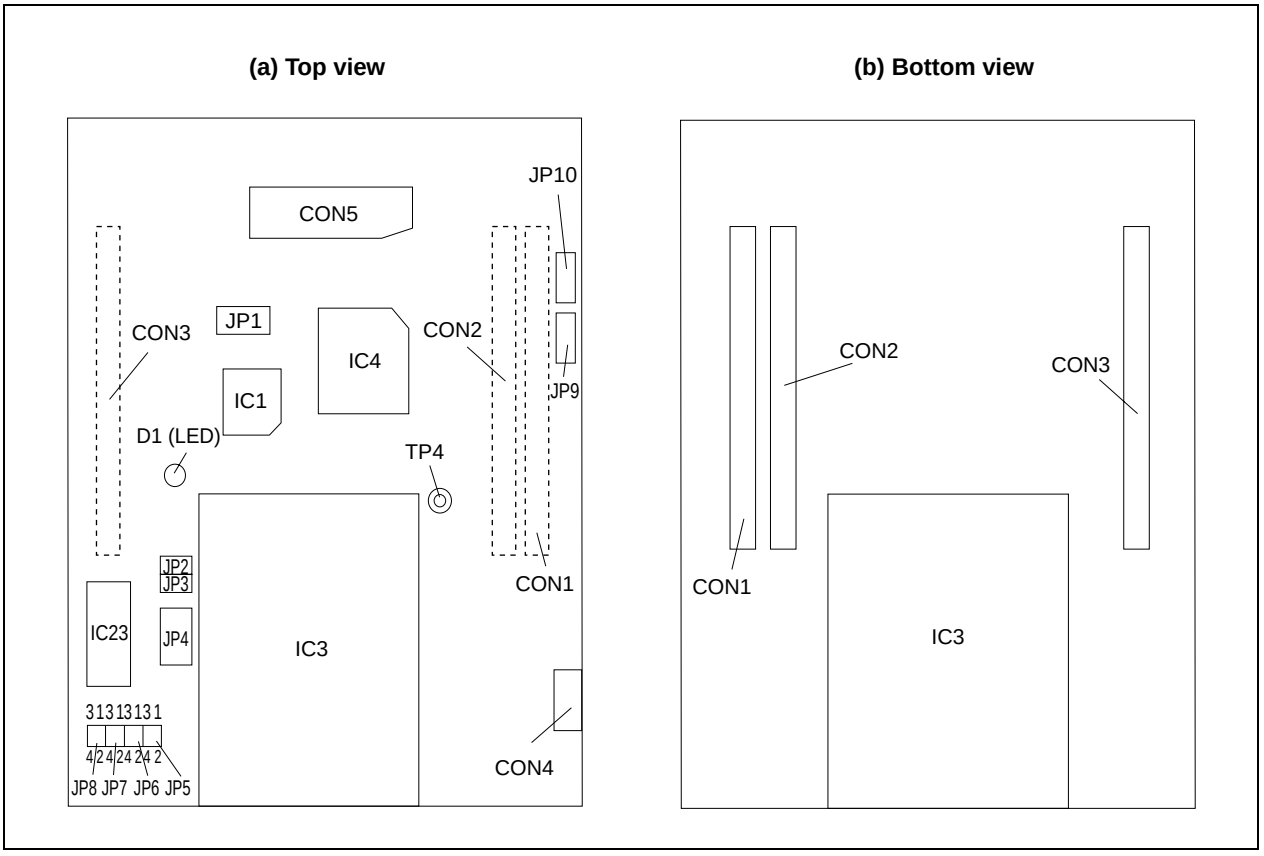
CHAPTER 2 PART NAMES AND FUNCTIONS

This chapter describes the name and functions of each part of the IE-V850E-MC-EM1-B, as well as the switch settings.

For more information about the pod, jumper, and switch positions, refer to the **IE-V850E-MC-A User's Manual (U14487E)**.

2.1 IE-V850E-MC-EM1-B Part Names and Functions

Figure 2-1. IE-V850E-MC-EM1-B



(1) JP1

This pin is used for testing before shipment. Do not change this setting.

(2) JP2

1-2 shorted: Enables use of the internal memory controller.

1-2 open: Enables use of the VSB bus.

(3) JP3

This pin is used for testing before shipment. Do not change this setting.

(4) JP4

This pin is used for testing before shipment. Do not change this setting.

(5) JP5

This pin is used for testing before shipment. Do not change this setting.

(6) JP6

This pin is used for testing before shipment. Do not change this setting.

(7) JP7

This pin is used for testing before shipment. Do not change this setting.

(8) JP8

This pin is used for testing before shipment. Do not change this setting.

(9) JP9

1-2 shorted: Interrupt edge detection.

1-2 open: Interrupt level detection.

(10) JP10

1-2 shorted: Enables STBC circuit operation.

1-2 open: Stops STBC circuit operation.

(11) TP4

This pin enables measurement of the CLKOUT output signal of the evaluation chip.

(12) D1

This LED is used for testing before shipment, and is therefore always off.

(13) CON1 to CON3

UDL board connectors

(14) CON4

This connector is used to connect the external sense probe to monitor signals on the UDL board, record them as trace data, and incorporate them in event sources.

Signals can be received at the 3.3 V CMOS level, but up to 5 V is tolerated.

The timing used to fetch signals is the program fetch timing.

Signals monitored with the external logic probe can also be fetched from the UDL interface connectors (CON3, CON093 to CON100).

(15) CON5

Connector used to mount the target substitution memory board (IE-V850E-MC-MM2)

(16) IC3

Socket used to connect the IE-V850E-MC-A

(17) IC23

Socket used to mount an oscillator

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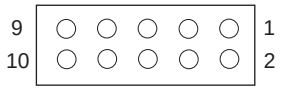
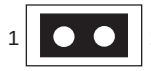
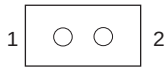
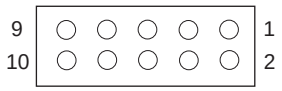
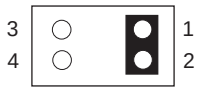
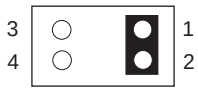
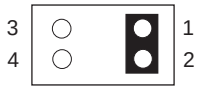
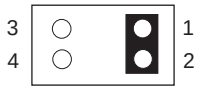
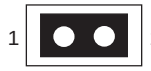
CHAPTER 3 LIST OF SETTINGS AT SHIPMENT

Item	Setting	Remark
JP1		Setting other than shipment default setting prohibited
JP2		Internal memory controller used
JP3		Setting other than shipment default setting prohibited
JP4		Setting other than shipment default setting prohibited
JP5		Setting other than shipment default setting prohibited
JP6		Setting other than shipment default setting prohibited
JP7		Setting other than shipment default setting prohibited
JP8		Setting other than shipment default setting prohibited
JP9		Interrupt edge detection
JP10		STBC circuit operation enabled

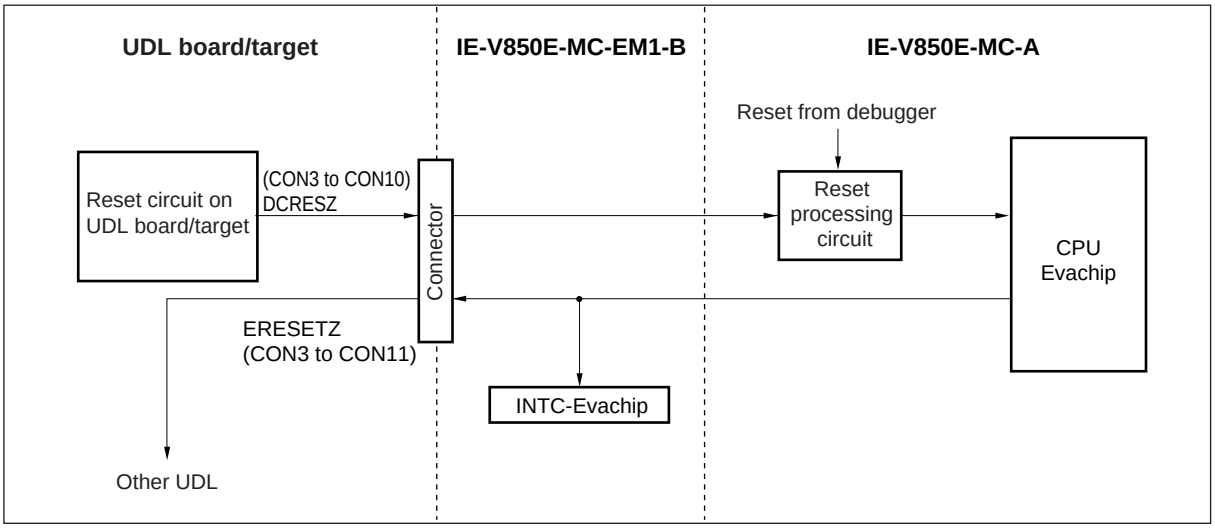
[MEMO]

CHAPTER 4 CAUTIONS

4.1 Reset Signal

Be sure to use the emulator output signal ERESETZ as the reset signal for circuits on the UDL board.
If the ERESETZ signal is not used, software reset from the debugger is not enabled for the UDL board.

Figure 4-1. Reset Signal



4.2 Clock

4.2.1 Clock supply method

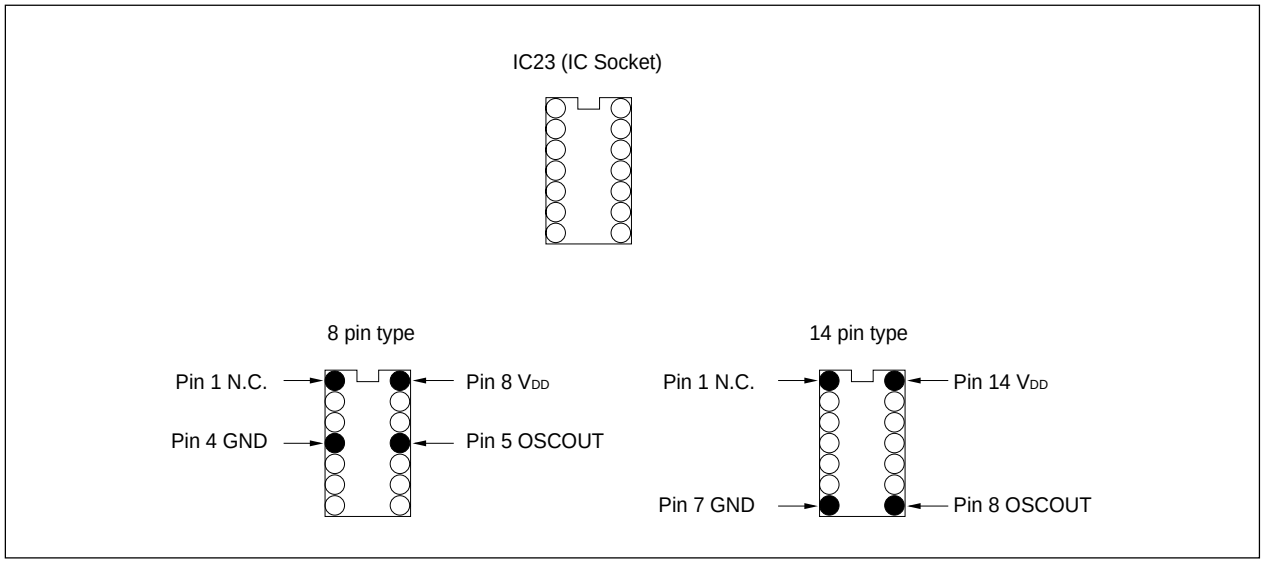
The clock used by the emulator can be supplied using one of two methods, selectable by the debugger.

(1) Supply VBCLK to emulator from UDL board
Be sure to use the oscillator output clock for VBCLK.

(2) Supply clock from oscillator mounted on emulator
A 20 MHz oscillator (8-pin type) is mounted on the emulator at shipment.
The output clock of this oscillator can be used as the main clock.
The emulator can be operated at the desired frequency by removing the already mounted 20 MHz oscillator and installing an oscillator of the desired frequency (40 MHz MAX.).

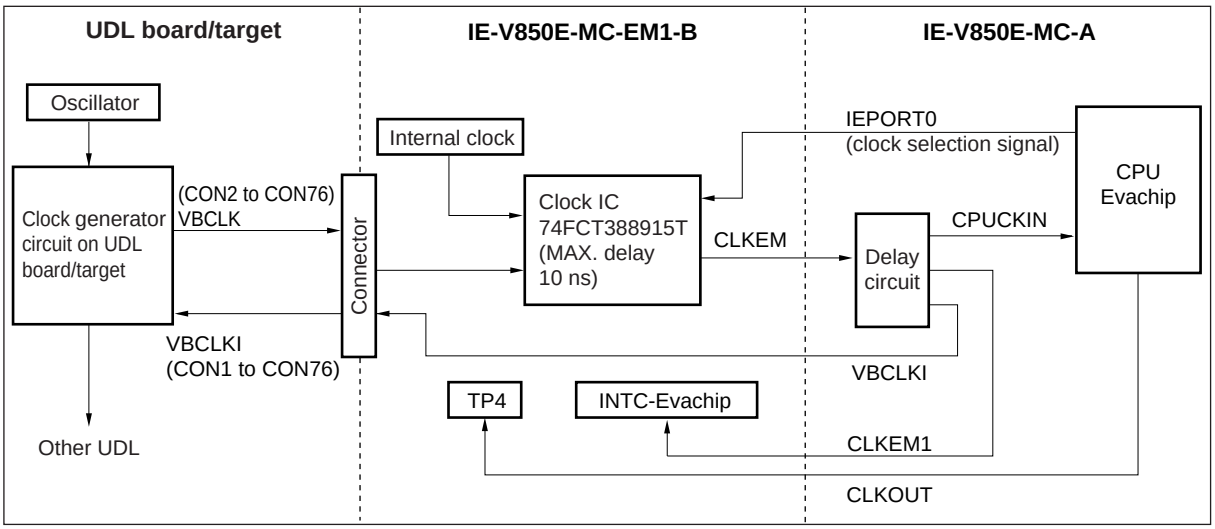
Caution If supplying the emulator clock from the UDL board, do not stop the clock supply even when going into the standby mode. If the clock supply stops, the emulator and debugger become deadlocked.

Figure 4-2. Oscillator IC Socket



Remark The emulator uses either one of the above clocks as the main clock and outputs it to the UDL board as VBCLKI.
Use VBCLKI for the clock distributed on the UDL board.

Figure 4-3. IE-V850E-MC-A and IE-V850-MC-EM1-B Clock Circuit Diagram



4.2.2 Main clock tuning

As the effect of an excessive load and two or more buffering stages on the UDL board, a timing delay may occur for the CPUCKIN and CLKEM1 signals in relation to VBCLKI. In such a case, the timing of the CPUCKIN and CLKEM1 signals can be delayed by setting JP2 of the IE-V850E-MC-A so as to tune the phase with VBCLKI. There are three types of tuning.

(a) 1-2 shorted and 7-8 shorted: Shipment default setting
(b) 3-4 shorted and 9-10 shorted: 6 ns (TYP.) phase delay in relation to shipment default setting
(c) 5-6 shorted and 11-12 shorted: 12 ns (TYP.) phase delay in relation to shipment default setting

When tuning the main clock, monitor the clock at the following two points and adjust the phase difference.

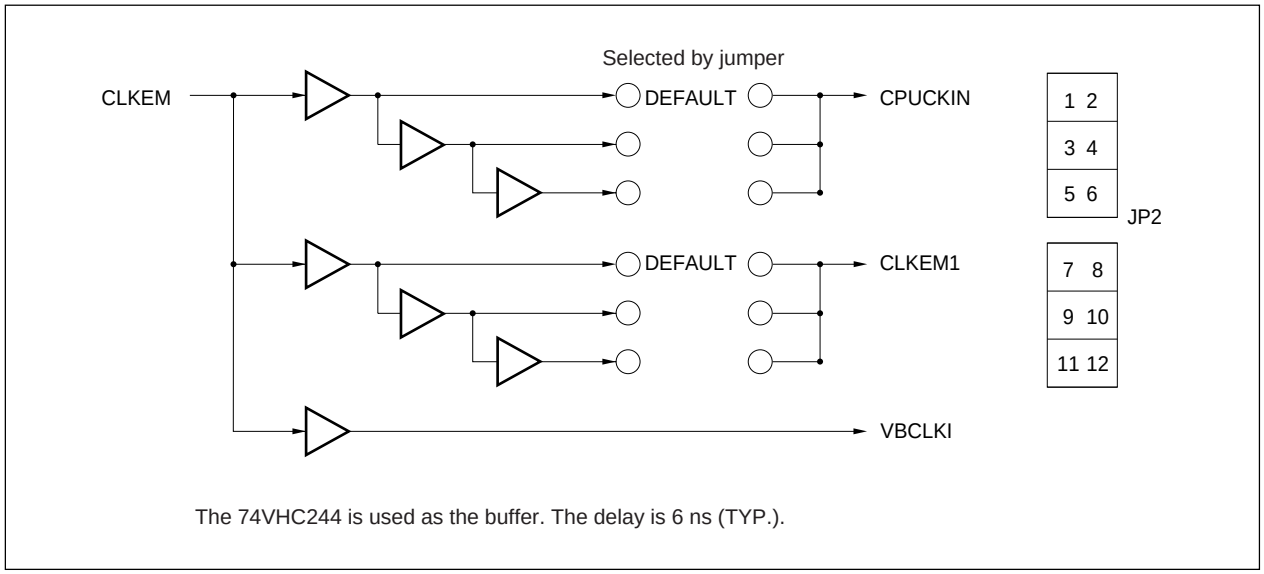
- Point serving as reference on UDL board
- TP4 on IE-V850E-MC-EM1-B (not output during reset)

Cautions 1. When manipulating JP2 of the IE-V850E-MC-A, ensure that the same number of buffering stages is inserted for CPUCKIN and CLKEM1.

2. The evaluation chip operation clock (CLKOUT) is approximately 10 ns later than VBCLKI. Therefore, when distributing VBCLKI on the UDL board, it is recommended to do so after the first buffer stage.

Moreover, as long as there is no excessive load and no more than one buffer stage, use the shipment default setting of JP2 of the IE-850E-MC-A.

Figure 4-4. Delay Circuit Diagram (IE-V850E-MC-A)



The 74VHC244 is used as the buffer. The delay is 6 ns (TYP.).

4.3 Emulation Memory

A standard emulation memory that can always be used as well as a target substitution memory that can be used by mounting the IE-V850E-MC-MM2 (sold separately) are available for the IE-V850E-MC-EM1-B.

The emulation memory can only be used only when the memory controller is selected; it cannot be used when the VSB bus is selected.

4.3.1 Standard emulation memory function

Memory capacity: 4 MB
Mapping unit: 1 MB (mapping of 1 MB × 4 banks MAX. is possible.)
Bus size: 16 bits or 32 bits (8-bit bus size is not supported.)
Mapping method: Specify the area to be mapped with the debugger as “Emulation RAM/ROM”. (There is no jumper setting.)
Wait insertion: If the operating frequency is 25 MHz or higher, insertion of 1 wait or more is required.
The number of waits for the emulation memory is not influenced by the _WAIT signal; it is determined by debugger setting or wait control register setting. (0 WAIT/1 WAIT/PROGRAMMABLE WAIT (1 to 7 WAITS).)

- For ID850
  The following three selections are available on the configuration screen.
  (a) WAIT MASK → Access is performed with 0 waits.
  (b) 1 WAIT (DEFAULT) → Access is performed with 1 wait.
  (c) TARGET WAIT → Access is performed with the number of waits set with the DWC0/1 register. However, the number of waits is always 1 wait if 0/1 WAIT is set.

- For MULTI
  The following three selections are available using the PINMASK command.
  (a) WAIT mask → Access is performed with 0 waits.
  EMWAIT mask (Wait signals to the external memory are masked)
  (b) WAIT mask → Access is performed with 1 wait.
  EMWAIT unmask (Wait signals to the external memory are masked)
  WAIT unmask → Access is performed with 1 wait.
  EMWAIT mask (Wait signals to the external memory are enabled)
  (c) WAIT unmask → Access is performed with the number of waits set by the DWC0/1 register.
  EMWAIT unmask However, the number of waits is always 1 wait if 0/1 WAIT is set.
  (Wait signals to the external memory are enabled)

4.3.2 Target substitution memory function

Memory capacity:	8 MB
Mapping specifications:	Emulation can be performed by selecting the mapping area using one of the chip select signals of the memory controller. The start address mapped in the memory block is determined by JP3 of the IE-V850E-MC-MM2.
Bus size:	16 bits or 32 bits (8-bit bus size is not supported.)
Mapping method:	Set JP2 and JP3[Note] of the IE-V850E-MC-MM2. Specify the area to be mapped with the debugger as “TARGET MEMORY”.

Note For how to set JP2 and JP3, refer to Chapter 5 IE-V850E-MC-MM2.

Cautions 1. If the target substitution memory is mapped to an area overlapping the standard emulation memory, the standard emulation memory has priority.

2. To access the target memory when the IE-V850E-MC-MM2 (sold separately) is mounted, make sure that the memory blocks to which the target memory is allocated and the memory blocks specified by setting JP2 and JP3 of the IE-V850E-MC-MM2 do not match.

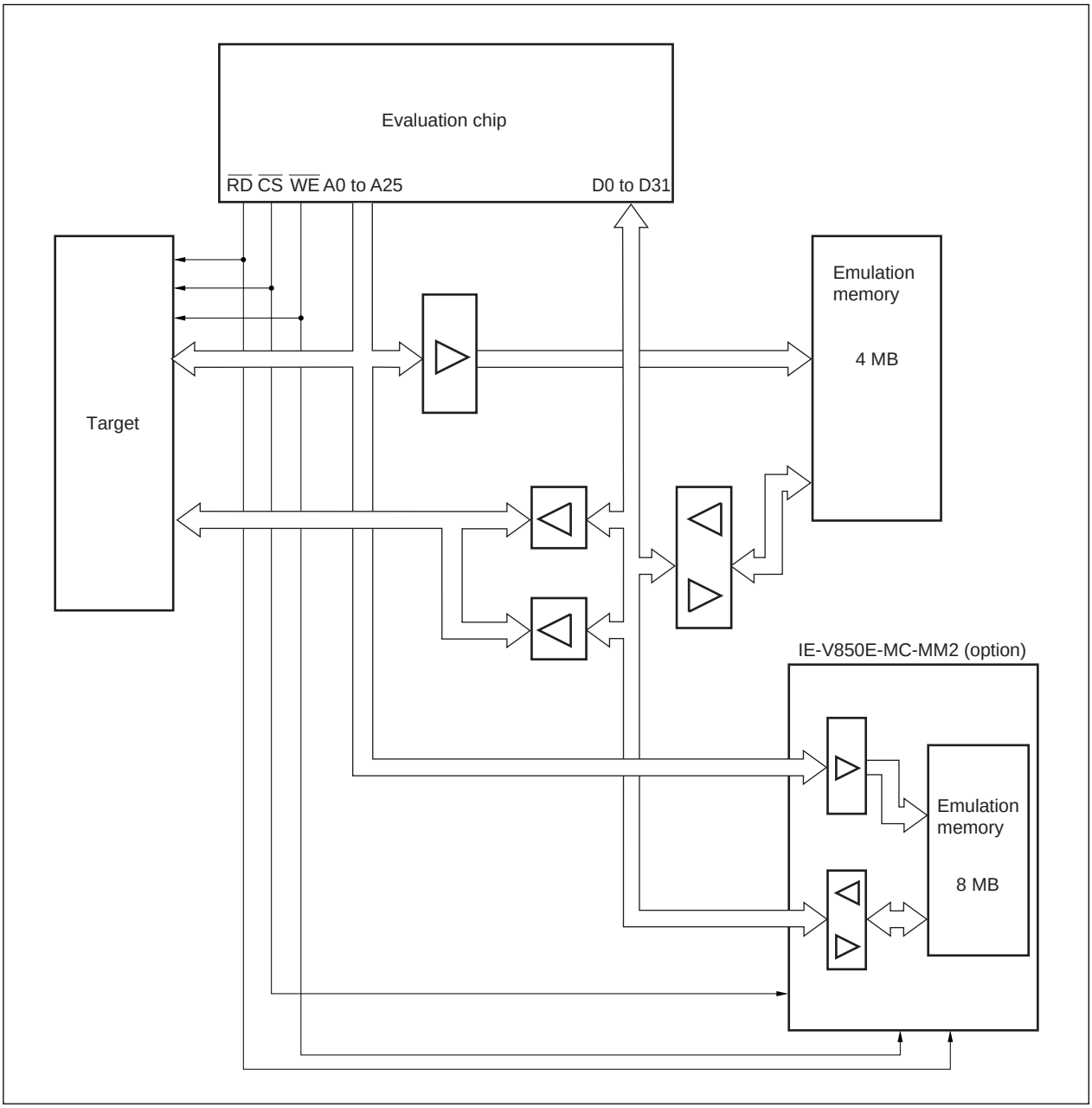
3. The target substitution memory can used only when the UDL board is connected.

4.3.3 Emulation memory operation timing differences

When the DRAM, SDRAM, and page ROM areas in the target system are allocated to the emulation memory, the access timing used is that of the SRAM.

When measuring the performance using emulation memory, perform wait settings so as to match the access timing of the memory actually used.

Figure 4-5. Emulation Memory Equivalent Circuit



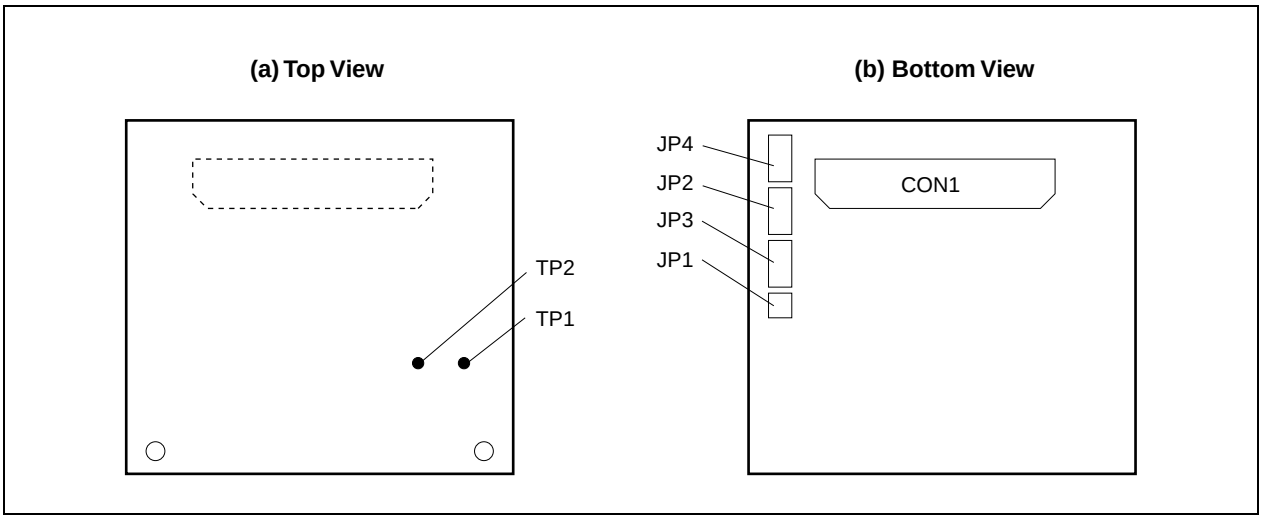
[MEMO]

CHAPTER 5 IE-V850E-MC-MM2

This chapter describes the parts and functions of the IE-V850E-MC-MM2 (sold separately) as well as the jumper settings.

5.1 IE-V850E-MC-MM2 Parts and Functions

Figure 5-1. IE-V850E-MC-MM2



(1) JP1

Jumper for bus size selection

1-2 shorted: 32 bits 1-2 open: 16 bits

(2) JP2

Jumper for target substitution memory mapping setting

The setting method is as follows.

Table 5-1. JP2 Setting Method

JP2 Setting	Target Substitution Memory Mapping Area
1-2 shorted	Memory block 0 (select CSZ0)
3-4 shorted	Memory block 1 (select CSZ1)
5-6 shorted	Memory block 2 (select CSZ2)
7-8 shorted	Memory block 3 (select CSZ3)
9-10 shorted	Memory block 4 (select CSZ4)
11-12 shorted	Memory block 5 (select CSZ5)
13-14 shorted	Memory block 6 (select CSZ6)
15-16 shorted	Memory block 7 (select CSZ7)
All pins open	Target substitution memory cannot be mapped.

(3) JP3

This jumper is used to specify bits 23 to 25 of the memory block addresses to be mapped to the target substitution memory.

Table 5-2. Bits 23 to 25 Setting Method Using JP3

JP3 Setting			Value of A25 to A23		
1-2	3-4	5-6	A25	A24	A23
Open	Open	Open	H	H	H
Open	Open	Shorted	H	H	L
Open	Shorted	Open	H	L	H
Open	Shorted	Shorted	H	L	L
Shorted	Open	Open	L	H	H
Shorted	Open	Shorted	L	H	L
Shorted	Shorted	Open	L	L	H
Shorted	Shorted	Shorted	L	L	L

(4) JP4

Pin block for testing before shipment. Use the shipment default settings.

(5) TP1

Ground pin

(6) TP2

Pin used for testing before shipment

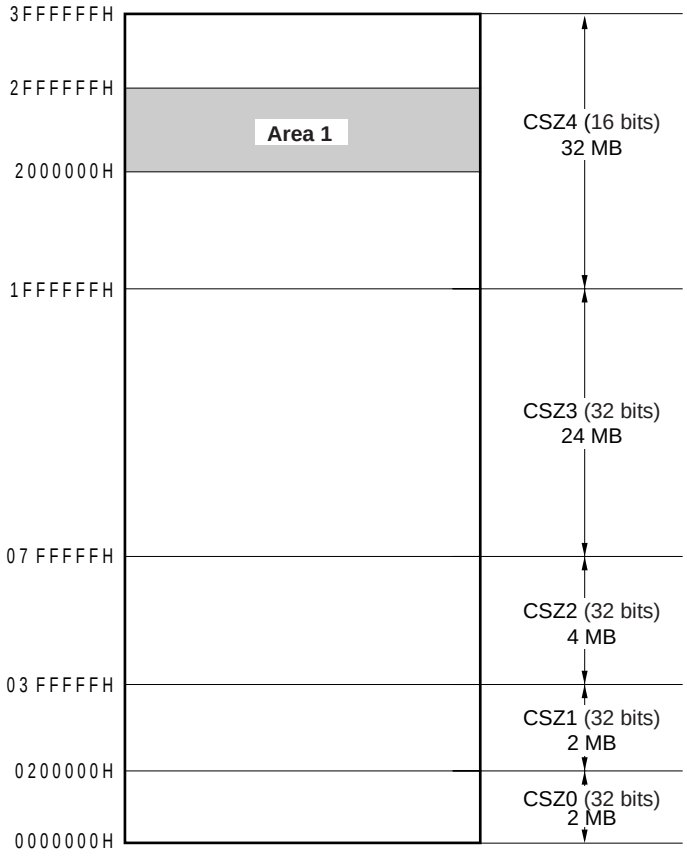
(7) CON1

Connector for interface with IE-V850E-MC-EM1-B

5.2 JP1 to JP3 Setting Examples

Setting examples of JP1 to JP3 in the 64 MB mode are described below.

Example 1



Area 1. The jumper settings when substituting this area are as follows.

JP1: Open

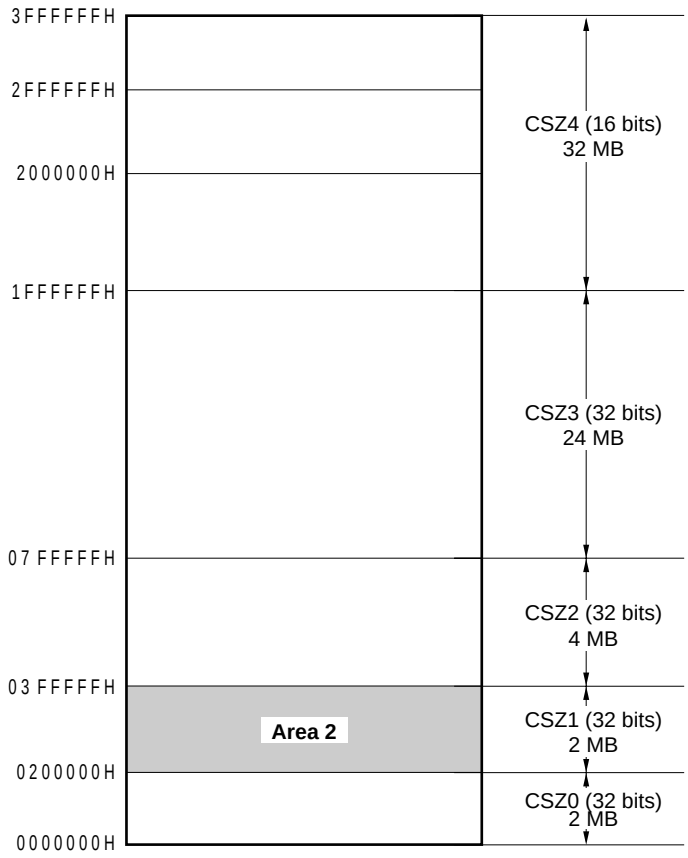
JP2: 9-10 open

JP3: 1-2 open

3-4 shorted

5-6 open

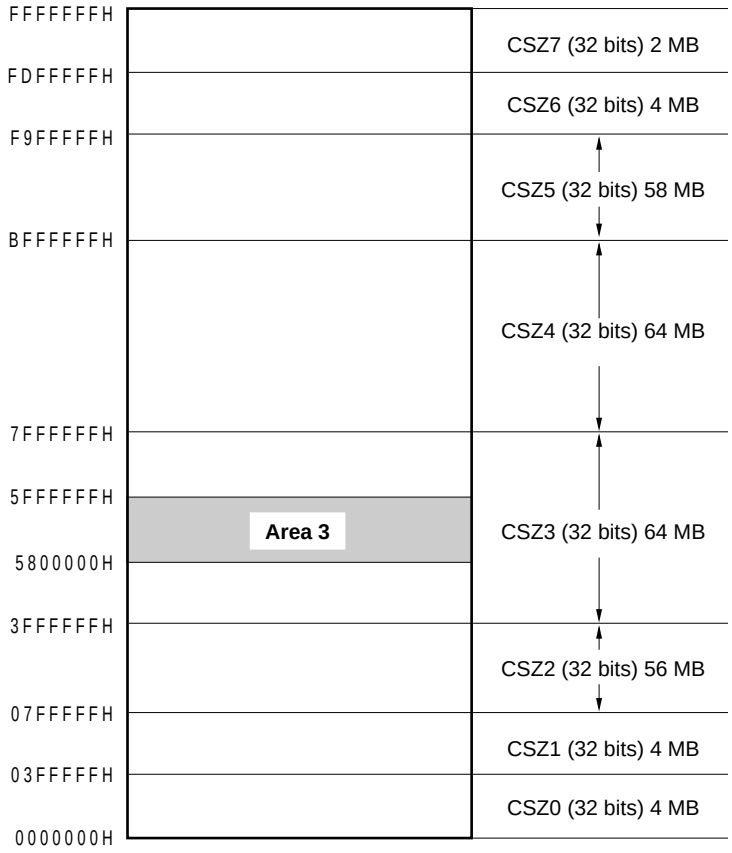
Example 2.



Area 2. The jumper settings when substituting this area are as follows.

JP1: Shorted
JP2: 3-4 shorted
JP3: 1-2 shorted
3-4 shorted
5-6 shorted

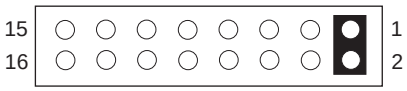
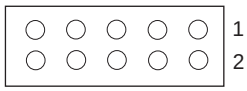
A JP1 to JP3 setting example when the 256 MB mode is used is described below.



Area 3. The jumper settings when substituting this area are as follows.

JP1: Shorted
JP2: 7-8 shorted
JP3: 1-2 shorted
3-4 shorted
5-6 shorted

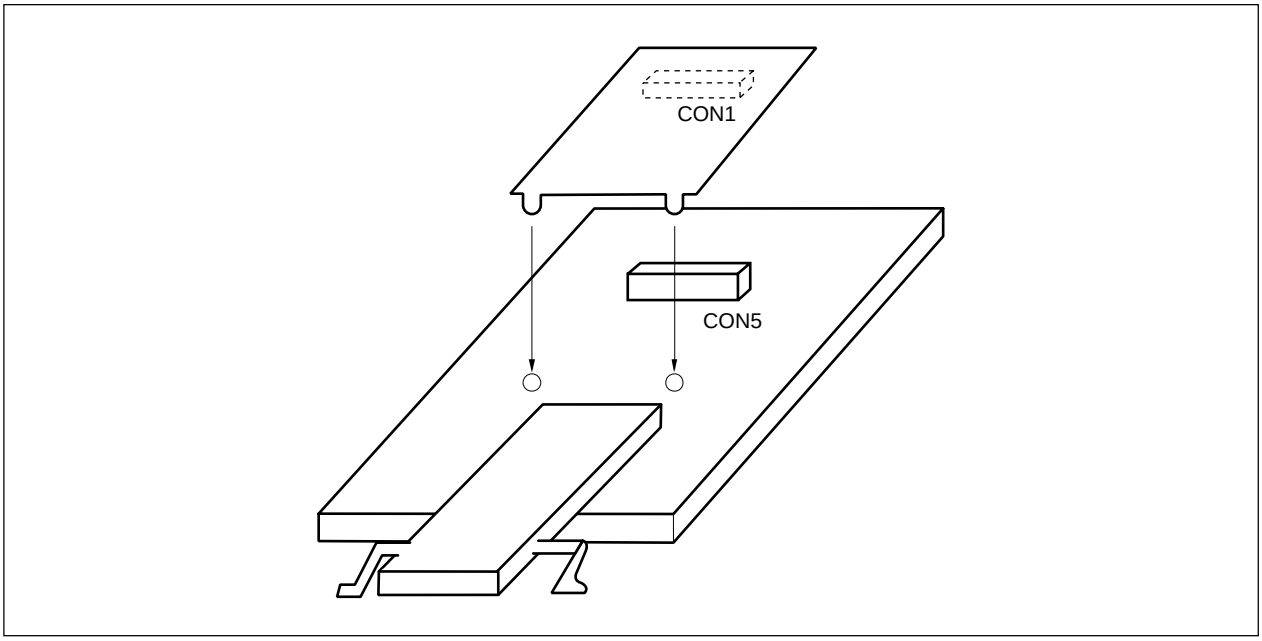
5.3 List of Settings at Product Shipment

Item	Setting	Remark
JP1		Sets bus size to 32 bits.
JP2		Maps memory block 0 to expanded emulation memory.
JP3		A25 = 1, A24 = A23 = 0
JP4		Use of settings other than the shipment default setting is prohibited.

5.4 Connection of IE-V850E-MC-EM1-B and IE-V850E-MC-MM2

<1> Set JP1, JP2, and JP3 of the IE-V850E-MC-MM2 as desired.
<2> Connect the screws and spacers to the IE-V850E-MC-MM2.
<3> Connect CON1 of the IE-V850E-MC-MM2 and CON5 of the IE-V850E-MC-EM1-B.
<4> Secure the IE-V850E-MC-MM2 with the screws from the back of the IE-V850E-MC-EM1-B.

Figure 5-2. IE-V850E-MC-EM1-B and IE-V850E-MC-MM2 Connection Diagram

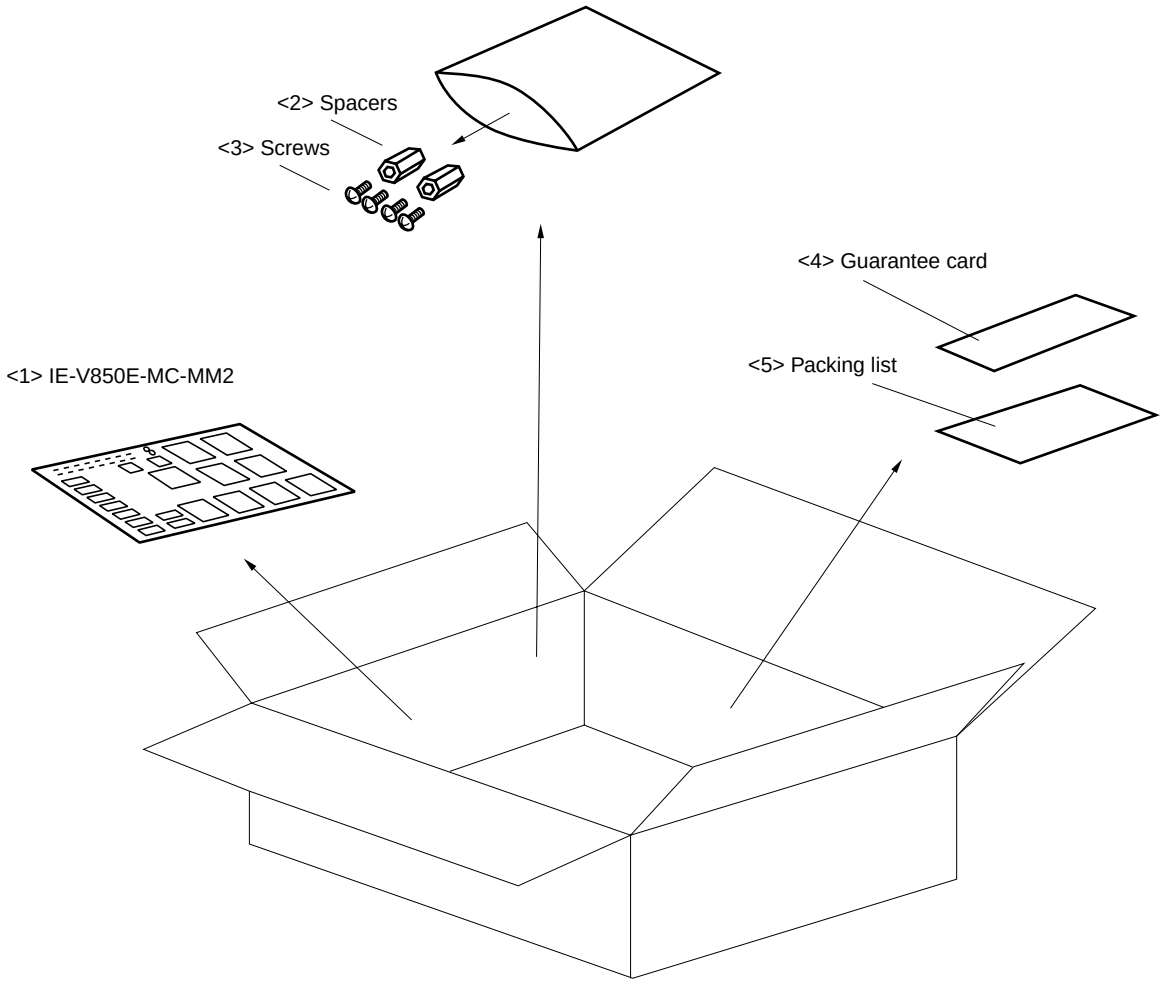


5.5 Contents in Carton

The IE-V850E-MC-MM2 box contains the IE-V850E-MC-MM2 in-circuit emulator board, spacers, screws, a guarantee card, and a packing list.

The spacers and screws are contained in the same envelope. If there are any missing or damaged items, contact an NEC sales representative or an NEC distributor.

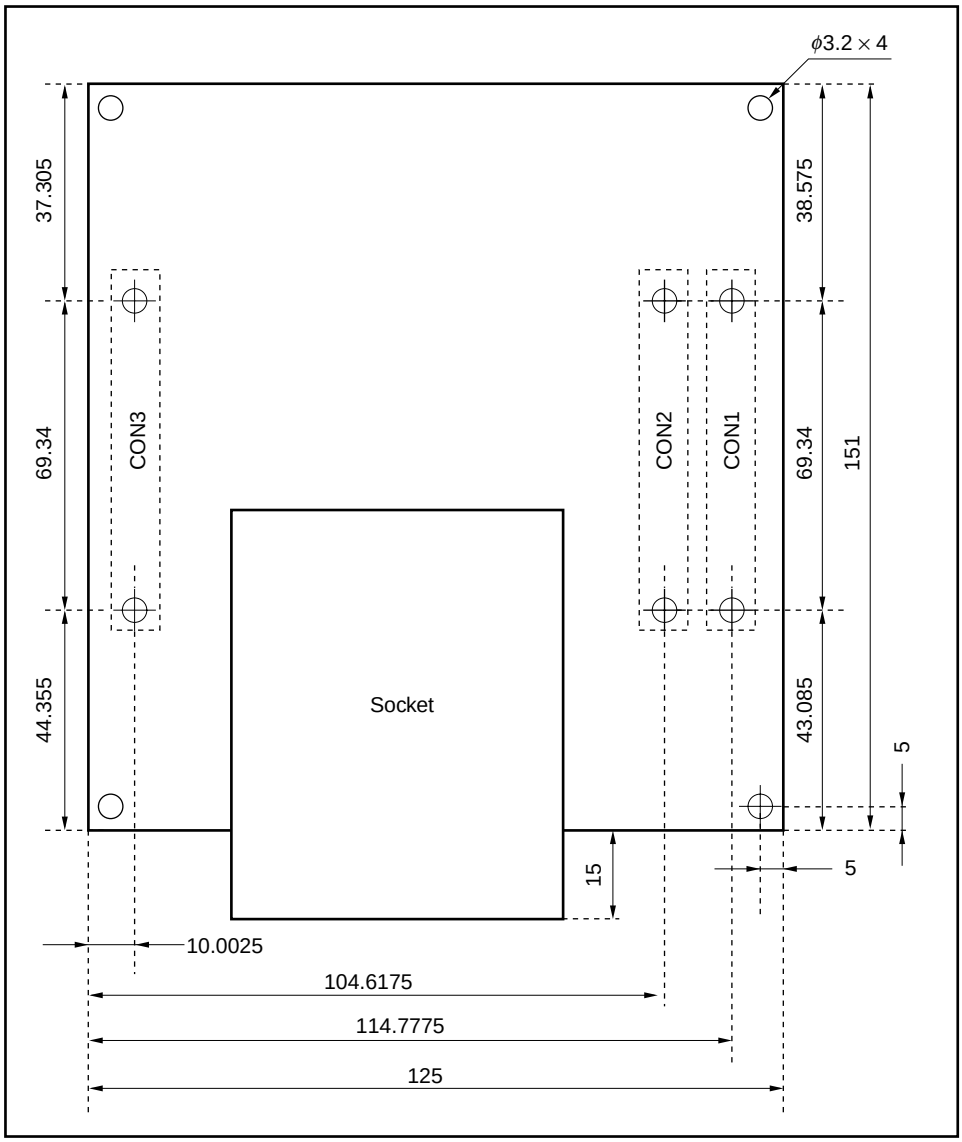
Figure 5-3. Contents in Carton



<1> IE-V850E-MC-MM2: 1
<2> Spacers: 2
<3> Screws: 4
<4> Guarantee card: 1
<5> Packing list: 1

APPENDIX A PRODUCT DRAWING

The drawing of the IE-V850E-MC-EM1-B is shown below. (Unit: mm)



(The IE-V850E-MC-A is on this side.)

Remark The UDL board is connected by CON1 to CON3, but the stacking height is 12 mm.
Do not place parts with a height of 8 mm or more on the part where the UDL board and IE-V850E-MC-EM1-B overlap.

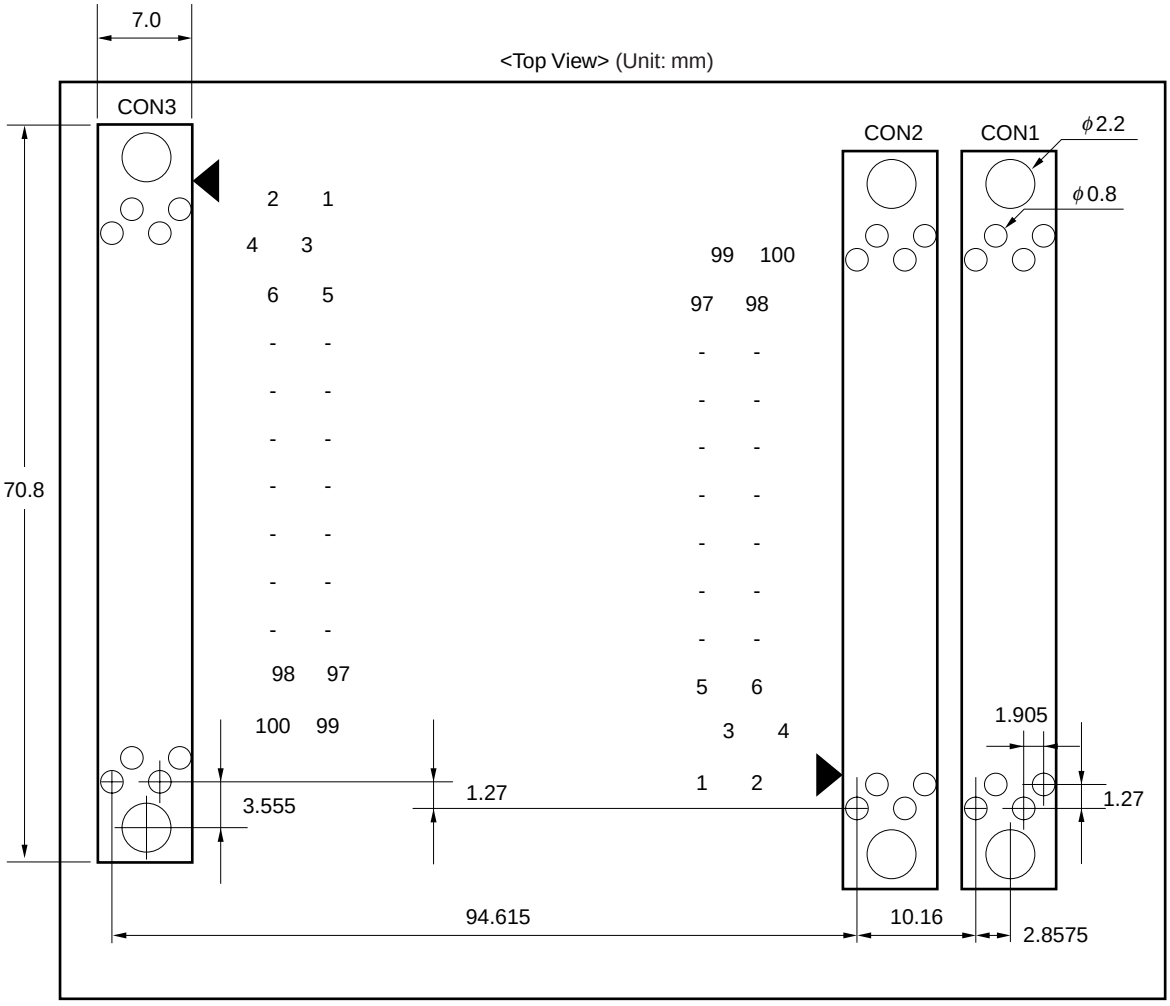
[MEMO]

APPENDIX B UDL BOARD INTERFACE CONNECTOR LOCATIONS

The following figure shows the top view of the UDL board.

The following part is used for the connector.

- XH3A-0141-A (made by Omron)



(The emulator is on this side.)

Caution When an option board is connected, the spacing with the UDL board becomes 12 mm. Therefore, do not place parts with a height of 8 mm or more on the connection part.

[MEMO]

APPENDIX C UDL INTERFACE CONNECTOR SIGNAL TABLE (VIEWED FROM IE-V850E-MC-EM1-B)

C.1 CON1 to CON3 Pin Assignment

The UDL interface connector signal table is shown from the next page.

C.1.1 Cautions

(1) The I/O attributes are as follows.

I/O: Bidirectional
I: Input signal to emulator.
O: Output signal from emulator.

(2) Signals assigned to connector

The signals assigned to the connector can be of two groups, as shown below.

(a) When VSB bus is selected

Pins for VSB, pins for NPB, pins for system control, pins for DMAC, pins for INTC

(b) When memory controller is selected

Pins for NB85E500, pins for NU85E502, pins for NPB, pins for system control, pins for DMAC, pins for INTC

(3) Handling of unused pins

No special handling of unused pins is required on the UDL board side, but to achieve greater pin status stability, perform the following processing on the UDL board.

- Input pin to UDL board: Leave open
- Output pin from UDL board: Fix to inactive
- I/O pin to UDL board: Leave open

(4) Since the emulator and UDL board interfaces are all performed using 3.3 V, to perform an interface at a voltage other than 3.3 V, convert the signal level on the UDL board side.

Since the emulator input pins support 5 V, inputting 5 V signals does not represent a problem.

C.2 Signal List

Signal List (1/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON1-CON001	3 V_{CC} Note 1				
CON1-CON002	3 V_{CC} Note 1				
CON1-CON003	DMACTV2			O	
CON1-CON004	DMACTV0			O	
CON1-CON005	V_{CC} Note 2				
CON1-CON006	V_{CC} Note 2				
CON1-CON007	VBD30	D30		I/O	5.1 K pull-up
CON1-CON008	VBD28	D28		I/O	5.1 K pull-up
CON1-CON009	VBD26	D26		I/O	5.1 K pull-up
CON1-CON010	VBD24	D24		I/O	5.1 K pull-up
CON1-CON011	VBD22	D22		I/O	5.1 K pull-up
CON1-CON012	VBD20	D20		I/O	5.1 K pull-up
CON1-CON013	VBD18	D18		I/O	5.1 K pull-up
CON1-CON014	VBD16	D16		I/O	5.1 K pull-up
CON1-CON015	GND				
CON1-CON016	GND				
CON1-CON017	VBD14	D14		I/O	5.1 K pull-up
CON1-CON018	VBD12	D12		I/O	5.1 K pull-up
CON1-CON019	VBD10	D10		I/O	5.1 K pull-up
CON1-CON020	VBD8	D8		I/O	5.1 K pull-up
CON1-CON021	VBD6	D6		I/O	5.1 K pull-up
CON1-CON022	VBD4	D4		I/O	5.1 K pull-up
CON1-CON023	VBD2	D2		I/O	5.1 K pull-up
CON1-CON024	VBD0	D0		I/O	5.1 K pull-up
CON1-CON025	GND				
CON1-CON026	GND				
CON1-CON027	GND				
CON1-CON028	GND				
CON1-CON029	VBBSTR	– Note 3	– Note 3	O	
CON1-CON030	VBDC	RDZ		O	
CON1-CON031	VBBENZ2	WRZ2	DQM2	O	
CON1-CON032	VBBENZ0	WRZ0	DQM0	O	
CON1-CON033	GND				
CON1-CON034	GND				
CON1-CON035	PCM4	– Note 3	REFRQZ	O	33 K pull-down
CON1-CON036	PCM2	HLDAKZ		O	33 K pull-down
CON1-CON037	PCM0	WAITZ		I	5.1 K pull-up

Notes 1. 3.3 V power supply of emulator

2. 5 V power supply of emulator

3. Leave open or perform pin processing according to **(3) Handling of unused pins in C.1.1 Cautions**

Signal List (2/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON1-CON038	GND				
CON1-CON039	GND				
CON1-CON040	VBA26	–Note 1		O	
CON1-CON041	VBA24	A24		O	
CON1-CON042	VBA22	A22		O	
CON1-CON043	VBA20	A20		O	
CON1-CON044	VBA18	A18		O	
CON1-CON045	VBA16	A16		O	
CON1-CON046	VBA14	A14		O	
CON1-CON047	GND				
CON1-CON048	GND				
CON1-CON049	VBA12	A12		O	
CON1-CON050	VBA10	A10		O	
CON1-CON051	VBA8	A8		O	
CON1-CON052	VBA6	A6		O	
CON1-CON053	VBA4	A4		O	
CON1-CON054	VBA2	A2		O	
CON1-CON055	VBA0	A0		O	
CON1-CON056	GND				
CON1-CON057	GND				
CON1-CON058	GND				
CON1-CON059	GND				
CON1-CON060	VDCSZ6	CSZ6	CSZ6	O	
CON1-CON061	VDCSZ4	CSZ4	CSZ4	O	
CON1-CON062	VDCSZ2	CSZ2/IOWRZ	CSZ2/IOWRZ	O	
CON1-CON063	VDCSZ0	CSZ0	CSZ0	O	
CON1-CON064	PCD2	–Note 1	SDCASZ	O	33 K pull-down
CON1-CON065	PCD0	–Note 1	CKE	O	33 K pull-down
CON1-CON066	VBCTYP2	–Note 1		O	
CON1-CON067	VBCTYP0	–Note 1		O	
CON1-CON068	VAACK	–Note 1		O	
CON1-CON069	VBAHLD	–Note 1		I	33 K pull-down
CON1-CON070	VBLOCK	–Note 1		O	
CON1-CON071	VBSIZE1	–Note 1		O	
CON1-CON072	VBTTYP1	–Note 1		O	
CON1-CON073	VBWRITE	–Note 1		O	
CON1-CON074	GND				
CON1-CON075	GND				
CON1-CON076	VBCLKINote 2			O	
CON1-CON077	GND				

Notes 1. Leave open or perform pin processing according to **(3) Handling of unused pins in C.1.1 Cautions**

2. Clock signal supplied to UDL board from emulator.

Signal List (3/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON1-CON078	GND				
CON1-CON079	VPD14			I/O	5.1 K pull-up
CON1-CON080	VPD12			I/O	5.1 K pull-up
CON1-CON081	VPD10			I/O	5.1 K pull-up
CON1-CON082	VPD8			I/O	5.1 K pull-up
CON1-CON083	VPD6			I/O	5.1 K pull-up
CON1-CON084	VPD4			I/O	5.1 K pull-up
CON1-CON085	VPD2			I/O	5.1 K pull-up
CON1-CON086	VPD0			I/O	5.1 K pull-up
CON1-CON087	GND				
CON1-CON088	GND				
CON1-CON089	GND				
CON1-CON090	GND				
CON1-CON091	VPA12			O	
CON1-CON092	VPA10			O	
CON1-CON093	VPA8			O	
CON1-CON094	VPA6			O	
CON1-CON095	VPA4			O	
CON1-CON096	VPA2			O	
CON1-CON097	VPA0			O	
CON1-CON098	VPUBENZ			O	
CON1-CON099	VPLOCK			O	
CON1-CON100	–[Note]				
CON2-CON001	3 V_{CC}				
CON2-CON002	3 V_{CC}				
CON2-CON003	DMACTV3			O	
CON2-CON004	DMACTV1			O	
CON2-CON005	V_{CC}				
CON2-CON006	V_{CC}				
CON2-CON007	VBD31	D31		I/O	5.1 K pull-up
CON2-CON008	VBD29	D29		I/O	5.1 K pull-up
CON2-CON009	VBD27	D27		I/O	5.1 K pull-up
CON2-CON010	VBD25	D25		I/O	5.1 K pull-up
CON2-CON011	VBD23	D23		I/O	5.1 K pull-up
CON2-CON012	VBD21	D21		I/O	5.1 K pull-up
CON2-CON013	VBD19	D19		I/O	5.1 K pull-up
CON2-CON014	VBD17	D17		I/O	5.1 K pull-up
CON2-CON015	GND				
CON2-CON016	GND				
CON2-CON017	VBD15	D15		I/O	5.1 K pull-up
CON2-CON018	VBD13	D13		I/O	5.1 K pull-up

Note Leave open or perform pin processing according to **(3) Handling of unused pins in C.1.1 Cautions**

Pin List (4/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON2-CON019	VBD11	D11		I/O	5.1 K pull-up
CON2-CON020	VBD9	D9		I/O	5.1 K pull-up
CON2-CON021	VBD7	D7		I/O	5.1 K pull-up
CON2-CON022	VBD5	D5		I/O	5.1 K pull-up
CON2-CON023	VBD3	D3		I/O	5.1 K pull-up
CON2-CON024	VBD1	D1		I/O	5.1 K pull-up
CON2-CON025	GND				
CON2-CON026	GND				
CON2-CON027	GND				
CON2-CON028	GND				
CON2-CON029	VBSTZ	BCYSTZ	BCYSTZ	O	
CON2-CON030	VDSELPZ	–[Note]	SDWEZ	O	
CON2-CON031	VBBENZ3	WRZ3	DQM3	O	
CON2-CON032	VBBENZ1	WRZ1	DQM1	O	
CON2-CON033	GND				
CON2-CON034	GND				
CON2-CON035	PCM5	–[Note]	SELFREF	I	33 K pull-down
CON2-CON036	PCM3	HLDRQZ		I	5.1 K pull-up
CON2-CON037	PCM1	–[Note]		I/O	33 K pull-down
CON2-CON038	GND				
CON2-CON039	GND				
CON2-CON040	VBA27	–[Note]		O	
CON2-CON041	VBA25	A25		O	
CON2-CON042	VBA23	A23		O	
CON2-CON043	VBA21	A21		O	
CON2-CON044	VBA19	A19		O	
CON2-CON045	VBA17	A17		O	
CON2-CON046	VBA15	A15		O	
CON2-CON047	GND				
CON2-CON048	GND				
CON2-CON049	VBA13	A13		O	
CON2-CON050	VBA11	A11		O	
CON2-CON051	VBA9	A9		O	
CON2-CON052	VBA7	A7		O	
CON2-CON053	VBA5	A5		O	
CON2-CON054	VBA3	A3		O	
CON2-CON055	VBA1	A1		O	
CON2-CON056	GND				
CON2-CON057	GND				
CON2-CON058	GND				
CON2-CON059	GND				

Note Leave open or perform pin processing according to **(3) Handling of unused pins in C.1.1 Cautions**

Signal List (5/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON2-CON060	VDCSZ7	CSZ7	CSZ7	O	
CON2-CON061	VDCSZ5	CSZ5/IORDZ	CSZ5/IORDZ	O	
CON2-CON062	VDCSZ3	CSZ3	CSZ3	O	
CON2-CON063	VDCSZ1	CSZ1	CSZ1	O	
CON2-CON064	PCD3	–Note	SDRASZ	O	33 K pull-down
CON2-CON065	PCD1	–Note	SDCLK	O	33 K pull-down
CON2-CON066	PBS3	–Note		I/O	33 K pull-down
CON2-CON067	VBCTYP1	–Note		O	
CON2-CON068	VAREQ	–Note		I	33 K pull-down
CON2-CON069	VBLAST	–Note		I	33 K pull-down
CON2-CON070	VBSIZE0	–Note		O	
CON2-CON071	VBTTYP0	–Note		O	
CON2-CON072	VBWAIT	–Note		I	33 K pull-down
CON2-CON073	GND				
CON2-CON074	GND				
CON2-CON075	GND				
CON2-CON076	VBCLK			I	
CON2-CON077	GND				
CON2-CON078	GND				
CON2-CON079	VPD15			I/O	5.1 K pull-up
CON2-CON080	VPD13			I/O	5.1 K pull-up
CON2-CON081	VPD11			I/O	5.1 K pull-up
CON2-CON082	VPD9			I/O	5.1 K pull-up
CON2-CON083	VPD7			I/O	5.1 K pull-up
CON2-CON084	VPD5			I/O	5.1 K pull-up
CON2-CON085	VPD3			I/O	5.1 K pull-up
CON2-CON086	VPD1			I/O	5.1 K pull-up
CON2-CON087	GND				
CON2-CON088	GND				
CON2-CON089	GND				
CON2-CON090	GND				
CON2-CON091	VPA13			O	
CON2-CON092	VPA11			O	
CON2-CON093	VPA9			O	
CON2-CON094	VPA7			O	
CON2-CON095	VPA5			O	
CON2-CON096	VPA3			O	
CON2-CON097	VPA1			O	
CON2-CON098	VPWRITE			O	
CON2-CON099	VPSTB			O	
CON2-CON100	VPRETR			I	500 pull-down

Note Leave open or perform pin processing according to **(3) Handling of unused pins in C.1.1 Cautions**

Signal List (6/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON3-CON001	DMARQ3			I	33 K pull-down
CON3-CON002	DMARQ2			I	33 K pull-down
CON3-CON003	DMARQ1			I	33 K pull-down
CON3-CON004	DMARQ0			I	33 K pull-down
CON3-CON005	DMTCO3			O	
CON3-CON006	DMTCO2			O	
CON3-CON007	DMTCO1			O	
CON3-CON008	DMTCO0			O	
CON3-CON009	IDMASTP			I	33 K pull-down
CON3-CON010	DCRESZ			I	5.1 K pull-up
CON3-CON011	ERESETZ[Note]			O	
CON3-CON012	GND				
CON3-CON013	GND				
CON3-CON014	GND				
CON3-CON015	DCNMI2			I	50 K pull-down
CON3-CON016	DCNMI1			I	50 K pull-down
CON3-CON017	DCNMI0			I	50 K pull-down
CON3-CON018	INT63			I	50 K pull-down
CON3-CON019	INT62			I	50 K pull-down
CON3-CON020	INT61			I	50 K pull-down
CON3-CON021	INT60			I	50 K pull-down
CON3-CON022	INT59			I	50 K pull-down
CON3-CON023	INT58			I	50 K pull-down
CON3-CON024	INT57			I	50 K pull-down
CON3-CON025	INT56			I	50 K pull-down
CON3-CON026	INT55			I	50 K pull-down
CON3-CON027	INT54			I	50 K pull-down
CON3-CON028	INT53			I	50 K pull-down
CON3-CON029	INT52			I	50 K pull-down
CON3-CON030	INT51			I	50 K pull-down
CON3-CON031	INT50			I	50 K pull-down
CON3-CON032	INT49			I	50 K pull-down
CON3-CON033	INT48			I	50 K pull-down
CON3-CON034	INT47			I	50 K pull-down
CON3-CON035	INT46			I	50 K pull-down
CON3-CON036	INT45			I	50 K pull-down
CON3-CON037	INT44			I	50 K pull-down
CON3-CON038	INT43			I	50 K pull-down
CON3-CON039	INT42			I	50 K pull-down
CON3-CON040	INT41			I	50 K pull-down
CON3-CON041	INT40			I	50 K pull-down

Note Reset signal supplied to UDL board from emulator.

Signal List (7/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON3-CON042	INT39			I	50 K pull-down
CON3-CON043	INT38			I	50 K pull-down
CON3-CON044	INT37			I	50 K pull-down
CON3-CON045	INT36			I	50 K pull-down
CON3-CON046	INT35			I	50 K pull-down
CON3-CON047	INT34			I	50 K pull-down
CON3-CON048	INT33			I	50 K pull-down
CON3-CON049	INT32			I	50 K pull-down
CON3-CON050	INT31			I	50 K pull-down
CON3-CON051	INT30			I	50 K pull-down
CON3-CON052	INT29			I	50 K pull-down
CON3-CON053	INT28			I	50 K pull-down
CON3-CON054	INT27			I	50 K pull-down
CON3-CON055	INT26			I	50 K pull-down
CON3-CON056	INT25			I	50 K pull-down
CON3-CON057	INT24			I	50 K pull-down
CON3-CON058	INT23			I	50 K pull-down
CON3-CON059	INT22			I	50 K pull-down
CON3-CON060	INT21			I	50 K pull-down
CON3-CON061	INT20			I	50 K pull-down
CON3-CON062	INT19			I	50 K pull-down
CON3-CON063	INT18			I	50 K pull-down
CON3-CON064	INT17			I	50 K pull-down
CON3-CON065	INT16			I	50 K pull-down
CON3-CON066	INT15			I	50 K pull-down
CON3-CON067	INT14			I	50 K pull-down
CON3-CON068	INT13			I	50 K pull-down
CON3-CON069	INT12			I	50 K pull-down
CON3-CON070	INT11			I	50 K pull-down
CON3-CON071	INT10			I	50 K pull-down
CON3-CON072	INT9			I	50 K pull-down
CON3-CON073	INT8			I	50 K pull-down
CON3-CON074	INT7			I	50 K pull-down
CON3-CON075	INT6			I	50 K pull-down
CON3-CON076	INT5			I	50 K pull-down
CON3-CON077	INT4			I	50 K pull-down
CON3-CON078	INT3			I	50 K pull-down
CON3-CON079	INT2			I	50 K pull-down
CON3-CON080	INT1			I	50 K pull-down
CON3-CON081	INT0			I	50 K pull-down
CON3-CON082	GND				
CON3-CON083	GND				
CON3-CON084	GND				

Signal List (8/8)

PIN No.	When VSB Bus Is Used	When Memory Controller Is Used		I/O	Processing on Emulator Side
		SRAM	SDRAM		
CON3-CON085	GND				
CON3-CON086	CGREL			I	50 K pull-down
CON3-CON087	HWSTOPRQ			O	
CON3-CON088	SWSTOPRQ			O	
CON3-CON089	STPRQ			O	
CON3-CON090	STPAK			I	4.7 K pull-up
CON3-CON091	DCSTOPZ			I	5.1 K pull-up
CON3-CON092	$TGTV_{DD}$ Note 1			I	33 K pull-down
CON3-CON093	EXTD7 Note 2			I	33 K pull-down
CON3-CON094	EXTD6 Note 2			I	33 K pull-down
CON3-CON095	EXTD5 Note 2			I	33 K pull-down
CON3-CON096	EXTD4 Note 2			I	33 K pull-down
CON3-CON097	EXTD3 Note 2			I	33 K pull-down
CON3-CON098	EXTD2 Note 2			I	33 K pull-down
CON3-CON099	EXTD1 Note 2			I	33 K pull-down
CON3-CON100	EXTD0 Note 2			I	33 K pull-down

Notes 1. UDL board power ON/OFF detection signal

2. External logic probe signal

C.3 NB85E Pin and UDL Connector Correspondence Tables

Correspondence Between NB85E Pins and UDL Connectors (1/6)

NB85E Pins		Pin No.
Pins for NPB	VPA0	CON1-CON097
	VPA1	CON2-CON097
	VPA2	CON1-CON096
	VPA3	CON2-CON096
	VPA4	CON1-CON095
	VPA5	CON2-CON095
	VPA6	CON1-CON094
	VPA7	CON2-CON094
	VPA8	CON1-CON093
	VPA9	CON2-CON093
	VPA10	CON1-CON092
	VPA11	CON2-CON092
	VPA12	CON1-CON091
	VPA13	CON2-CON091
	VPD0	CON1-CON086
	VPD1	CON2-CON086
	VPD2	CON1-CON085
	VPD3	CON2-CON085
	VPD4	CON1-CON084
	VPD5	CON2-CON084
	VPD6	CON1-CON083
	VPD7	CON2-CON083
	VPD8	CON1-CON082
	VPD9	CON2-CON082
	VPD10	CON1-CON081
	VPD11	CON2-CON081
	VPD12	CON1-CON080
	VPD13	CON2-CON080
	VPD14	CON1-CON079
	VPD15	CON2-CON079
	VPWRITE	CON1-CON098
	VPSTB	CON2-CON099
	VPLOCK	CON1-CON099
	VPUBENZ	CON2-CON098
	VPRETR	CON1-CON100
	VPDACT	—[Note]
Pins for VSB	VAREQ	CON2-CON068
	VAACK	CON1-CON068
	VBA0	CON1-CON055
	VBA1	CON2-CON055

Note Indicates that the corresponding pin does not exist in emulator.

Correspondence Between NB85E Pins and UDL Connectors (2/6)

NB85E Pins		Pin No.
Pins for VSB	VBA2	CON1-CON054
	VBA3	CON2-CON054
	VBA4	CON1-CON053
	VBA5	CON2-CON053
	VBA6	CON1-CON052
	VBA7	CON2-CON052
	VBA8	CON1-CON051
	VBA9	CON2-CON051
	VBA10	CON1-CON050
	VBA11	CON2-CON050
	VBA12	CON1-CON049
	VBA13	CON2-CON049
	VBA14	CON1-CON046
	VBA15	CON2-CON046
	VBA16	CON1-CON045
	VBA17	CON2-CON045
	VBA18	CON1-CON044
	VBA19	CON2-CON044
	VBA20	CON1-CON043
	VBA21	CON2-CON043
	VBA22	CON1-CON042
	VBA23	CON2-CON042
	VBA24	CON1-CON041
	VBA25	CON2-CON041
	VBA26[Note]	CON1-CON040
	VBA27[Note]	CON2-CON040
	VBD0	CON1-CON024
	VBD1	CON2-CON024
	VBD2	CON1-CON023
	VBD3	CON2-CON023
	VBD4	CON1-CON022
	VBD5	CON2-CON022
	VBD6	CON1-CON021
	VBD7	CON2-CON021
	VBD8	CON1-CON020
	VBD9	CON2-CON020
	VBD10	CON1-CON019
	VBD11	CON2-CON019
	VBD12	CON1-CON018
	VBD13	CON2-CON018
	VBD14	CON1-CON017
	VBD15	CON2-CON017

Note Undefined operation in the 64 MB mode. Only used in the 256 MB mode.

Correspondence Between NB85E Pins and UDL Connectors (3/6)

NB85E Pins		Pin No.
Pins for VSB	VBD16	CON1-CON014
	VBD17	CON2-CON014
	VBD18	CON1-CON013
	VBD19	CON2-CON013
	VBD20	CON1-CON012
	VBD21	CON2-CON012
	VBD22	CON1-CON011
	VBD23	CON2-CON011
	VBD24	CON1-CON010
	VBD25	CON2-CON010
	VBD26	CON1-CON009
	VBD27	CON2-CON009
	VBD28	CON1-CON008
	VBD29	CON2-CON008
	VBD30	CON1-CON007
	VBD31	CON2-CON007
	VBTTYP0	CON2-CON071
	VBTTYP1	CON1-CON072
	VBSTZ	CON2-CON029
	VBBENZ0	CON1-CON032
	VBBENZ1	CON2-CON032
	VBBENZ2	CON1-CON031
	VBBENZ3	CON2-CON031
	VBSIZE0	CON2-CON070
	VBSIZE1	CON1-CON071
	VBWRITE	CON2-CON073
	VBLOCK	CON1-CON070
	VBCTYP0	CON2-CON067
	VBCTYP1	CON1-CON067
	VBCTYP2	CON2-CON066
	VBSEQ0	–[Note]
	VBSEQ1	–[Note]
	VBSEQ2	–[Note]
	VBBSTR	CON1-CON029
	VBWAIT	CON2-CON072
	VBLAST	CON2-CON069
	VBAHLD	CON1-CON069
	VBDC	CON1-CON030
	VDCSZ0	CON1-CON063
	VDCSZ1	CON2-CON063
	VDCSZ2	CON1-CON062
	VDCSZ3	CON2-CON062

Note Indicates that the corresponding pin does not exist in emulator.

Correspondence Between NB85E Pins and UDL Connectors (4/6)

NB85E Pins		Pin No.
Pins for VSB	VDCSZ4	CON1-CON061
	VDCSZ5	CON2-CON061
	VDCSZ6	CON1-CON060
	VDCSZ7	CON2-CON060
	VDSELPZ	CON2-CON030
Pins for system control	DCRESZ	CON3-CON010
	VBCLK	CON2-CON076
	SWSTOPRQ	CON3-CON088
	HWSTOPRQ	CON3-CON087
	DCSTOPZ	CON3-CON091
	STPRQ	CON3-CON089
	STPAK	CON3-CON090
	CGREL	CON3-CON086
Pins for DMAC	IDMASTP	CON3-CON009
	DMARQ0	CON3-CON004
	DMARQ1	CON3-CON003
	DMARQ2	CON3-CON002
	DMARQ3	CON3-CON001
	DMTCO0	CON3-CON008
	DMTCO1	CON3-CON007
	DMTCO2	CON3-CON006
	DMTCO3	CON3-CON005
	DMACTV0	CON1-CON004
	DMACTV1	CON2-CON004
	DMACTV2	CON1-CON003
	DMACTV3	CON2-CON003
Pins for INTC	DCNMI0	CON3-CON017
	DCNMI1	CON3-CON016
	DCNMI2	CON3-CON015
	INT0	CON3-CON081
	INT1	CON3-CON080
	INT2	CON3-CON079
	INT3	CON3-CON078
	INT4	CON3-CON077
	INT5	CON3-CON076
	INT6	CON3-CON075
	INT7	CON3-CON074
	INT8	CON3-CON073
	INT9	CON3-CON072
	INT10	CON3-CON071
	INT11	CON3-CON070
	INT12	CON3-CON069
	INT13	CON3-CON068
	INT14	CON3-CON067

Correspondence Between NB85E Pins and UDL Connectors (5/6)

NB85E Pins		Pin No.
Pins for INTC	INT15	CON3-CON066
	INT16	CON3-CON065
	INT17	CON3-CON064
	INT18	CON3-CON063
	INT19	CON3-CON062
	INT20	CON3-CON061
	INT21	CON3-CON060
	INT22	CON3-CON059
	INT23	CON3-CON058
	INT24	CON3-CON057
	INT25	CON3-CON056
	INT26	CON3-CON055
	INT27	CON3-CON054
	INT28	CON3-CON053
	INT29	CON3-CON052
	INT30	CON3-CON051
	INT31	CON3-CON050
	INT32	CON3-CON049
	INT33	CON3-CON048
	INT34	CON3-CON047
	INT35	CON3-CON046
	INT36	CON3-CON045
	INT37	CON3-CON044
	INT38	CON3-CON043
	INT39	CON3-CON042
	INT40	CON3-CON041
	INT41	CON3-CON040
	INT42	CON3-CON039
	INT43	CON3-CON038
	INT44	CON3-CON037
	INT45	CON3-CON036
	INT46	CON3-CON035
	INT47	CON3-CON034
	INT48	CON3-CON033
	INT49	CON3-CON032
	INT50	CON3-CON031
	INT51	CON3-CON030
	INT52	CON3-CON029
	INT53	CON3-CON028
	INT54	CON3-CON027
	INT55	CON3-CON026
	INT56	CON3-CON025
	INT57	CON3-CON024
	INT58	CON3-CON023

Correspondence Between NB85E Pins and UDL Connectors (6/6)

NB85E Pins		Pin No.
Pins for INTC	INT59	CON3-CON022
	INT60	CON3-CON021
	INT61	CON3-CON020
	INT62	CON3-CON019
	INT63	CON3-CON018

Caution The following pins are not supported by the emulator:
Pins for VFB, pins for VDB, pins for instruction cache, pins for data cache, pins for RCU, pins for peripheral evaluation chip mode, pins for operation mode settings, pins for test mode, pins for VSB (only when NB85E500/NU85E502 are used).

C.4 NB85E500 Pins and CON1 to CON3 Correspondence Tables

Correspondence Between NB85E500 Pins and CON1 to CON3 (1/3)

NB85E500 Pins		Pin No.
Pins for external memory connection	A0	CON1-CON055
	A1	CON2-CON055
	A2	CON1-CON054
	A3	CON2-CON054
	A4	CON1-CON053
	A5	CON2-CON053
	A6	CON1-CON052
	A7	CON2-CON052
	A8	CON1-CON051
	A9	CON2-CON051
	A10	CON1-CON050
	A11	CON2-CON050
	A12	CON1-CON049
	A13	CON2-CON049
	A14	CON1-CON046
	A15	CON2-CON046
	A16	CON1-CON045
	A17	CON2-CON045
	A18	CON1-CON044
	A19	CON2-CON044
	A20	CON1-CON043
	A21	CON2-CON043
	A22	CON1-CON042
	A23	CON2-CON042
	A24	CON1-CON041
	A25	CON2-CON041
	D0	CON1-CON024
	D1	CON2-CON024
	D2	CON1-CON023
	D3	CON2-CON023
	D4	CON1-CON022
	D5	CON2-CON022
	D6	CON1-CON021
	D7	CON2-CON021
	D8	CON1-CON020
	D9	CON2-CON020
	D10	CON1-CON019
	D11	CON2-CON019
	D12	CON1-CON018
	D13	CON2-CON018
	D14	CON1-CON017

Correspondence Between NB85E500 Pins and CON1 to CON3 (2/3)

NB85E500 Pins		Pin No.
Pins for external memory connection	D15	CON2-CON017
	D16	CON1-CON014
	D17	CON2-CON014
	D18	CON1-CON013
	D19	CON2-CON013
	D20	CON1-CON012
	D21	CON2-CON012
	D22	CON1-CON011
	D23	CON2-CON011
	D24	CON1-CON010
	D25	CON2-CON010
	D26	CON1-CON009
	D27	CON2-CON009
	D28	CON1-CON008
	D29	CON2-CON008
	D30	CON1-CON007
	D31	CON2-CON007
	RDZ	CON1-CON030
	WRZ0	CON1-CON032
	WRZ1	CON2-CON032
	WRZ2	CON1-CON031
	WRZ3	CON2-CON031
	IORDZ[Note 1]	CON2-CON061
	IOWRZ[Note 1]	CON1-CON062
	WAITZ	CON1-CON037
	HLDRQZ	CON2-CON036
	HLDAKZ	CON1-CON036
	DC0	–[Note 2]
	DC1	–[Note 2]
	DC2	–[Note 2]
	DC3	–[Note 2]
	CSZ0	CON1-CON063
	CSZ1	CON2-CON063
	CSZ2[Note 1]	CON1-CON062
	CSZ3	CON2-CON062
	CSZ4	CON1-CON061
	CSZ5[Note 1]	CON2-CON061
	CSZ6	CON1-CON060
	CSZ7	CON2-CON060
	BENZ0	–[Note 2]
	BENZ1	–[Note 2]

Notes 1. CS5Z and IORDZ are mutually exclusive, as are CS2Z and IOWRZ i.e., only one pin in each pair can be used.

2. Indicates that the corresponding pin does not exist in emulator.

Correspondence Between NB85E500 Pins and CON1 to CON3 (3/3)

NB85E500 Pins		Pin No.
Pins for external memory connection	BENZ2	–[Note]
	BENZ3	–[Note]
	BCYSTZ	CON2-CON029
	REFRQZ	CON1-CON035
	SELFREF	CON2-CON035
	SDCLK	CON2-CON065

Note Indicates that the corresponding pin does not exist in emulator.

Caution The following pins are not supported by the emulator:
Pins for NB85E connection, pins for initial setting, pins for NU85E502 connection, pins for test mode

C.5 NU85E502 Pins and CON1 to CON3 Correspondence Tables

Correspondence Between NU85E502 pins and CON1 to CON3 (1/2)

NU85E502 Pins		Pin No.
Pins for external memory connection	A0	CON1-CON055
	A1	CON2-CON055
	A2	CON1-CON054
	A3	CON2-CON054
	A4	CON1-CON053
	A5	CON2-CON053
	A6	CON1-CON052
	A7	CON2-CON052
	A8	CON1-CON051
	A9	CON2-CON051
	A10	CON1-CON050
	A11	CON2-CON050
	A12	CON1-CON049
	A13	CON2-CON049
	A14	CON1-CON046
	A15	CON2-CON046
	A16	CON1-CON045
	A17	CON2-CON045
	A18	CON1-CON044
	A19	CON2-CON044
	A20	CON1-CON043
	A21	CON2-CON043
	A22	CON1-CON042
	A23	CON2-CON042
	A24	CON1-CON041
	A25	CON2-CON041
	D0	CON1-CON024
	D1	CON2-CON024
	D2	CON1-CON023
	D3	CON2-CON023
	D4	CON1-CON022
	D5	CON2-CON022
	D6	CON1-CON021
	D7	CON2-CON021
	D8	CON1-CON020
	D9	CON2-CON020
	D10	CON1-CON019
	D11	CON2-CON019
	D12	CON1-CON018
	D13	CON2-CON018
	D14	CON1-CON017

Correspondence Between NU85E502 pins and CON1 to CON3 (2/2)

NU85E502 Pins		Pin No.
Pins for external memory connection	D15	CON2-CON017
	D16	CON1-CON014
	D17	CON2-CON014
	D18	CON1-CON013
	D19	CON2-CON013
	D20	CON1-CON012
	D21	CON2-CON012
	D22	CON1-CON011
	D23	CON2-CON011
	D24	CON1-CON010
	D25	CON2-CON010
	D26	CON1-CON009
	D27	CON2-CON009
	D28	CON1-CON008
	D29	CON2-CON008
	D30	CON1-CON007
	D31	CON2-CON007
	SDRASZ	CON2-CON064
	SDCASZ	CON1-CON064
	SDWEZ	CON2-CON030
	CKE	CON1-CON065
	DQM0	CON1-CON032
	DQM1	CON2-CON032
	DQM2	CON1-CON031
	DQM3	CON2-CON031

Caution The following pins are not supported by the emulator:
Pins for NB85E connection, pins for NB85E500 connection, pins for test mode

APPENDIX D ELECTRICAL SPECIFICATIONS OF UDL INTERFACE

The electrical specifications of the UDL interface when this product is connected to the IE-V850E-MC-A are described below.

A voltage of 3.3 V ±10% is supplied from the emulator as V_{DD}.

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage (emulator)	V_{DD}		–0.5 to +4.6	V
Supply voltage (target pin)	TV_{DD}		–0.5 to +4.6	V
Input voltage	V_{I1}	V_{DD} = 3.0 V to 3.6 V	–0.5 to V_{DD}+0.5	V
Clock input voltage	V_K	V_{DD} = 3.0 V to 3.6 V	–0.5 to V_{DD}+1.0	V
Low-level output current	I_{OL}	Per pin	40	mA
		Total of all pins	400	mA
High-level output current	I_{OH}	Per pin	–40	mA
		Total of all pins	–400	mA
Output voltage	V_O	V_{DD} = 3.0 V to 3.6 V	–0.5 to V_{DD}+0.5	V
Operating ambient temperature	T_A		0 to +45	°C

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

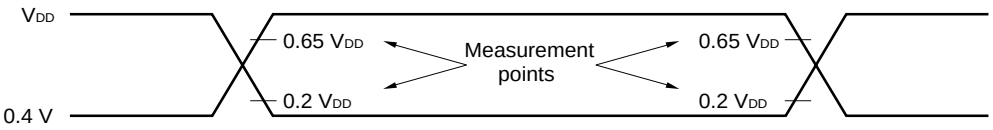
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz 0 V for unmeasured pins			10	pF
I/O capacitance	C_{IO}				10	pF
Output capacitance	C_O				10	pF

DC Characteristics (T_A = -40°C to +85°C, V_{DD} 3.0 V to 3.6 V, V_{SS} = 0 V)

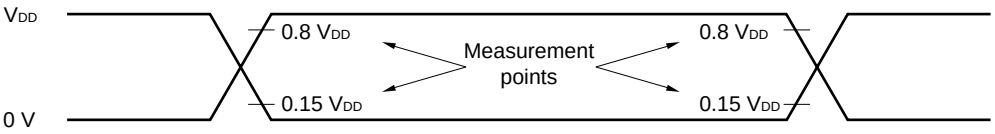
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}		0.65 V_{DD}		V_{DD}+0.3	V
Low-level input voltage	V_{IL}		–0.5		0.2 V_{DD}	V
High-level clock input voltage	V_{XH}	X1 pin	0.8 V_{DD}		V_{DD}+0.3	V
Low-level clock input voltage	V_{XL}	X1 pin	–0.3		0.15 V_{DD}	V
High-level output voltage	V_{OH}	I_{OH} = –2 mA	V_{DD} – 0.2			V
Low-level output voltage	V_{OL}	I_{OL} = 10 mA			0.4	V
High-level input leak current	I_{LIH}	V_I = V_{DD}			10	μA
Low-level input leak current	I_{LIL}	V_I = 0 V			–10	μA
High-level output leak current	I_{LOH}	V_O = V_{DD} – 0.4 V			10	μA
Low-level output leak current	I_{LOL}	V_O = 0.4 V			–10	μA
High-level output current	I_{OH}	V_O = V_{DD} – 0.4 V			2	mA
Low-level output current	I_{OL}	V_O = 0.4 V			–12	mA

Remark TYP. values are reference values when T_A = 25°C and V_{DD} = 3.3 V.

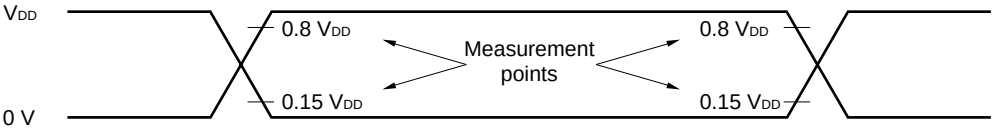
AC Test Input Waveform (Other Than $\overline{\text{RESET}}$)



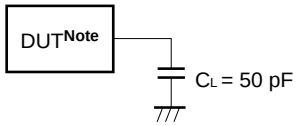
AC Test Input Waveform ($\overline{\text{RESET}}$)



AC Test Output Measurement Points



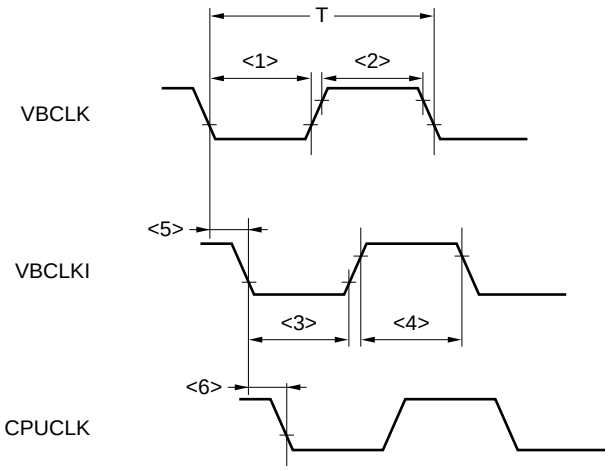
Load Conditions



Note DUT stands for device under test.

Caution If the load capacitance exceeds 50 pF due to the circuit configuration, the load capacitance of this device must be maintained at 50 pF or lower using buffers.

Clock Timing

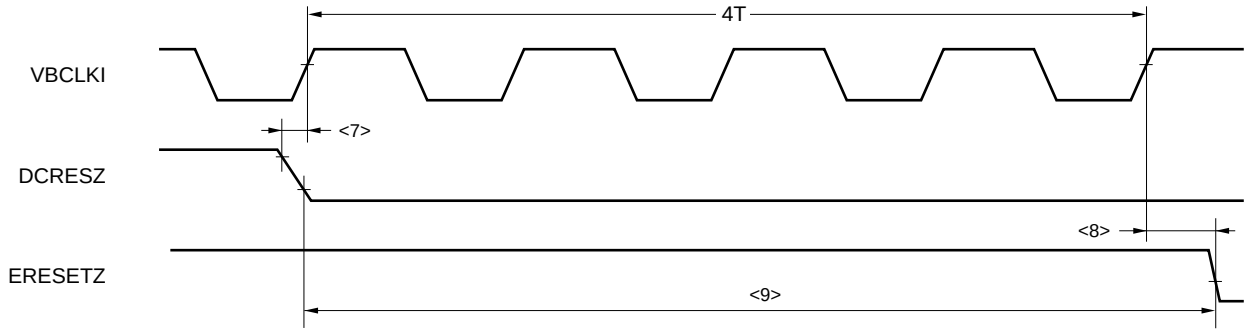


Clock Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		MIN.	MAX.	Unit
VBCLK low-level width	t_{WKIL}	<1>	11		ns
VBCLK high-level width	t_{WKIH}	<2>	11		ns
VBCLKI low-level width	t_{WKOL}	<3>	11		ns
VBCLKI high-level width	t_{WKOH}	<4>	11		ns
VBCLKI delay time (from VBCLK ↓)	t_{CLD1}	<5>		18	ns
CPUCLK delay time (from VBCLKI ↓)	t_{CLD2}	<6>		10	ns

Remark CPUCLK: Clock used inside evaluation chip

Reset Timing

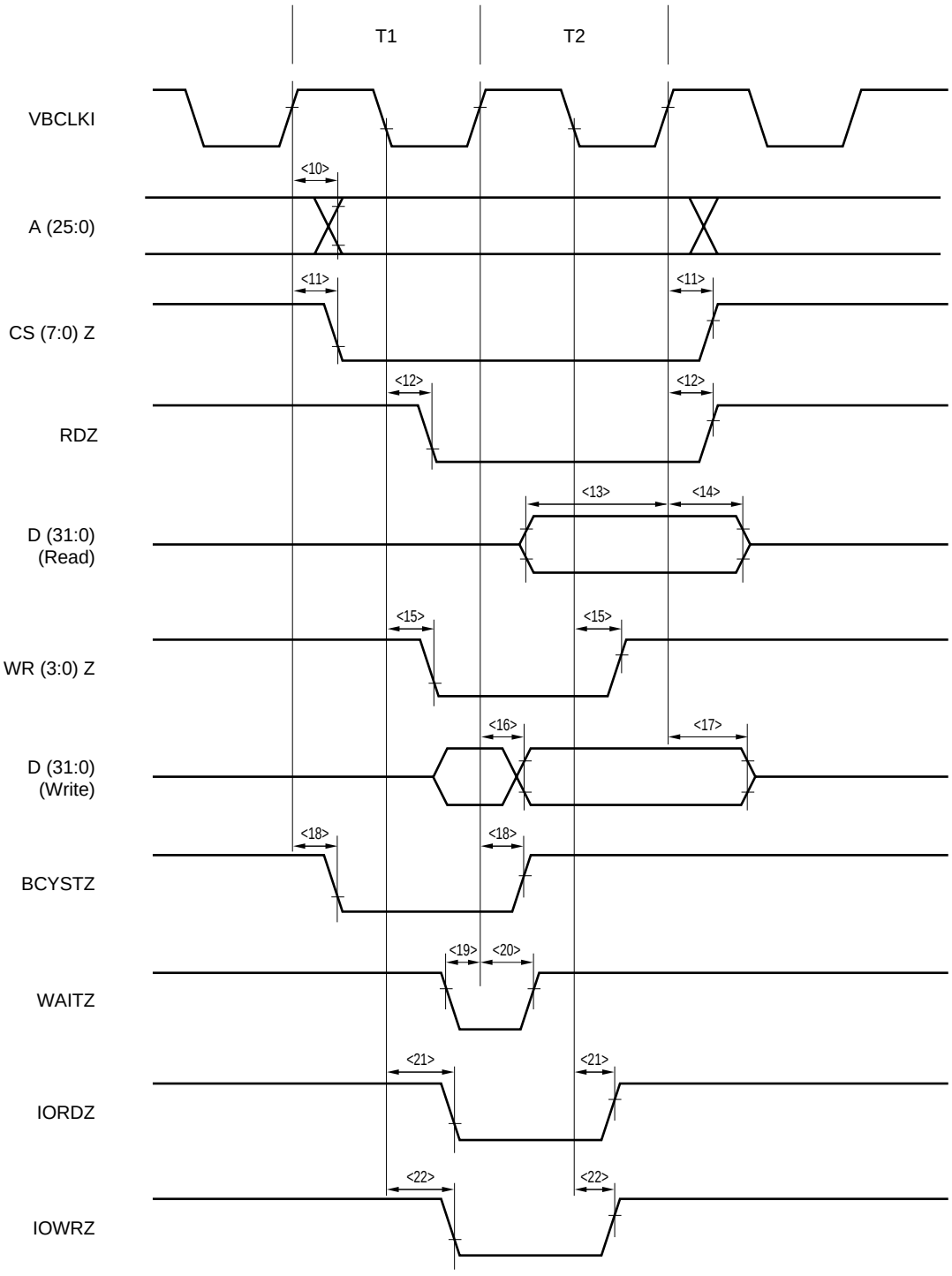


ERESETZ Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Asynchronous		Synchronous		Unit
			MIN.	MAX.	In Relation to VBCLKI		
					MIN.	MAX.	
DCRESZ setup (to VBCLKI ↑)	t_{SKRST}	<7>			12	17	ns
ERESETZ delay time (from VBCLKI ↑)	t_{DKERST}	<8>			12	17	ns
ERESETZ delay time (from DCRESZ ↓)	t_{DRST}	<9>	4T-5	17			ns

Target Interface

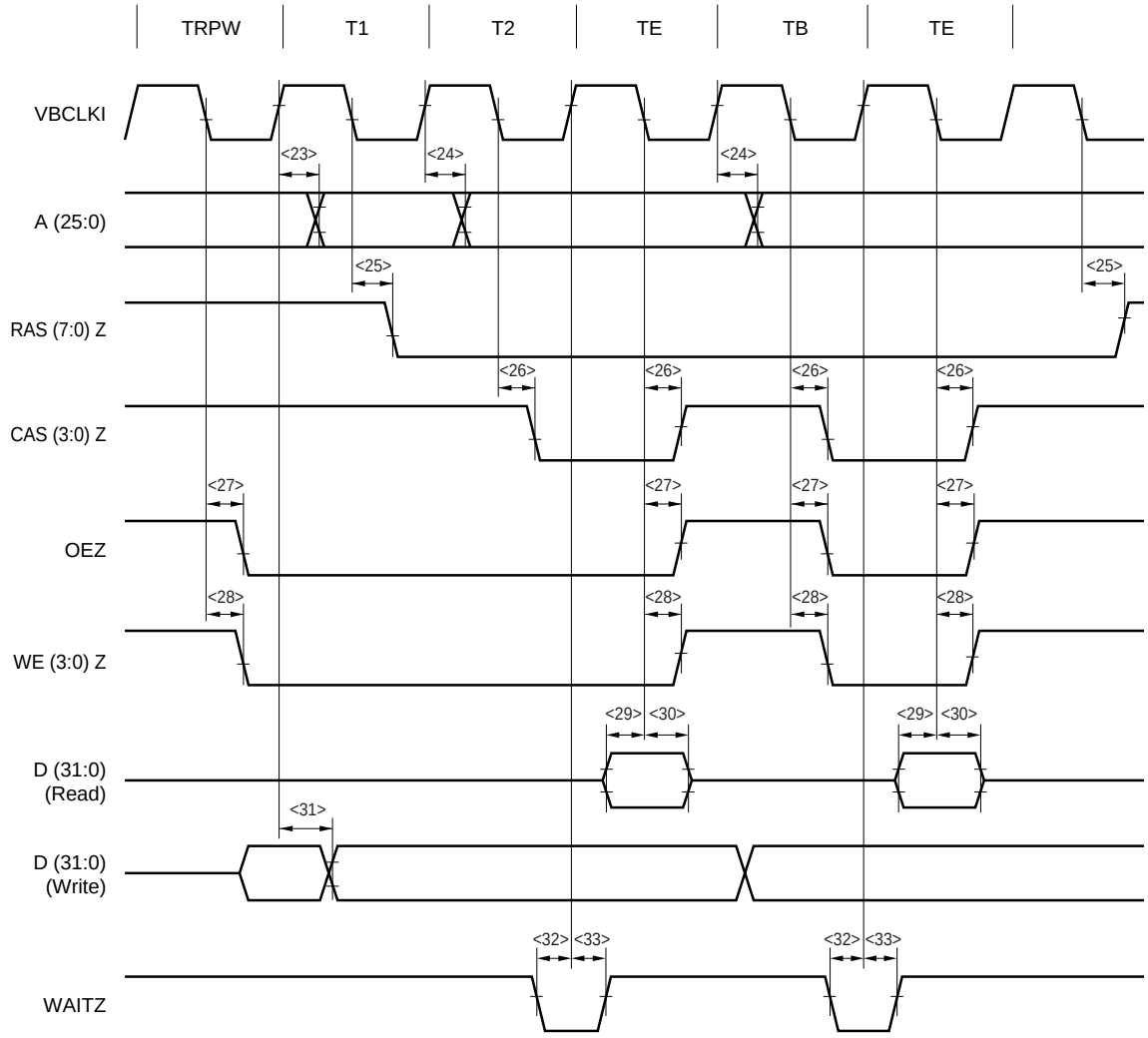
SRAM/page ROM cycle (other than bus mode)



SRAM/Page ROM Cycle (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
A (25:0) delay time (from VBCLKI ↑)	t_{AD}	<10>		18	ns
CS (7:0) Z delay time (from VBCLKI ↑)	t_{CSZD}	<11>		18	ns
RDZ delay time (from VBCLKI)	t_{RDZD}	<12>		13	ns
D (31:0) setup time (to VBCLKI ↑)	t_{DS}	<13>	–15		ns
D (31:0) hold time (from VBCLKI ↑)	t_{DH}	<14>	11		ns
WR (3:0) Z delay time (from VBCLKI ↓)	t_{WRZD}	<15>		13	ns
D (31:0) delay time 1 (from VBCLKI ↑)	t_{DD1}	<16>		26	ns
D (31:0) delay time 2 (from VBCLKI ↑)	t_{DD2}	<17>		23	ns
BCYSTZ delay time (from VBCLKI ↑)	t_{BCYD}	<18>		13	ns
WAITZ setup time (to VBCLKI ↑)	t_{WTS}	<19>	–7		ns
WAITZ hold time (from VBCLKI ↑)	t_{WTH}	<20>	11		ns
IORDZ delay time (from VBCLKI ↓)	t_{IORD}	<21>		13	ns
IOWRZ delay time (from VBCLKI ↓)	t_{IOWR}	<22>		13	ns

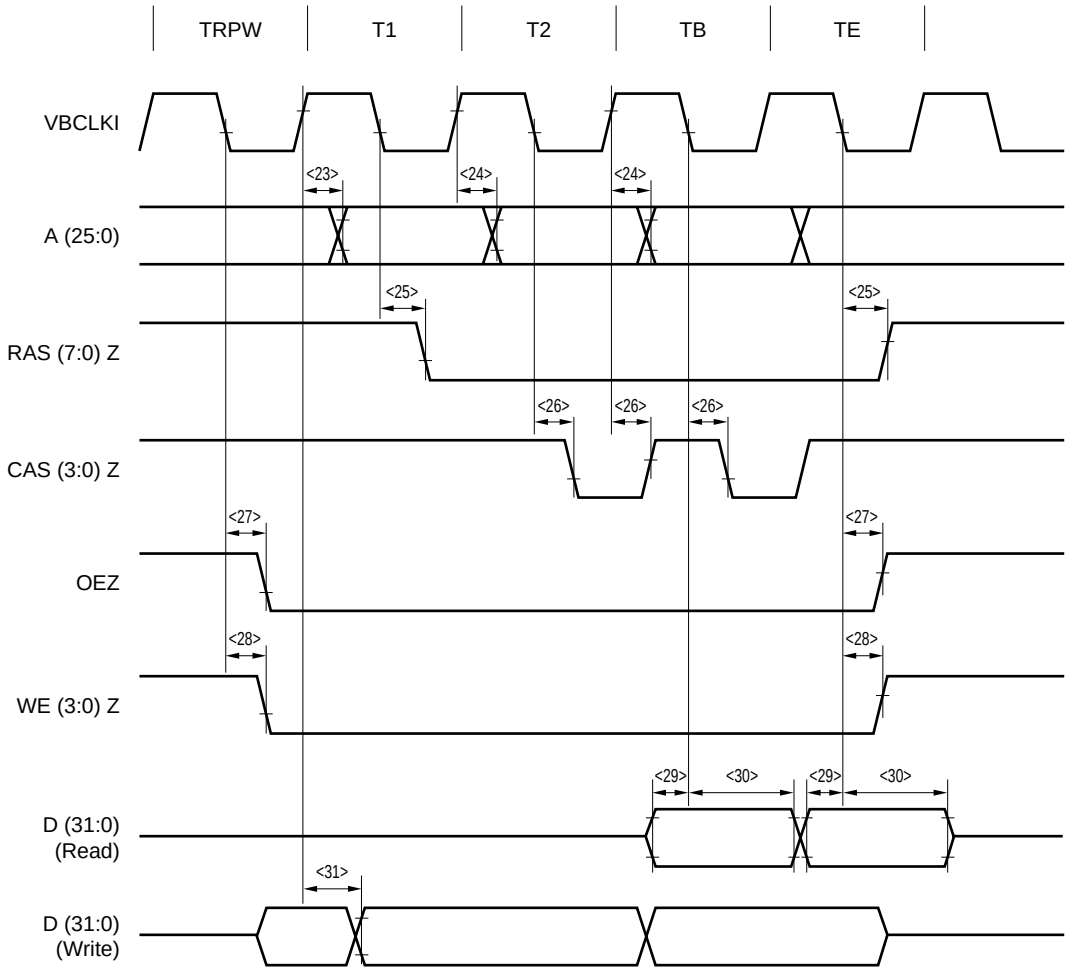
DRAM Cycle (Fast Page)



DRAM Cycle (Fast Page) (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
Row address delay time (from VBCLKI ↑)	t_{RAD}	<23>		17	ns
Column address delay time (from VBCLKI ↑)	t_{CAD}	<24>		17	ns
RAS (7:0) Z delay time (from VBCLKI ↓)	t_{RASD}	<25>		13	ns
CAS (3:0) Z delay time (from VBCLKI ↓)	t_{CASD}	<26>		14	ns
OEZ delay time (from VBCLKI ↓)	t_{OED}	<27>		13	ns
WE (3:0) Z delay time (from VBCLKI ↓)	t_{WED}	<28>		13	ns
D (31:0) setup time (to VBCLKI ↓)	t_{DS3}	<29>	–13		ns
D (31:0) hold time (from VBCLKI ↓)	t_{DH3}	<30>	11		ns
D (31:0) delay time 1 (from VBCLKI ↑)	t_{DD1}	<31>		26	ns
WAITZ setup time (to VBCLKI ↑)	t_{WTS}	<32>	–7		ns
WAITZ hold time (from VBCLKI ↑)	t_{WTH}	<33>	11		ns

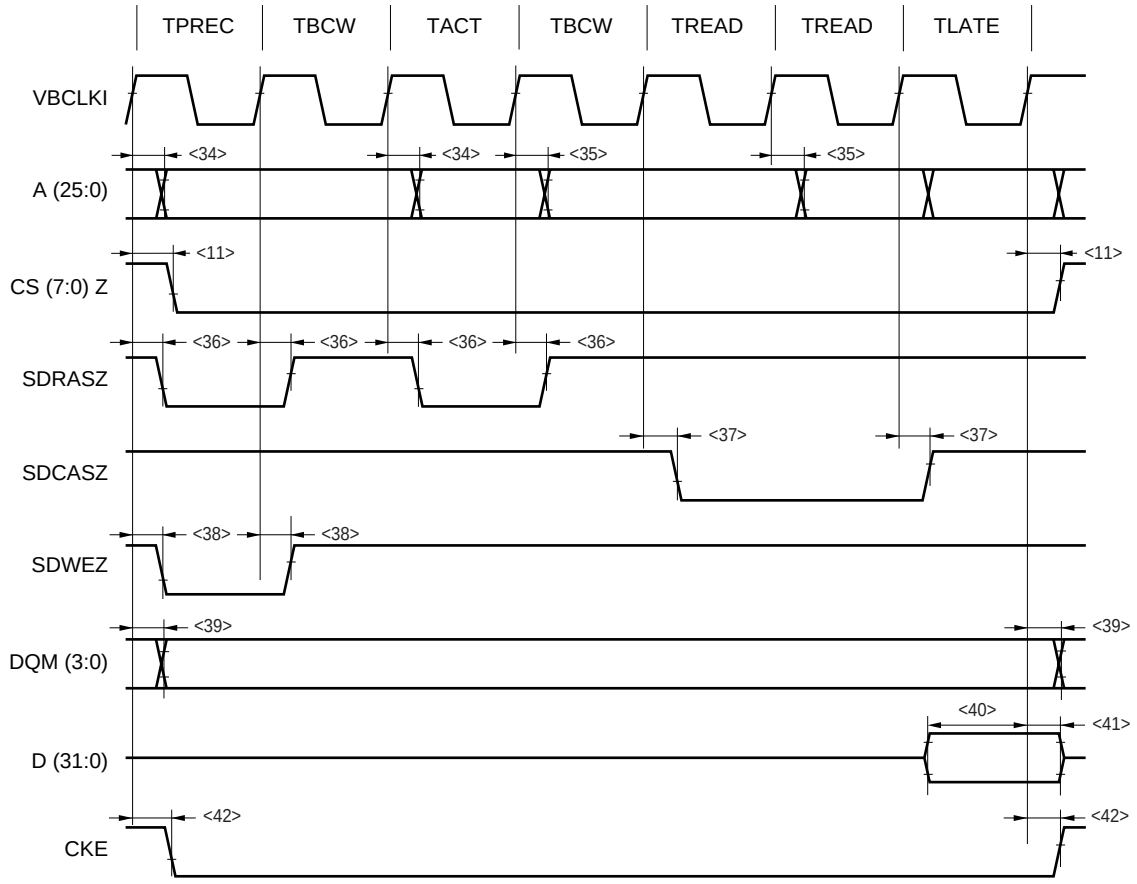
DRAM Cycle (Hyper Page (EDO))



DRAM Cycle (Hyper Page (EDO)) (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
Row-address delay time (from VBCLKI ↑)	t_{RAD}	<23>		17	ns
Column address delay time (from VBCLKI ↑)	t_{CAD}	<24>		17	ns
RAS (7:0) Z delay time (from VBCLKI ↓)	t_{RASD}	<25>		13	ns
CAS (3:0) Z delay time (from VBCLKI)	t_{CASD}	<26>		14	ns
OEZ delay time (from VBCLKI ↓)	t_{OED}	<27>		13	ns
WE (3:0) Z delay time (from VBCLKI ↓)	t_{WED}	<28>		13	ns
D (31:0) setup time (to VBCLKI ↓)	t_{DS3}	<29>	–13		ns
D (31:0) hold time (from VBCLKI ↓)	t_{DH3}	<30>	11		ns
D (31:0) delay time 1 (from VBCLKI ↑)	t_{DD1}	<31>		26	ns

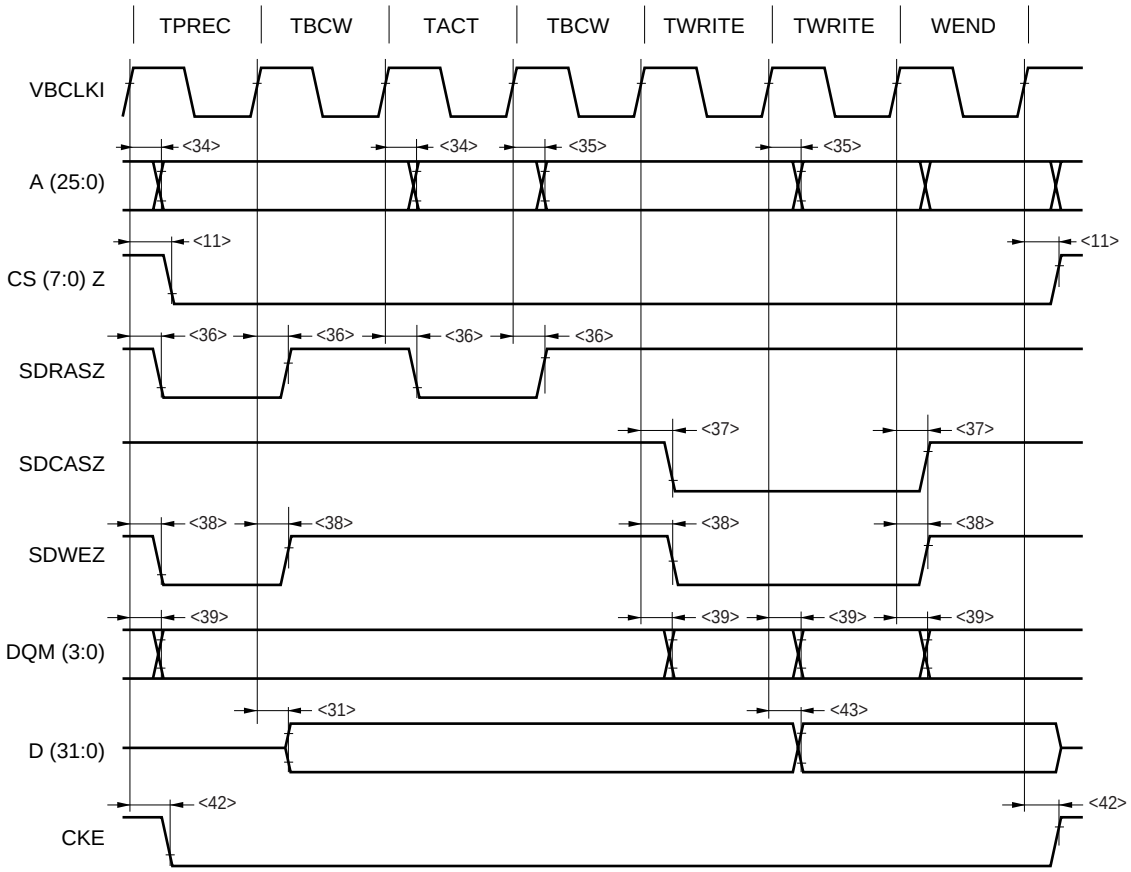
SDRAM Cycle (Read)



SDRAM Cycle (Read) (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
Row address delay time (from VBCLKI ↑)	t_{SDRAD}	<34>	14	21	ns
Column address delay time (from VBCLKI ↑)	t_{SDCAD}	<35>	14	21	ns
CS (7:0) Z delay time (from VBCLKI ↑)	t_{CSZD}	<11>		18	ns
SDRASZ delay time (from VBCLKI ↑)	t_{SRD}	<36>	11.5	13	ns
SDCASZ delay time (from VBCLKI ↑)	t_{SCD}	<37>	11.5	13	ns
SDWEZ delay time (from VBCLKI ↑)	t_{SWD}	<38>	11.5	13	ns
DQM (3:0) delay time (from VBCLKI ↑)	t_{DQD}	<39>	11.5	13	ns
D (31:0) setup time (to VBCLKI ↑)	t_{DS4}	<40>	0.5		ns
D (31:0) hold time (from VBCLKI ↑)	t_{DH4}	<41>	11		ns
CKE delay time (from VBCLKI ↑)	t_{CKED}	<42>	11.5	13	ns

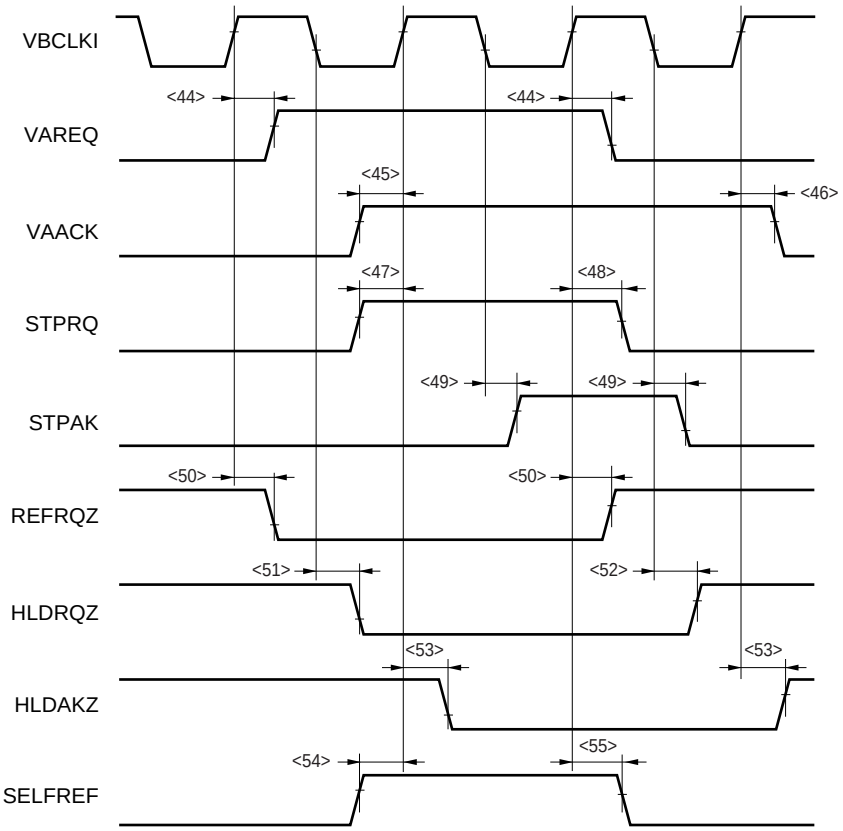
SDRAM Cycle (Write)



SDRAM Cycle (Write) (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
Row address delay time (from VBCLKI ↑)	t_{SDRAD}	<34>	14	21	ns
Column address delay time (from (VBCLKI ↑)	t_{SDCAD}	<35>	14	21	ns
CS (7:0) Z delay time (from VBCLKI ↑)	t_{CSZD}	<11>		18	ns
SDRASZ delay time (from VBCLKI ↑)	t_{SRD}	<36>	11.5	13	ns
SDCASZ delay time (from VBCLKI ↑)	t_{SCD}	<37>	11.5	13	ns
SDWEZ delay time (from VBCLKI ↑)	t_{SWD}	<38>	11.5	13	ns
DQM (3:0) delay time (from VBCLKI ↑)	t_{DQD}	<39>	11.5	13	ns
D (31:0) delay time 1 (from VBCLKI ↑)	t_{DD1}	<31>		26	ns
D (31:0) delay time 2 (from VBCLKI ↑)	t_{DD2}	<43>		23	ns
CKE delay time (from VBCLKI ↑)	t_{CKED}	<42>	11.5	13	ns

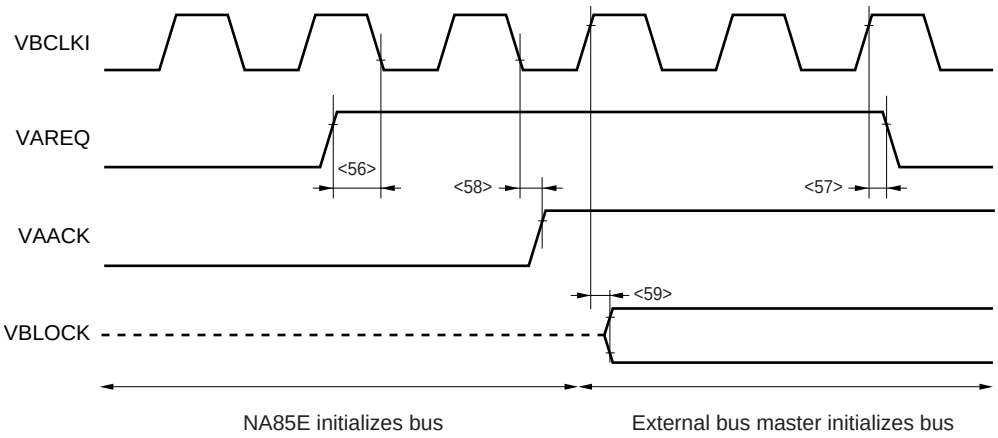
Bus Arbitration Interface



Bus Arbitration Interface (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
VAREQ delay time (from VBCLKI ↑)	t_{ARQD}	<44>		12	ns
VAACK setup time (to VBCLKI ↑)	t_{AKS}	<45>	–8		ns
VAACK hold time (from VBCLKI ↑)	t_{AKH}	<46>	11		ns
STPRQ setup time (to VBCLKI ↑)	t_{STRQS}	<47>	–8		ns
STPRQ hold time (from VBCLKI ↑)	t_{STRQH}	<48>	11		ns
STPAK delay time (from VBCLKI ↓)	t_{STAKD}	<49>		12	ns
REFRQZ delay time (from VBCLKI ↓)	t_{RERQD}	<50>		12	ns
HLDRQZ setup time (to VBCLKI ↓)	t_{HLRQS}	<51>	–8		ns
HLDRQZ hold time (from VBCLKI ↓)	t_{HLRQH}	<52>	11		ns
HLDAKZ delay time (from VBCLKI ↑)	t_{HLAKD}	<53>		12	ns
SELFREF setup time (to VBCLKI ↑)	t_{SLRFS}	<54>	–8		ns
SELFREF hold time (from VBCLKI ↑)	t_{SLRFH}	<55>	11		ns

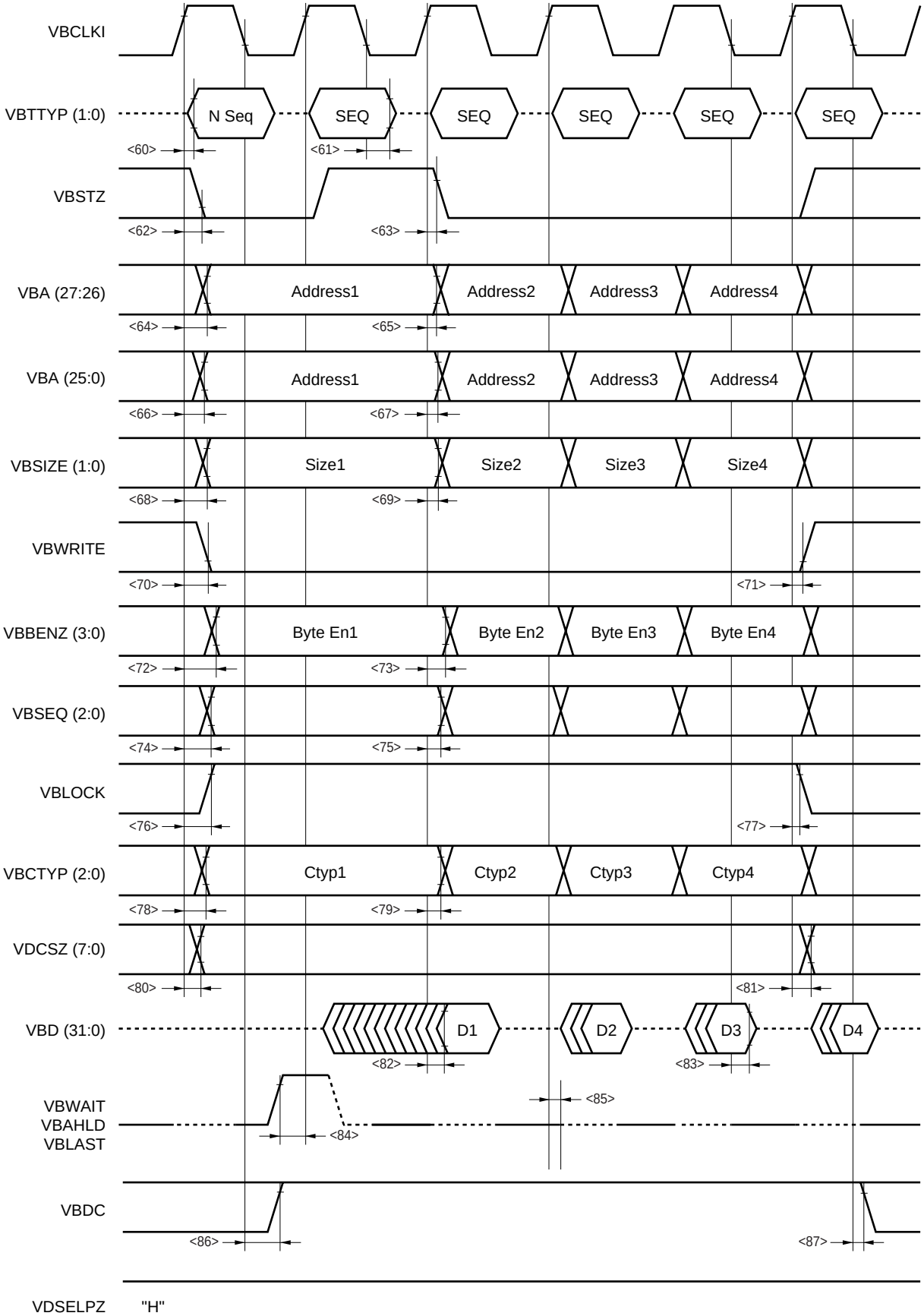
SOC Interface VSB Arbitration Timing



SOC Interface VSB Arbitration Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
VAREQ setup time (to VBCLKI ↓)	t_{SKQ}	<56>	–6		ns
VAREQ hold time (from VBCLKI ↑)	t_{HKQ}	<57>	13		ns
VAACK delay time (from VBCLK ↓)	t_{DKACK}	<58>	12	17	ns
VBLOCK delay time (from VBCLKI ↑)	$t_{DKBLOCK}$	<59>	12	17	ns

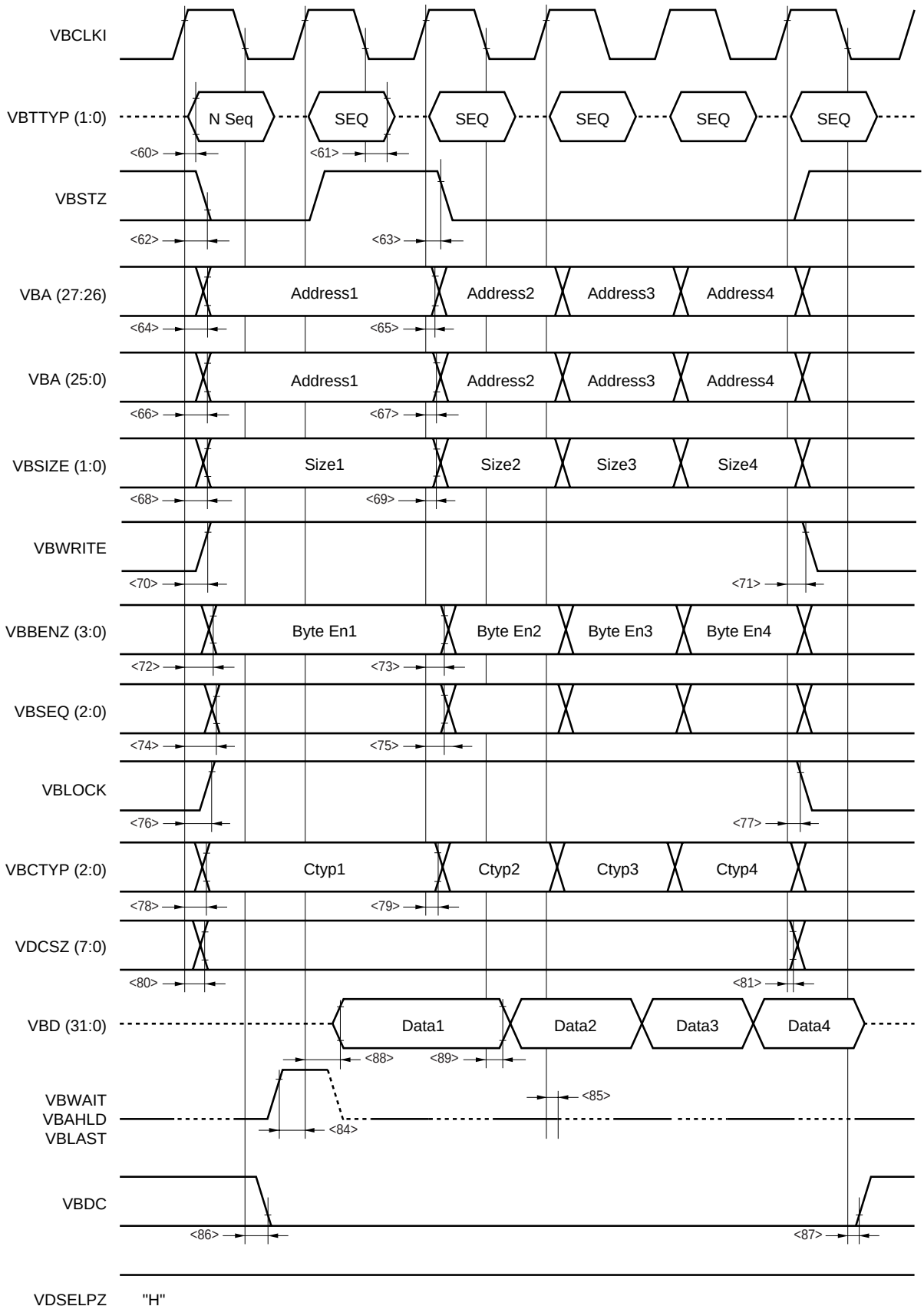
VSB Master Read Timing



VSB Timer Read Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
VBTTYP (1:0) delay time (from VBCLKI ↑)	t_{DKT1}	<60>	12	17	ns
VBTTYP (1:0) hold time (from VBCLKI ↓)	t_{HKT1}	<61>	11		ns
VBSTZ delay time (from VBCLKI ↑)	t_{DKT2}	<62>	12	17	ns
VBSTZ hold time (from VBCLKI ↑)	t_{HKT2}	<63>	11		ns
VBA (27:26) delay time (from VBCLKI ↑)	t_{DKA1}	<64>	19.5	24.5	ns
VBA (27:26) hold time (from VBCLKI ↑)	t_{HKA1}	<65>	18.5		ns
VBA (25:0) delay time (from VBCLKI ↑)	t_{DKA2}	<66>	12	17	ns
VBA (25:0) hold time (from VBCLKI ↑)	t_{HKA2}	<67>	11		ns
VBSIZE (1:0) delay time (from VBCLKI ↑)	t_{DKS1}	<68>	12	17	ns
VBSIZE (1:0) hold time (from VBCLKI ↑)	t_{HKS1}	<69>	11		ns
VBWRITE delay time (from VBCLKI ↑)	t_{DKS2}	<70>	12	17	ns
VBWRITE hold time (from VBCLKI ↑)	t_{HKS2}	<71>	11		ns
VBBENZ (3:0) delay time (from VBCLKI ↑)	t_{DKS3}	<72>	12	17	ns
VBBENZ (3:0) hold time (from VBCLKI ↑)	t_{HKS3}	<73>	11		ns
VBSEQ (2:0) delay time (from VBCLKI ↑)	t_{DKS4}	<74>	12	17	ns
VBSEQ (2:0) hold time (from VBCLKI ↑)	t_{HKS4}	<75>	11		ns
VBLOCK delay time (from VBCLKI ↑)	t_{DKS5}	<76>	12	17	ns
VBLOCK hold time (from VBCLKI ↑)	t_{HKS5}	<77>	11		ns
VBCTYP (2:0) delay time (from VBCLKI ↑)	t_{DKS6}	<78>	12	17	ns
VBCTYP (2:0) hold time (from VBCLKI ↑)	t_{HKS6}	<79>	11		ns
VDCSZ (7:0) delay time (from VBCLI ↑)	t_{DKC}	<80>	12	17	ns
VDCSZ (7:0) hold time (from VBCLKI ↑)	t_{HKC}	<81>	11		ns
VBD (31:0) setup time (to VBCLKI ↑)	t_{SKD}	<82>	2		ns
VBD (31:0) hold time (from VBCLKI ↓)	t_{HKDI}	<83>	13		ns
VBWAIT setup time (to VBCLKI ↑)	t_{SKW}	<84>	–6		ns
VBWAIT hold time (from VBCLKI ↑)	t_{HKW}	<85>	13		ns
VBAHLD setup time (to VBCLKI ↑)	t_{SKW}	<84>	–6		ns
VBAHLD hold time (from VBCLKI ↑)	t_{HKW}	<85>	13		ns
VBLAST setup time (to VBCLKI ↑)	t_{SKW}	<84>	–6		ns
VBLAST hold time (from VBCLKI ↑)	t_{HKW}	<85>	13		ns
VBDC delay time (from VBCLKI ↓)	t_{DKS7}	<86>		4.6	ns
VBDC hold time (from VBCLKI ↓)	t_{HKS7}	<87>	0		ns

VSB Master Write Timing

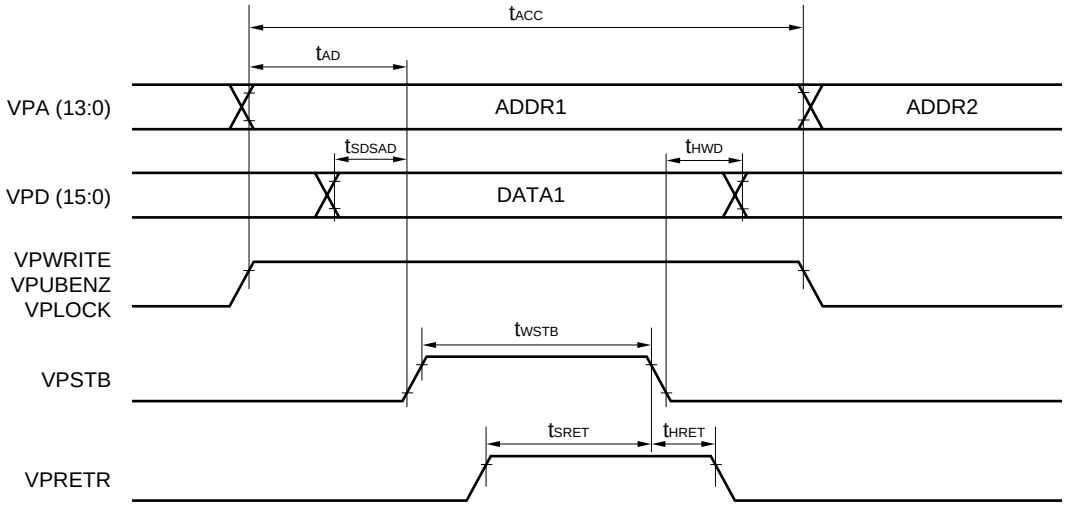


VSB Master Write Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

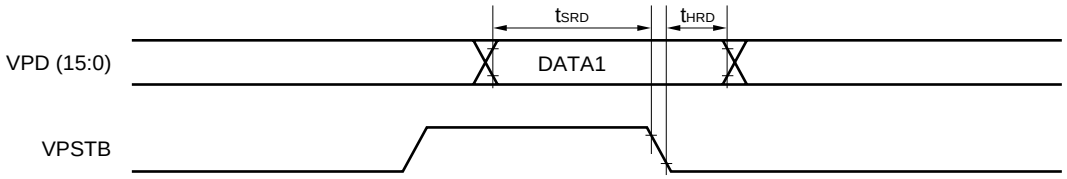
Parameter	Symbol		Synchronous		Unit
			In Relation to VBCLKI		
			MIN.	MAX.	
VBTTYP (1:0) delay time (from VBCLKI ↑)	t_{DKT1}	<60>	12	17	ns
VBTTYP (1:0) hold time (from VBCLKI ↑)	t_{HKT1}	<61>	11		ns
VBSTZ delay time (from VBCLKI ↑)	t_{DKT2}	<62>	12	17	ns
VBSTZ hold time (from VBCLKI ↑)	t_{HKT2}	<63>	11		ns
VBA (27:26) delay time (from VBCLKI ↑)	t_{DKA1}	<64>	19.5	24.5	ns
VBA (27:26) hold time (from VBCLKI ↑)	t_{HKA1}	<65>	18.5		ns
VBA (25:0) delay time (from VBCLKI ↑)	t_{DKA2}	<66>	12	17	ns
VBA (25:0) hold time (from VBCLKI ↑)	t_{HKA2}	<67>	11		ns
VBSIZE (1:0) delay time (from VBCLKI ↑)	t_{DKS1}	<68>	12	17	ns
VBSIZE (1:0) hold time (from VBCLKI ↑)	t_{HKS1}	<69>	11		ns
VBWRITE delay time (from VBCLKI ↑)	t_{DKS2}	<70>	12	17	ns
VBWRITE hold time (from VBCLKI ↑)	t_{HKS2}	<71>	11		ns
VBBENZ (3:0) delay time (from VBCLKI ↑)	t_{DKS3}	<72>	12	17	ns
VBBENZ (3:0) hold time (from VBCLKI ↑)	t_{HKS3}	<73>	11		ns
VBSEQ (2:0) delay time (from VBCLKI ↑)	t_{DKS4}	<74>	12	17	ns
VBSEQ (2:0) hold time (from VBCLKI ↑)	t_{HKS4}	<75>	11		ns
VBLOCK delay time (from VBCLKI ↑)	t_{DKS5}	<76>	12	17	ns
VBLOCK hold time (from VBCLKI ↑)	t_{HKS5}	<77>	11		ns
VBCTYP (2:0) delay time (from VBCLKI ↑)	t_{DKS6}	<78>	12	17	ns
VBCTYP (2:0) hold time (from VBCLKI ↑)	t_{HKS6}	<79>	11		ns
VDCSZ (7:0) delay time (from VBCLKI ↑)	t_{DKC}	<80>	12	17	ns
VDCSZ (7:0) hold time (from VBCLKI ↑)	t_{HKC}	<81>	11		ns
VBD (31:0) delay time (from VBCLKI ↑)	t_{DKD0}	<88>	12	25	ns
VBD (31:0) delay time (from VBCLKI ↓)	t_{DKD1}	<89>	12	25	ns
VBWAIT setup time (to VBCLKI ↑)	t_{SKW}	<84>	–6		ns
VBWAIT hold time (from VBCLKI ↑)	t_{HKW}	<85>	13		ns
VBAHLD setup time (to VBCLKI ↑)	t_{SKW}	<84>	–6		ns
VBAHLD hold time (from VBCLKI ↑)	t_{HKW}	<85>	13		ns
VBLAST setup time (to VBCLKI ↑)	t_{SKW}	<84>	–6		ns
VBLAST hold time (from VBCLKI ↑)	t_{HKW}	<85>	13		ns
VBDC delay time (from VBCLK ↓)	t_{DKS7}	<86>		4.6	ns
VBDC hold time (from VBCLKI ↓)	t_{HKS7}	<87>	0		ns

NPB Interface Timing

NPB interface write timing



NPB interface read timing

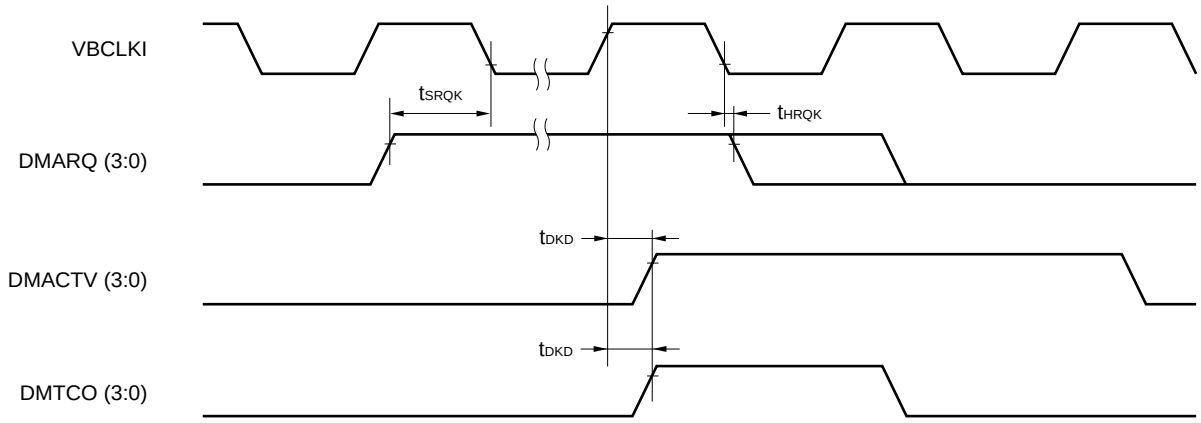


NPB Interface Timing (During Write) (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol	MIN.	MAX.	Unit
Access time	t_{ACC}	T–5		ns
Address decoding time	t_{AD}	T+0.5T–5		ns
VPSTB high-level width	t_{WSTB}	nT+T–5[Note]		ns
Write VPD setup time (to VPSTB ↑)	t_{SDSAD}	0.5T–2		ns
Write VPD hold time (from VPSTB ↓)	t_{HWD}	0		ns
VPRETR setup time (to VPSTB ↓)	t_{SRET}	10		ns
VPRETR hold time (from VPSTB ↓)	t_{HRET}	0		ns
Read VPD setup time	t_{SRD}	10		ns
Read VPD hold time	t_{HRD}	0		ns

Notes n = 1 when the operating frequency is up to 25 MHz
n = 2 when the operating frequency is 25 to 33 MHz
n = 4 when the operating frequency is 33 to 50 MHz
n = 5 when the operating frequency is 50 to 66 MHz

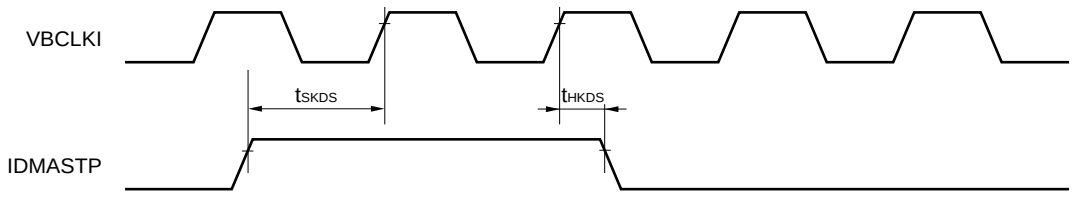
DMA Req/Ack Timing



DMA Req/Ack Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol	Synchronous		Unit
		In Relation to VBCLKI		
		MIN.	MAX.	
DMARQ setup time (to VBCLKI ↓)	t_{SRQK}	4		ns
DMARQ hold time (from VBCLKI ↓)	t_{HRQK}	3		ns
DMACTV/DMTCO delay time (from VBCLKI ↑)	t_{DKD}	12	17	ns

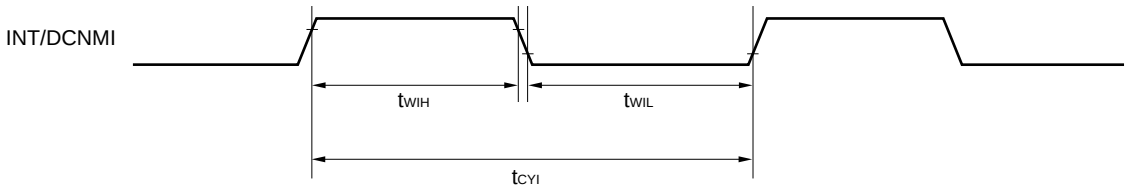
DMA Stop Request Timing



DMA Stop Request Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol	Synchronous		Unit
		In Relation to VBCLKI		
		MIN.	MAX.	
IDMASTP setup time (to VBCLKI ↑)	t_{SKDS}	–6		ns
IDMASTP hold time (from VBCLKI ↑)	t_{HKDS}	3		ns

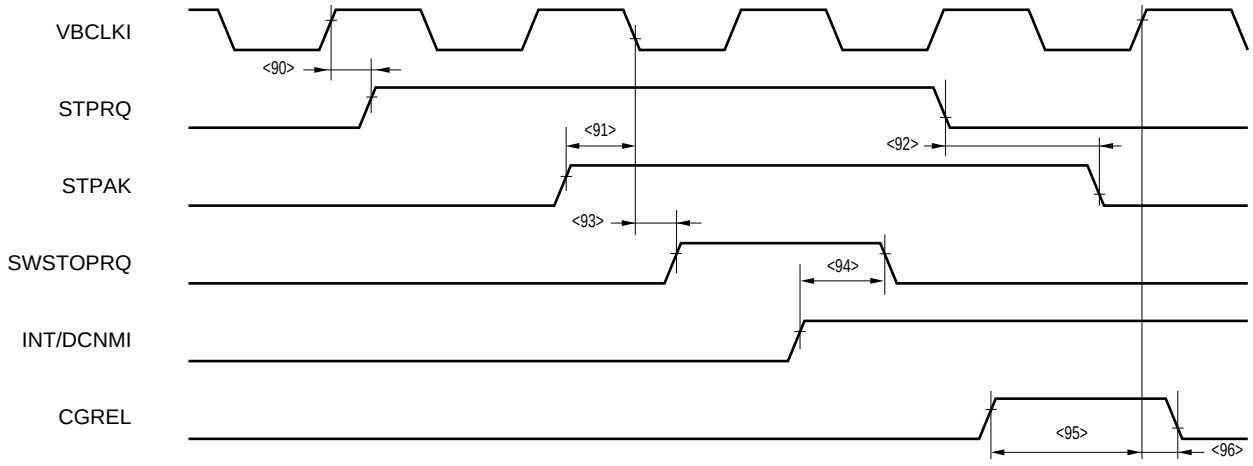
INT/NMI Request Timing



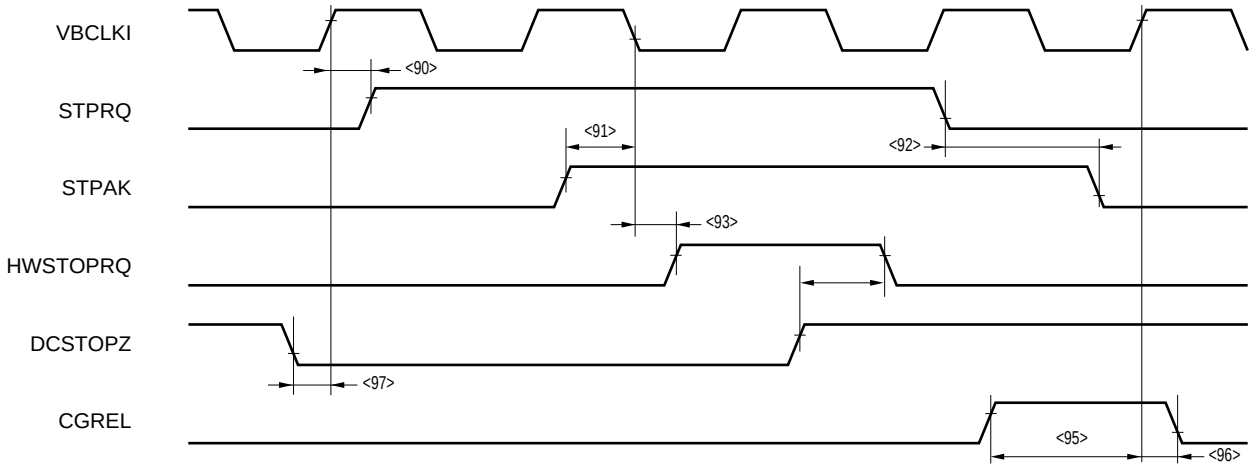
INT/NMI Request Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol	Synchronous		Unit
		MIN.	MAX.	
INT/NMI high-level width	t_{WIH}	10		ns
INT/NMI low-level width	t_{WIL}	10		ns
INT interval	t_{CYI}	3T		ns

Software Stop Timing



Hardware Stop Timing

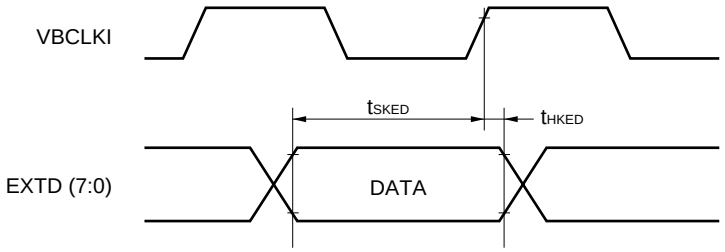


Software/Hardware Stop Timing (T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol		Asynchronous		Synchronous		Unit
			MIN.	MAX.	In Relation to VBCLKI		
					MIN.	MAX.	
STPRQ delay time (from VBCLKI ↑)	t_{DKSQ}	<90>			12	17	ns
STPAK setup time (to VBCLKI ↓)	t_{SKSA}	<91>			0		ns
STPAK hold time (from STPRQ ↓)	t_{HQSA}	<92>	7				ns
STOP status delay time (from VBCLKI ↓)	t_{DKSS}	<93>			12	17	ns
STOP release delay time	t_{DRSR}	<94>	0	15			ns
CGREL setup time (to VBCLKI ↑)	t_{SKSG}	<95>			T		ns
CGREL hold time (from VBLCKI ↑)	t_{HKSG}	<96>			13		ns
DCSTOPZ setup time (to VBCLKI ↑)	t_{SKST}	<97>			10		ns

External Probe Timing

- **Operation sampling timing write/fetch**

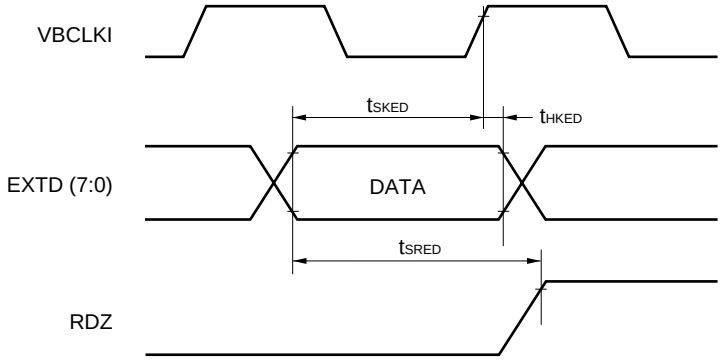


External Probe Timing (Operation Sampling Timing Write/Fetch)

(T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol	Synchronous		Unit
		In Relation to VBCLKI		
		MIN.	MAX.	
EXTD (7:0) setup time (to VBCLKI ↑)	t_{SKED}	4		ns
EXTD (7:0) hold time (from VBCLKI ↑)	t_{HKED}	0		ns

- **Operation Sampling Timing Read**



External Probe Timing (Operation Sampling Timing Read)

(T_A = 0 to 40°C, Output Pin Load Capacitance C_L = 50 pF)

Parameter	Symbol	Asynchronous		Synchronous		Unit
		MIN.	MAX.	In Relation to VBCLKI		
				MIN.	MAX.	
EXTD (7:0) setup time (to VBCLKI ↑)	t_{SKED}			4		ns
EXTD (7:0) hold time (from VBCLKI ↑)	t_{HKED}			0		ns
RDZ setup time	t_{SRED}	6				ns

APPENDIX E RESTRICTIONS

(1) The VSB bus and memory controller bus cannot be used together.

The memory controller bus (equivalent to NB85E500/NU85E502) incorporated in the emulator and the VSB bus cannot be used together.

(2) When VPSTB is not enabled, an undefined signal is output to VPRETR.

Make VPRETR input to the emulator from the UDL board Hi-Z while the VPSTB signal is low level.

(3) When using the emulator in the 64 MB mode, do not use VBA (27:26).

When using the emulator in the 64 MB mode, VBA (27:26) becomes undefined and must therefore not be used.

(4) Not all the pins of the V850E1 can be emulated by the emulator.

The emulator cannot perform emulation of the following pins because they are not included in the emulator.

- VBSEQ (2:0) pin among pins for VSB (sequential status)
- VPDACT pin among pins for NPB (active level from external address decoder)
- Pins for VFB (pins for internal ROM access)
- Pins for VDB (pins for internal RAM access)
- Pins for instruction cache
- Pins for data cache
- Pins for RCU (pins for debugging circuit)
- Pins for operation mode setting
- Pins for test mode

(5) Not all the pins of the NB85E500/NU85E502 can be emulated by the emulator.

The emulator cannot perform emulation of the following pins because they are not included in the emulator.

- Pins for NB85E connection
- Pins for initial setting
- DC0 to DC3 pins among pins for external memory connection (for data bus control)
- BENZ0 to BENZ3 pins among pins for external memory connection (byte enable)
- Pins for NB85E500/NU85E502 connection
- Pins for test mode

(6) The IORDZ, IOWRZ pins are also used as the CSZ2, CSZ5 pins.

If the memory controller contained in the emulator is used, the IORDZ, IOWRZ pins and the CSZ2, CSZ5 pins provided for the NB85E500 cannot be used together. They must be exclusively switched.

Since CSZ5/CSZ2 are set after reset, the following instruction must be executed on the program after each reset in order to use IORDZ, IOWRZ.

```
st.b 0xZZ, 0xFFFFF049
```

Remark ZZ = 00H: Use as CSZ5/CSZ2 (initial value after reset)
= 20H: Use as IORDZ/CSZ2
= 04H: Use as CSZ5/IOWRZ
= 24H: Use as IORDZ/IOWRZ

(7) Emulation memory cannot be used with an 8-bit bus size.

The standard emulation memory provided in the IE-V850E-MC-EM1-B, and the target substitution memory provided in the IE-V850E-MC-MM2 (sold separately) cannot be used with an 8-bit bus size. Use a 16-bit or 32-bit bus.

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