T-45-23-09 T-45-23-25 T-66-21-51 T-43-15
T-66-21-55 T-45-23-05 T-46-23-05 T-45-17
T-45-23-29 T-66-21-57 T-46-09-05 T-49-11
T-46-07-09 T-52-11

MOTOROLA INTEGRATED CIRCUITS

4300 Series
4000 Series

TTL

These MTTL integrated circuits provide complex functions designed for digital applications in thye medium to high-speed range.

These MTTL devices provide significant reduction in package count and increased logic per function over devices in the basic MTTL and MDTL families.

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25° C)

MAXIMUM RATINGS

Rating	Value	Unit
Supply Operating Voltage Range - V_{CC}	4.75 to 5.25	Vdc
supply Voltage	+7.0	Vdc
Input Voltage - V_{in}	+5.5	Vdc
Output Voltage - V_{out}	+5.5	Vdc
Maximum Junction Temperature	+150	°C

PACKAGING AVAILABLE (See page 49):
C - 14-LEAD DIP
D - 14-LEAD FLAT PACK
J - 24-LEAD DIP
K - 24-LEAD FLATPACK
E - 16-LEAD DIP
F - 16-LEAD FLATPACK
H - 10-LEAD FLATPACK

FUNCTION	TYPE/ PKG -55 TO +125° C	LOADING FACTOR EACH OUTPUT	PROPA-GATION DELAY ns typ	POWER DISSIPATION mW typ/pkg
Dual 4-Channel Data Selector	4300/H	10	Control Line = 18 Data Line = 11	150
BCD-to-Binary/Binary-to-BCD Number Converter	4301/C,D	Open Collector I_{OL} = 16 mA	Address Time <45 ns	300
Dual Data Distributor	4302/H	10	10.5	175
16 Bit Scratch Pad Memory Cell	4304/H	I_{OL} = 40 mA	Write mode 25 Sense mode 15	250
16 Bit Scratch Pad Memory Cell	4305/H	Open Collector I_{OL} = 20 mA	Write mode 25 Sense mode 15	250
Binary to One-of-Eight Line Decoder	4306/C,D	10	14	100
Dual Binary to One-of-Four Line Decoder	4307/E,F	10	14	125
8-Bit Parity Tree	4308/C,D	10	15 to 30	150
Dual 4 Bit Parity Tree	4310/C,D	10	9.5 to 22	125
4-Bit Shift register	4312/C,D	10	22/bit	180
Quad Type D Flip-Flop	4315/E,F	10	16	190
Programmable Module-N Decade Counter	4316/E,F	8	Clock to Q3 = 50 Clock to Bus = 35	250
Programmable Module 2, Module 5 Counters	4317/E,F	8	Clock to Q3 = 50 Clock to Bus = 35	250
Programmable Module-N Hexadecimal Counter	4318/E,F	8	Clock to Q3 = 50 Clock to Bus = 35	250
Dual Programmable Module 4 Counters	4319/E,F	8	Clock to Q3 = 50 Clock to Bus = 35	250
Dual 4-Bit Comparator (Open Collector)	4321/E,F	10	20	250
Dual 4-Bit Comparator	4322/E,F	10	20	250
4-Bit Universal Counter	4323/C,D	10	16/bit	200
Full Adder	4326/H	15/12*	25/13**	90
Full Adder	4327/H	7/6*	25/13**	90
Adder (Dependent Carry)	4328/H	15/12*	25/13**	125
Adder (Dependent Carry	4329/H	7/6*	25/13**	125

T-45-23-09 T-45-23-25 T-46-07-09
T-66-21-55 T-45-23-05 T-43-15
T-45-23-29 T-66-21-57 T-45-17
T-66-21-51 T-49-11
T-46-23-05 T-52-11

MTTL FUNCTIONS AND CHARACTERISTICS (continued)

FUNCTION	TYPE/ PKG -55 TO +125° C	LOADING FACTOR EACH OUTPUT	PROPA-GATION DELAY ns typ	POWER DISSIPATION mW typ/pkg
Adder (Independent Carry)	4330/H	15/12*	25/13**	125
Adder (Independent Carry)	4331/H	7/6*	25/31**	125
Carry Decoder	4332/H	--	Δt_{pd} = 4 decoder	20
Quad Latch (open Collector)	4335/H	7	25	140
Quad Latch	4337/H	10	25	150
Inverting/Non-Inverting One-of-Eight Decoder	4338/E,F	Open Collector I_{OL} = 20 mA	Address Time <45 ns	240
Seven Segment Character Generator	4339/E,F			240
Binary to Two-of-Eight Decoder	4340/E,F			200
Single-Error Hamming Code Detector and Generator	4341/E,F			240
Quad Predriver	4342/H	I_{OL} = 50 mA Open Collector	15	120
Dual Line Selector	4343/H	I_{OL} = 400 mA Pulsed	20	70
Non-Inverting One-of-Eight Decoder	4348E,F	Open Collector I_{OL} = 16 mA	Address Time <50 ns	240
Counter-Latch-Decoder	4350/E,F	Open Collector I_{OL} = 40 mA	f_{Tog} = 35 MHz	350
Counter-Latch Decoder	4351/E,F	Open Emitter 40 mA Sourcing Capability @ 10% Duty Cycle	f_{Tog} = 35 MHz	450
Dual Decade Counter	4352/E,F	10	f_{Tog} = 40 MHz	350
Dual Hexadecimal Counter	4353/E,F	10	f_{Tog} = 40 MHz	350
Dual Decade Up/Down Counter	4354/J,K	10	f_{Tog} = 12 MHz	600
Dual Binary Up/Down Counter	4355/J,K	10	f_{Tog} = 12 MHz	600
NBCD Adder	4356/E,F	10	30	300
Nines Complement/Zero Element	4358/C,D	10	30	200
Bus Transfer Switch	4360/E,F	10	25	350
Dual Majority Logic Gate	4362/C,D	10	z = 20 z = 11	75
64-Bit Random Access Memory	4364/E,F	Open Collector I_{OL} = 15 mA	Access Time <60 ns	384
Dual MOS-to-TTL Level Translator with Tri-state Output	4368/C,D	10	20	150

*4300/4000 Series loading specified for use with MTTLI Devices

**Add delay, Carry delay

PACKAGING INFORMATION

Per MIL-M-38510 Package Case Outline

All of Lansdale's products come in one of the following configurations. On each of the product pages in the catalog, there is a package box. The letters in that box correspond to one of the letters below. This is a guide to how the product is available.

LETTER	DESIGNATION	DESCRIPTION
A	F-1	14-LEAD FP (1/4" X 1/4")
B	F-3	14-LEAD FP (3/16" X 1/4")
C *	D-1	14-LEAD DIP (1/4" X 3/4")
D *	F-2	14-LEAD FP (1/4" X 3/8")
E *	D-2	16-LEAD DIP (1/4" X 7/8")
F *	F-5	16-LEAD FP (1/4" X 3/8")
G	A-1	8-LEAD CAN
H *	F-4	10-LEAD FP (1/4" X 1/4")
I *	A-2	10-LEAD CAN
J *	D-3	24-LEAD DIP (1/2" X 1 1/4")
K*	F-6	24-LEAD FP (3/8" X 5/8")
L	D-9	24-LEAD DIP (1/4" X 1 1/4")
M	A-3	12-LEAD CAN
P	D-4	8-LEAD DIP (1/4" X 3/8")
Q	D-5	40-LEAD DIP (9/16" X 2 1/16")
R	D-8	20-LEAD DIP (1/4" X 1 1/16")
S	F-9	20-LEAD FP (1/4" X 1/2")
V	D-6	18-LEAD DIP (1/4" X 15/16")
W	D-7	22-LEAD DIP (3/8" X 1 1/8")

FP (flat pack)
DIP (dual inline)
CAN (metal can)

* ***LANSDALE STANDARD PACKAGES***

CONTACT FACTORY FOR OTHER PACKAGE QUOTES