

Multiline Transient Voltage Surge Suppressor

MLN SurgeArray™ Suppressor

The MLN SurgeArray™ Suppressor is designed to help protect components from transient voltages that exist at the circuit board level. This device provides four independent suppressors in a single "1206" leadless chip in order to reduce part count and placement time as well as save space on printed circuit boards.

SurgeArray™ devices are intended to suppress ESD, EFT and other transients in order to protect integrated circuits or other sensitive components operating at any voltage up to 18V_{DC}. SurgeArray devices are rated to the IEC 61000-4-2 human body model ESD to help products attain EMC compliance. The array offers excellent isolation and low crosstalk between sections.

The inherent capacitance of the SurgeArray Suppressor permits it to function as a filter/suppressor, thereby replacing separate zener/capacitor combinations.

The MLN array is manufactured using the Littelfuse Multilayer technology process and is similar to the Littelfuse ML and MLE Series of discrete leadless chips.

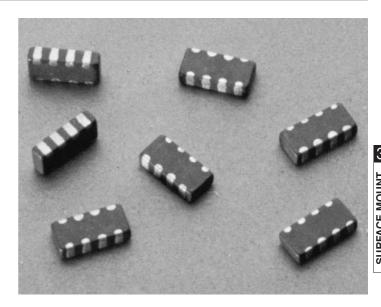
The MLN can also be provided in a Dual version. Contact Littelfuse for information

Features

- Four Individual Devices in One 1206 Chip
- ESD Rated to IEC 61000-4-2 (Level 4)
- · AC Characterized for Impedance and Capacitance
- Low Adjacent Channel Crosstalk, -55dB at 10MHz (Typ)
- · Low Leakage (6nA at 5.5V, 30nA at 15V)
- Operating Voltage up to 18V_{M(DC)}
- -55°C to 125°C Operating Temperature Range
- · Low-Profile, PCMCIA Compatible

Applications

- Data, Diagnostic I/O Ports
- Analog Signal/Sensor Lines
- Portable/Hand-Held Products
- Mobile Communications/Cellular Phones
- Computer/DSP Products
- Industrial Instruments Including Medical





Surface Mount Varistors

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Absolute Maximum Ratings For ratings of individual members of a series, see device ratings and specifications table.

Continuous:	MLN ARRAY	UNITS
Steady State Applied Voltage: DC Voltage Range (V _{M(DC)})	18	V
Operating Ambient Temperature Range (T _A)	55 to 125	°C
Storage Temperature Range (T _{STG})		°C

Device Ratings and Specifications Any Single Section

	MAX RATIN	GS (125°C)	PERFORMANCE SPECIFICATIONS (25 °C)								
PART NUMBER	MAXIMUM CONTINUOUS WORKING VOLTAGE	MAXIMUM NON- REPETITIVE SURGE CURRENT (8/20µs)	MAXIMUM CLAMPING VOLTAGE (AT NOTED 8/20μs) CURRENT	MAXIMUM NON- REPETITIVE SURGE ENERGY (10/1000μs)	ESD SUPPRESSION VOLT VOLTAGE (NOTE 1) 1m CUF		NOM VOLTA 1mA CURF	GE AT	CAPACITANCE AT 1MHz (1V p-p)		
	V _{M(DC)} I _{TM}		v _c	W_{TM}			(NOTE 3) 15kV AIR	V _{N(DC)}	V _{N(DC)}	(NOTE 4) C	
			(See Fig. 3)		Peak	Clamp	Peak	MIN	MAX	TYP	MAX
	(V)	(A)	(V)	(J)	(V)	(V)	(V)	(V)	(V)	(pF)	(pF)
V5.5MLN41206	5.5	30	15.5 at 2A	0.1	60	35	45	7.1	9.3	430	520
V9MLN41206	9	30	23 at 2A	0.1	95	50	75	11.0	16.0	250	300
V14MLN41206	14	30	30 at 2A	0.1	110	55	85	15.9	20.3	140	175
V18MLN41206	18	30	40 at 2A	0.1	165	60	100	22.0	28.0	100	125
V18MLN41206L	18	20	50 at 1A	0.05	200	95	130	25.0	35.0	45	75

NOTES:

- 1. Tested to IEC61000-4-2 Human Body Model (HBM) discharge test circuit. See explanation of Terms on page 7.
- 2. Direct discharge to device terminals (IEC preffered test method). See figure 2.
- 3. Corona discharge through air (represents actual ESD event)
- 4. Capacitance may be customized, contact Sales.

Temperature Derating

For applications exceeding 125°C ambient temperature, the peak surge current and energy ratings must be reduced as shown in Figure 1.

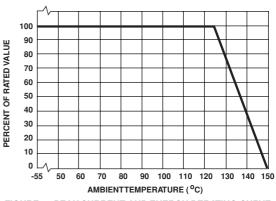
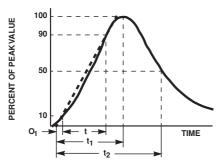


FIGURE 1. PEAK CURRENT AND ENERGY DERATING CURVE



O₁ = VIRTUAL ORIGIN OFWAVE t =TIME FROM 10% TO 90% OF PEAK $\,$ FOR AN $8/20\mu s$ CURRENT

t₁ = VIRTUAL FRONT TIME = 1.25 x t t_2 = VIRTUALTIME TO HALFVALUE (IMPULSE DURATION)

WAVEFORM: $8\mu s = t_1 = VIRTUAL FRONT$ TIME t₂ = VIRTUALTIME TO **HALFVALUE**

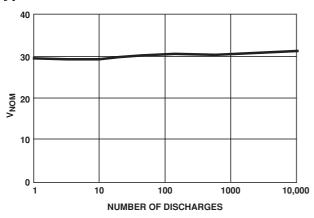
EXAMPLE:

FIGURE 2. PEAK PULSE CURRENT TEST WAVEFORM FOR CLAMPING VOLTAGE



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Typical Performance Curves Any Single Section



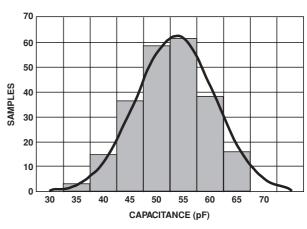


FIGURE 4. PRODUCT DISTRIBUTION OF CAPACITANCE (1MHz)

Typical Performance Curves Any Single Section

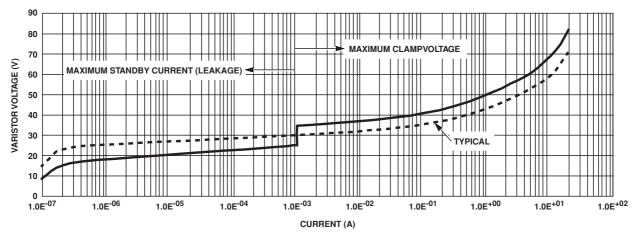


FIGURE 5. V-I CHARACTERISTICS

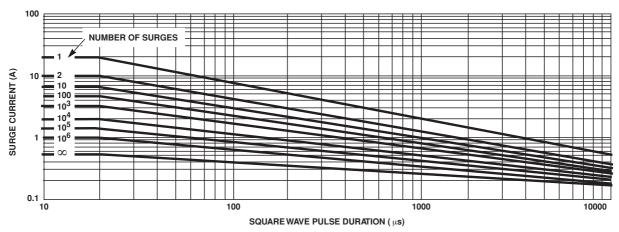


FIGURE 6. PULSE RATING FOR LONG DURATION SURGES (ANY SINGLE SECTION)



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Typical Performance Curves Any Single Section (Continued)

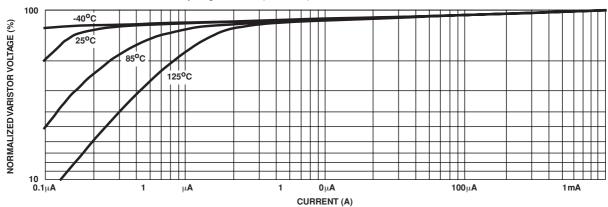


FIGURE 7. STANDBY CURRENT AT NORMALIZED VARISTOR VOLTAGE AND TEMPERATURE (ANY SINGLE SECTION)

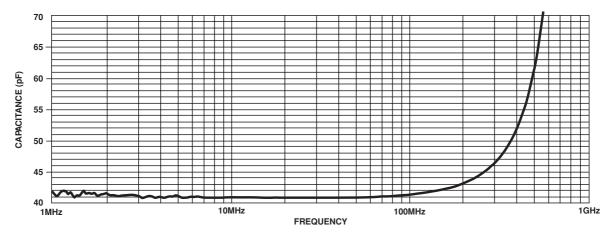


FIGURE 8. CAPACITANCE vs FREQUENCY

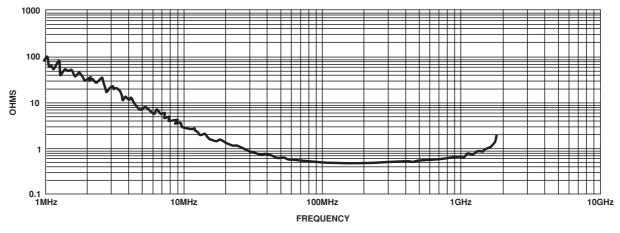


FIGURE 9. EQUIVALENT SERIES RESISTANCE

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Typical Performance Curves Any Single Section (Continued)

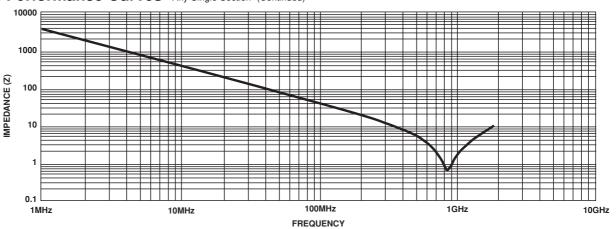


FIGURE 10. IMPEDANCE vs FREQUENCY

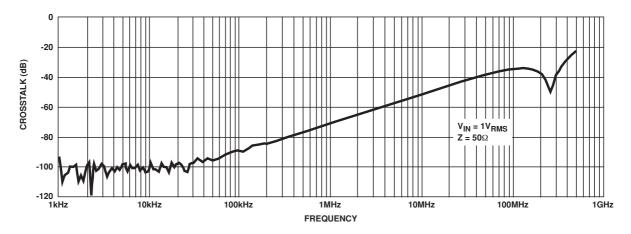


FIGURE 11. ADJACENT CHANNEL CROSSTALK

Soldering Recommendations

The principal techniques used for the soldering of components in surface mount technology are Infrared (IR) Reflow, Vapour Phase Reflow, and Wave Soldering. Typical profiles are shown in Figures 12, 13 and 14. When wave soldering, the MLN suppressor is attached to the circuit board by means of an adhesive. The assembly is then placed on a conveyor and run through the soldering process to contact the wave. With IR and Vapour Phase Reflow, the device is placed in a solder paste on the substrate. As the solder paste is heated, it reflows and solders the unit to the board.

The recommended solder for the MLN suppressor is a 62/36/2 (Sn/Pb/Ag), 60/40 (Sn/Pb), or 63/37 (Sn/Pb). Littelfuse also recommends an RMA solder flux.

Wave soldering is the most strenuous of the processes. To avoid the possibility of generating stresses due to thermal shock, a preheat stage in the soldering process is recommended, and the peak temperature of the solder process should be rigidly controlled.

When using a reflow process, care should be taken to ensure that the MLN chip is not subjected to a thermal gradient steeper than 4 degrees per second; the ideal gradient being 2 degrees per second. During the soldering process, preheating to within 100 degrees of the solders peak temperature is essential to minimize thermal shock. Examples of the soldering conditions for the MLN array of suppressors are given in the tables below.

Once the soldering process has been completed, it is still necessary to ensure that any further thermal shocks are avoided. One possible cause of thermal shock is hot printed circuit boards being removed from the solder process and subjected to cleaning solvents at room temperature. The boards must be allowed to gradually cool to less than 50°C before cleaning.



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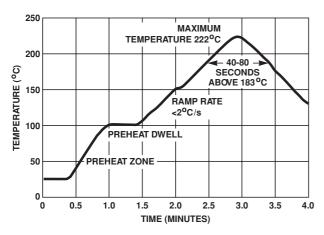


FIGURE 12. IR REFLOW SOLDER PROFILE

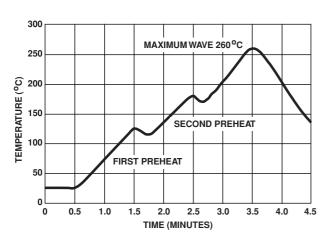


FIGURE 13. WAVE SOLDER PROFILE

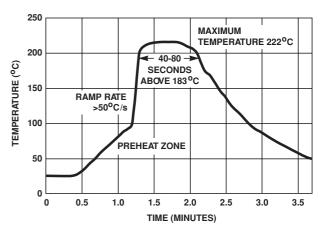


FIGURE 14. VAPOR PHASE SOLDER PROFILE

Recommended Pad Outline

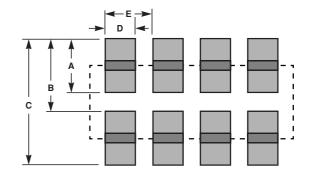
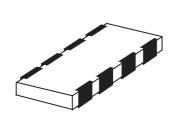
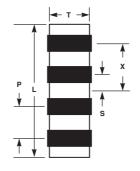


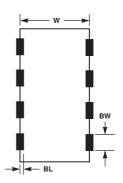
TABLE 1. PAD LAYOUT DIMENSIONS

DIMENSION	Α	В	С	D	E
Millimeters	0.89	1.65	2.54	0.46	0.79
Inches	0.035	0.065	0.100	0.018	0.030

Mechanical Dimensions







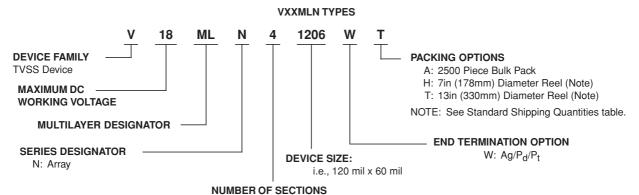
	L	W	Т	BW	BL	Р	Х	S
Inch	0.126 ±0.008	0.063 ±0.008	0.053 Max	0.016 ±0.004	0.007 +0.01/- 0.002	0.030 Ref	0.045 ±0.004	0.015 ±0.004
Millimeter	3.2 ±0.2	1.6 ±0.2	1.35 Max	0.41 ±0.1	0.18 +0.25/-0.05	0.76 Ref	1.14 ±0.1	0.38 ±0.1

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Ordering Information

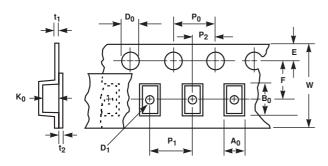


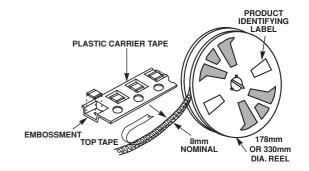
Tape and Reel Specifications

- Conforms to EIA 481, Revision A
- Can be Supplied to IEC Publication 286 3

SYMBOL	DESCRIPTION	MILLIMETERS
A ₀	Width of Cavity	Dependent on Chip Size to Minimize Rotation.
B ₀	Length of Cavity	Dependent on Chip Size to Minimize Rotation.
K ₀	Depth of Cavity	Dependent on Chip Size to Minimize Rotation.
W	Width of Tape	8 ±0.2
F	Distance Between Drive Hole Centers and Cavity Centers	3.5 ±0.5
E	Distance Between Drive Hole Centers and Tape Edge	1.75 ±0.1
P ₁	Distance Between Cavity Center	4 ±0.1
P ₂	Axial Distance Between Drive Hole Centers and Cavity Centers	2 ±0.1
P ₀	Axial Distance Between Drive Hole Centers	4 ±0.1
D ₀	Drive Hole Diameter	1.55 ±0.05
D ₁	Diameter of Cavity Piercing	1.05 ±0.05
t ₁	Embossed Tape Thickness	0.3 Max
t ₂	Top Tape Thickness	0.1 Max

NOTE: Dimensions in millimeters.





Standard Shipping Quantities

DEVICE SIZE	"13" INCH REEL ("T" OPTION)	"7" INCH REEL ("H"OPTION)	BULK PACK ("A" OPTION)
1206	10,000	2,500	2,500