Quad 8-Bit CMOS D/A Converters With Voltage Output

PM-7226A/PM-7226

FEATURES

- **No Adjustments Required, Total Error ±1/2 LSB Max Over Temperature**
- **Four Voltage Output DACs on a Single Chip**
- **Single (+5V to +15V) or Dual Supply**
- **Improved PM-7226A Version Provides**
  - **Faster 50ns Write Time, All Temperatures**
  - **Tested 5V Specifications**
  - **Reduced Reference Input Transition Current**
  - **Epi-CMOS Processing for Improved Latch-up Resistance**

APPLICATIONS

- **Automatic Test Equipment**
- **Process and Industrial Control**
- **Scientific Instrumentation**
- **Medical Instrumentation**
- **Multichannel Microprocessor Controlled**
  - **System Calibration**
  - **Op Amp Offset and Gain Adjust**
  - **Level and Threshold Setting**

GENERAL DESCRIPTION

The PM-7226 contains four 8-bit voltage output CMOS digital-to-analog converters in a single chip. Also incorporated into this chip are four input latches and interface control logic.

The four latches are under control of one write and two address signals and are fed from a common 8-bit data bus. It allows the PM-7226 to be packaged into a narrow space-saving 20-pin, 300 mil DIP. All digital inputs are TTL/CMOS (5V) compatible. Also, each DAC's input latch is addressable for easy microprocessor interface. The on-board output amplifier can each drive up to 5mA from either a single or dual supply. *Continued*

ORDERING INFORMATION †

TOTAL UNADJUSTED ERROR	MILITARY TEMPERATURE	EXTENDED INDUSTRIAL TEMPERATURE	COMMERCIAL TEMPERATURE
±1/2 LSB	PM7226AR	PM7226ER	PM7226GP
±1 LSB	PM7226BR	PM7226FR	—
±1 LSB	PM7226BRC/883	PM7226FPC	—
±1 LSB	—	PM7226FS	—
±1 LSB	—	PM7226FP	—
±1 LSB	—	PM7226AFR	—
±1 LSB	—	PM7226AFP	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

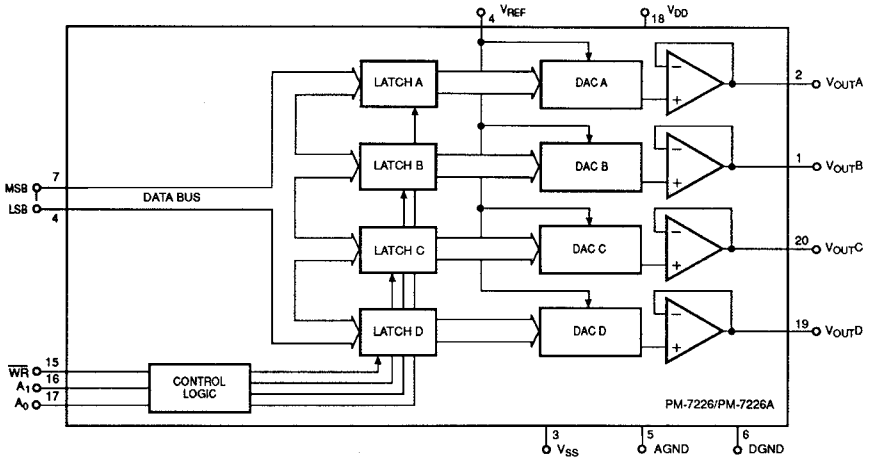
† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7226AR PM7226BR	— AD7226TQ	MIL
PM7226ER PM7226FR	— AD7226BQ	IND
PM7226GP PM7226FPC PM7226FP	— AD7226KP AD7226KN	COM

FUNCTIONAL DIAGRAM

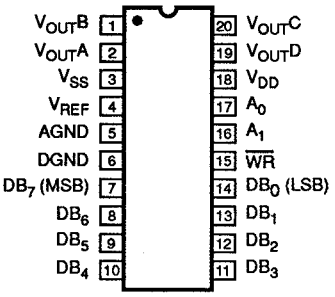


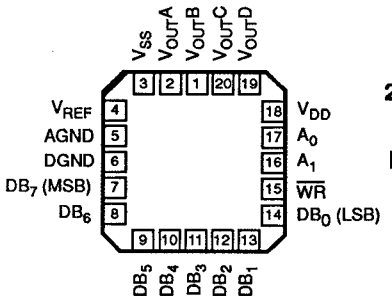
REV. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

PIN CONNECTIONS

20-PIN HERMETIC DIP
(R-Suffix)
20-PIN EPOXY DIP
(P-Suffix)
20-PIN SOL
(S-Suffix)





PM-7226FPC
20-CONTACT PLCC
(PC-Suffix)

PM-7226BRC/883C
20-CONTACT LCC
(RC-Suffix)

GENERAL DESCRIPTION *Continued*

The PM-7226's compact size, low power, and economical cost per channel, make it attractive for applications requiring multiple D/A converters without sacrificing circuit board space. System reliability is also increased due to reduced part count. For higher channel output systems the PM-7226A can be connected with the DAC-8426 to provide a complete eight or higher channel output D/A system with an internal +10V reference in only two IC packages.

PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the PM-7226's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

The PM-7226 and the PM-7226A are improved replacements for the AD7226.

For military temperature range PM-7226A, contact factory for 883 data sheet.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} –4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise specified. T_A = –55°C to +125°C apply for PM-7226AR/BR; T_A = –40°C to +85°C apply for PM-7226ER/FR/FP/FPC/FS/AFR/AFP; T_A = 0°C to +70°C apply for PM-7226GP. All specifications apply for DACs A, B, C, and D.

PARAMETER	SYMBOL	CONDITIONS	PM-7226A/PM-7226 MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 1)	TUE	PM-7226A/E/G (Note 7)	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Relative Accuracy	INL	PM-7226A/E/G	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	PM-7226A/E/G	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Full-Scale Error	G_{FSE}	PM-7226A/E/G	–	–	±1/2	LSB
		PM-7226B/F/H/AF	–	–	±1	
Full-Scale Temperature Coefficient (Note 4)	TCG_{FS}		–	1	±20	ppm/°C
Zero Code Error	V_{ZSE}	DUAL SUPPLY				mV
		PM-7226A/E/G	–	–	±5	
		PM-7226B/F/H/AF	–	–	±20	
		SINGLE SUPPLY				
		PM-7226A/E/G	–	–	±10	
		PM-7226B/F/H/AF	–	–	±20	
Zero Code Error Temperature Coefficient (Note 4)	TCV_{ZS}	DUAL SUPPLY ONLY	–	±10	–	µV/°C

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} –4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise specified. T_A = –55°C to +125°C apply for PM-7226AR/BR; T_A = –40°C to +85°C apply for PM-7226ER/FR/FP/FPC/FS/AFR/AFP; T_A = 0°C to +70°C apply for PM-7226GP. All specifications apply for DACs A, B, C, and D. *Continued*

			PM-7226A/PM-7226			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
REFERENCE INPUT						
Input Voltage Range (Note 3)	V_{REF}		2	–	(V_{DD} –4V)	V
Input Resistance	R_{REF}		2	4	–	kΩ
Input Capacitance (Note 4)	C_{REF}	Digital Inputs = all 0s Digital Inputs = all 1s	65 –	– –	– 300	pF
DIGITAL INPUTS						
Digital Inputs High	V_{INH}		2.4	–	–	V
Digital Inputs Low	V_{INL}		–	–	0.8	V
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	–	0.1	±1	µA
Digital Input Capacitance (Note 4)	C_{IN}		–	4	8	pF
Input Coding				BINARY		
POWER SUPPLIES						
Positive Supply Current (Note 6)	I_{DD}		–	6	12	mA
Negative Supply Current (Note 6)	I_{SS}	DUAL SUPPLY ONLY, V_{SS} = –5V	–	4	10	mA
Power Dissipation	P_{DISS}	V_{DD} = +12V, V_{SS} = 0V	–	72	144	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%	–	–	0.01	%/%
DYNAMIC PERFORMANCE						
V_{OUT} Slew Rate (Note 4)	SR		2.5	4	–	V/µs
V_{OUT} Settling Time (Positive or Negative) (Notes 4, 5)	t_s		–	3	5	µs
Digital Crosstalk (Note 4)	Q		–	10	–	nVs
Minimum Load Resistance	$R_{L(MIN)}$	V_{OUT} = +10V	2	–	–	kΩ
SWITCHING CHARACTERISTICS (Note 4)						
Address to Write Set-Up Time	t_{AS}		0	–	–	ns
Address to Write Hold Time	t_{AH}		0	–	–	ns
Data Valid to Write Set-Up Time	t_{DS}	PM-7226 PM-7226A	90 70	– –	– –	ns
Data Valid to Write Hold Time	t_{DH}		10	–	–	ns
Write Pulse Width	t_{WR}	PM-7226 PM-7226A	90 50	– –	– –	ns

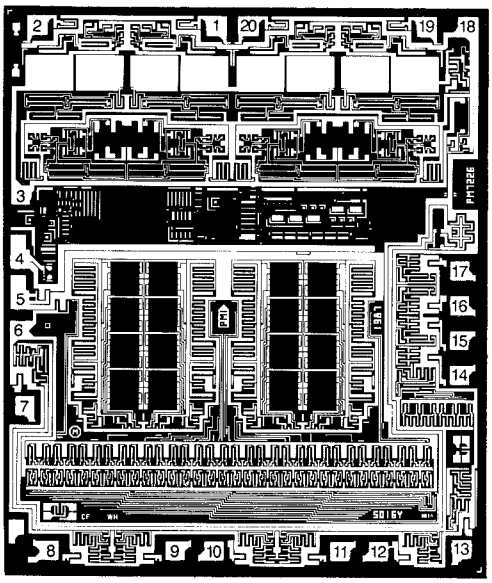
NOTES:

1. Includes Full-Scale Error, Relative Accuracy, and Zero Code Error.
2. All devices guaranteed monotonic over the full operating temperature range.
3. V_{DD} –4V is the maximum reference voltage for the above specifications.
4. Guaranteed by design and not subject to production test.
5. V_{REF} = +10V; to where output settles to 1/2 LSB.
6. V_{IN} = V_{INL} or V_{INH}; outputs unloaded.
7. V_{DD} = +15V only.

ELECTRICAL CHARACTERISTICS : +5V Supply Operation at V_{DD} = +5V ±5%, V_{SS} = 0 or –5V, AGND = DGND = 0V, V_{REF} = +1.25V, unless otherwise noted. T_A = –40°C to +85°C applies for PM-7226AFR/FP. All specifications apply for DACs A, B, C, and D.

			PM-7226A ONLY			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution	N		8	–	–	Bits
Differential Nonlinearity	DNL	Applies to Codes 2 through 255	–	–	±1	LSB
Full-Scale Error	G_{FSE}		–	–	±4	LSB
Zero Code Error	V_{ZSE}		–	–	30	mV
Reference Input Voltage Range	V_{REF}	$V_{OUT} < (V_{DD} - 3.5V)$	1.2	1.25	1.3	V
Reference Input Resistance	R_{REF}	Digital Inputs all 1s	2	–	–	kΩ
Reference Input Capacitance	C_{REF}	Digital Inputs all 1s	–	–	300	pF
DIGITAL INPUTS (All specifications the same as for V_{DD} = +12V supplies)						
DYNAMIC PERFORMANCE (All specifications are the same as for V_{DD} = +12V supplies.)						
Positive Supply Current	I_{DD}		–	3.5	12	mA
Negative Supply Current	I_{SS}	V_{SS} = –5V only	–	3.5	10	mA
Power Dissipation	P_{DISS}	V_{SS} = 0V	–	17.5	60	mW
SWITCHING CHARACTERISTICS						
Address-to-Write Setup Time	t_{AS}		0	–	–	ns
Address-to-Write Hold Time	t_{AH}		20	–	–	ns
Data Valid-to-Write Setup Time	t_{DS}		180	–	–	ns
Data Valid-to-Write Hold Time	t_{DS}		20	–	–	ns
Write Pulse Width	t_{WR}		120	–	–	ns

DICE CHARACTERISTICS



DIE SIZE 0.129 x 0.152 inch, 19,608 sq. mils
(3.28 x 3.86 mm, 12.65 sq. mm)

1. $V_{OUT}B$
2. $V_{OUT}A$
3. V_{SS}
4. V_{REF}
5. AGND
6. DGND
7. DB_7 (MSB)
8. DB_6
9. DB_5
10. DB_4
11. DB_3
12. DB_2
13. DB_1
14. DB_0 (LSB)
15. $\overline{WR}$
16. A_1
17. A_0
18. V_{DD}
19. $V_{OUT}D$
20. $V_{OUT}C$

Substrate (die backside) is internally connected to V_{DD}.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.
WAFER TEST LIMITS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} −4V). SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; unless otherwise specified. T_A = +25°C. All specifications apply for DACs A, B, C, D.

PARAMETER	SYMBOL	CONDITIONS	PM-7226BGC LIMITS	UNITS
Total Unadjusted Error	TUE	V_{DD} = +15V	±1	LSB MAX
Relative Accuracy	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Full-Scale Error	G_{FSE}		±1	LSB MAX
Zero Code Error	V_{ZSE}		±20	mV MSX
Reference Input Voltage Range	V_{REF}		2 to (V_{DD} −4V)	V
Reference Input Resistance	R_{IN}		2	kΩ MIN
Digital Inputs High	V_{INH}		2.4	V MIN
Digital Inputs Low	V_{INL}		0.8	V MAX
Digital Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	µA MAX
Positive Supply Current	I_{DD}	V_{IN} = V_{INL} or V_{INH}	12	mA MAX
Negative Supply Current	I_{SS}	V_{IN} = V_{INL} or I_{INH}, V_{SS} = −5V	10	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

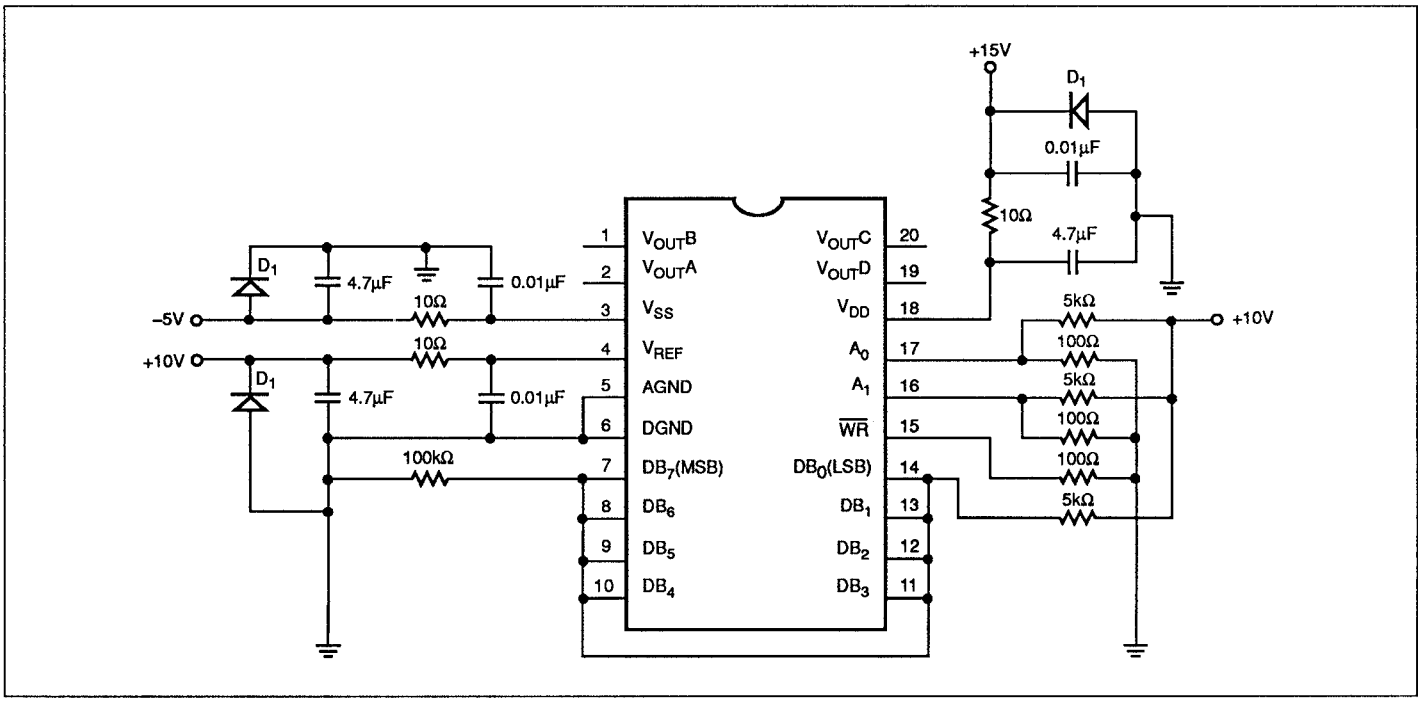
V_{DD} to AGND or DGND ..... –0.3V, +17V
V_{SS} to AGND or DGND ..... –7V, V_{DD}
V_{DD} to V_{SS} ..... –0.3V, +24V
AGND or DGND ..... –0.3V, V_{DD}
Digital Input Voltage to DGND ..... –0.3V, V_{DD} + 0.3V
V_{REF} to AGND ..... –0.3V, V_{DD}
V_{OUT} to AGND (Note 1)
Operating Temperature
AR/BR Versions ..... –55°C to +125°C
ER/FR/FP/FPC/FS/AFR/AFP Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 5)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
20-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTES:

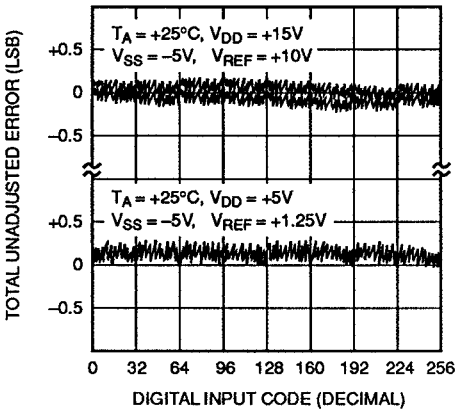
1. Outputs may be shortened to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50mA.
2. The digital inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep device in conductive foam at all times until ready for use.
3. Use proper antistatic handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
5. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

BURN-IN CIRCUIT

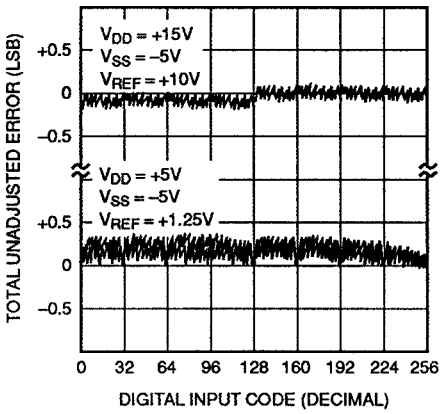


TYPICAL PERFORMANCE CHARACTERISTICS

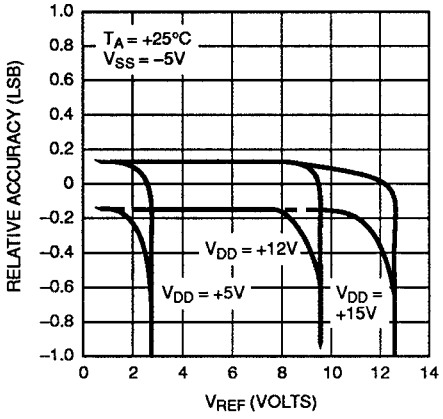
CHANNEL-TO-CHANNEL MATCHING (DACs A, B, C, D SUPERIMPOSED)



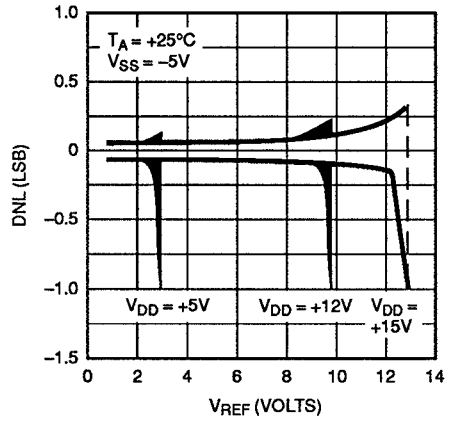
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT T_A = –55°C, +25°C, +125°C (ALL SUPERIMPOSED)



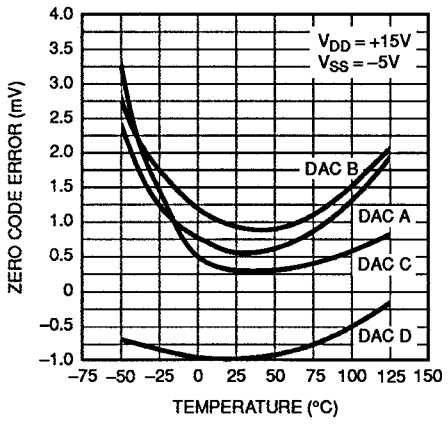
RELATIVE ACCURACY vs V_{REF}



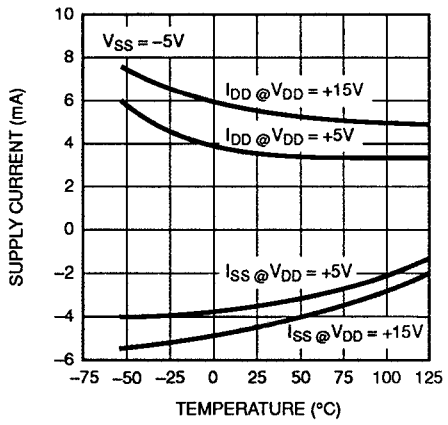
DIFFERENTIAL NONLINEARITY vs V_{REF}



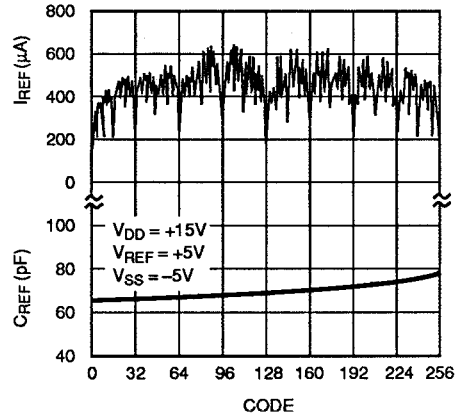
ZERO CODE ERROR vs TEMPERATURE



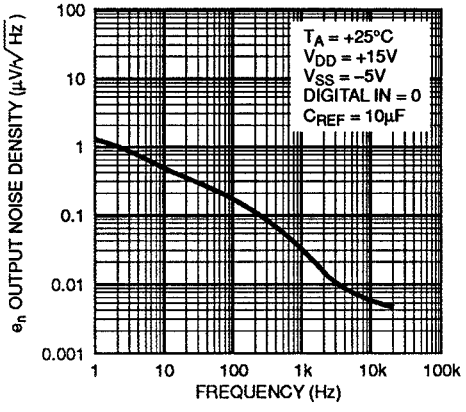
SUPPLY CURRENT vs TEMPERATURE



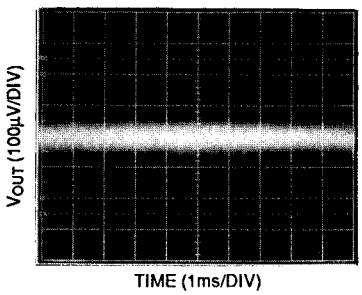
REFERENCE INPUT CURRENT AND CAPACITANCE vs CODE



V_{OUT} NOISE DENSITY vs FREQUENCY



BROADBAND NOISE (DC TO 200kHz)



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR

This specification includes full-scale error, relative accuracy, and zero code error. Ideal full-scale output is V_{REF} – 1 LSB, and 1 LSB is V_{REF} x (2^{-n}).

DIGITAL CROSSTALK

Digital crosstalk is the signal coupled to the output of one DAC due to a change in digital input code from other DACs. It is specified in nano-volt-seconds and measured with V_{REF} = 0V.

Refer to PMI's Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The PM-7226 contains four output amplifiers, four highly stable thin-film, R-2R resistor ladder networks, four input data latches, and interface control logic. Also included are 32 NMOS single-pole, double-throw switches. These switches select either V_{REF} or AGND and are controlled by the digital input code.

Figure 1 shows a simplified circuit for the R-2R ladder network. It is shown employed in the voltage mode configuration and connected to an amplifier. The advantages gained in operating the ladder in the voltage mode are twofold: it allows the DAC to be operated with a single supply, and the ladder resistance/capacitance modulation encountered in the current mode configuration are eliminated. The modulation (caused by the varying digital code) is now presented to the low impedance reference voltage source (most voltage reference output impedances are low enough so that its output voltage will not be affected by the varying digital code). The amplifier's input terminal now "sees" a constant resistance/capacitance, thus the output offset voltage modulation is eliminated. Also, digital glitches will not feed through the switch capacitance to the output; instead, it will be absorbed by the low output impedance of the external reference source, thus, resulting in a "cleaner" output voltage.

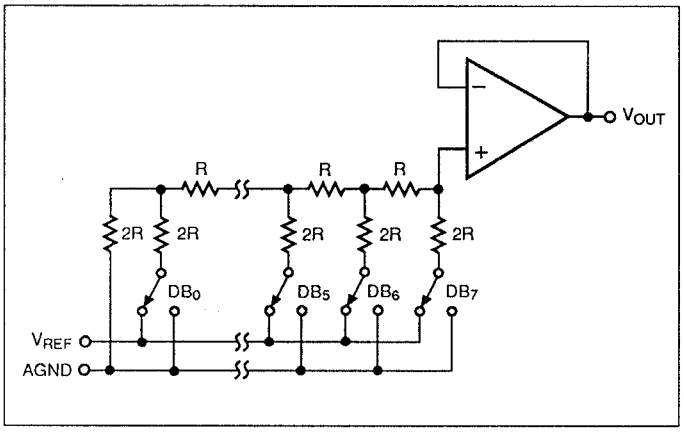


FIGURE 1: *Simplified circuit configuration for one DAC. (Switches are shown for all "1s" on the digital inputs.)*

Note in Figure 1 that the amplifier is configured to operate as a buffer amplifier; no signal inversion takes place from input to output (V_{REF} to V_{OUT}). Also note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the application section on AGND Biasing.

For proper operation, V_{REF} maximum should be limited to V_{DD} minus 4 volts. This means that in order to operate the DAC with +10V at the reference input terminal, V_{DD} must be at least +14V.

The PM-7226's reference input terminal is common to the four DACs. This puts each R-2R ladder resistance in parallel and its resistance can range from 2kΩ to infinity; the value depends on the digital input code. The capacitance at this node also varies from 65pF to 300pF, and is code dependent. The typical performance characteristic curves show the variation in reference input resistance (I_{REF} @ V_{REF} = 5V) and C_{REF} versus code. The PM-7226A offers improved transient I_{REF} current as shown in Figure 2 which minimizes loading on the external reference circuitry.

The voltage output equation for each DAC is given by:

$V_{OUT} = V_{REF} \times D/256$

where D is the digital input code integer number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

Each R-2R resistor ladder network has a typical resistance of 10kΩ; a 100kΩ load would cause the gain error to rise to 23 LSB. Therefore, in order to drive a 2kΩ load, the R-2R ladder was buffered with a stable CMOS amplifier configured to operate in the unity-gain mode. The amplifier can drive 10 volts across a 2kΩ load delivering 5mA, and can easily drive a 3300pF capacitive load. The PM-7226's output can also withstand an indefinite short circuit to AGND (typical short-circuit current to AGND is 50mA). The output may also be shorted to any voltage between V_{DD} and V_{SS}; however, care must be taken to not exceed the device maximum power dissipation.

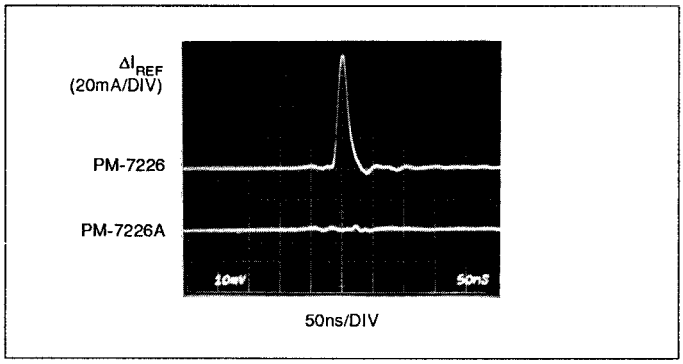


FIGURE 2: *Switching Transient Input Reference Current*

The amplifier's output stage uses an intrinsic NPN bipolar transistor. This transistor provides a low impedance, high output current capability using a small part of the chip area. The transistor is derived from the P–well and the substrate. The emitter of this NPN transistor is loaded with a 450µA NMOS current source referenced to V_{SS}. This allows 450µA to be sunk to the negative supply allowing the amplifier's output to go directly to ground.

A simplified circuit of the output amplifier is shown in Figure 3. Note how the current source is connected between the parasitic NPN output transistor's emitter and V_{SS}. Figure 4 shows a typical plot of the DAC's current sink capability versus output voltage; note that it is for a dual and single supply operation. Let's take a closer look at what happens to its behavior by referring to Figure 4.

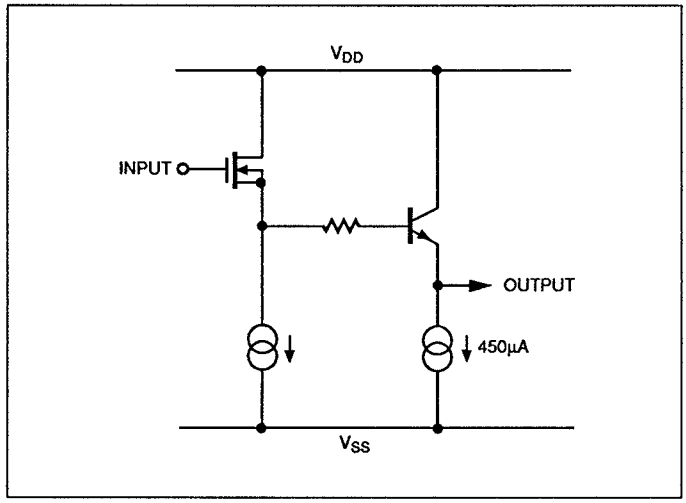


FIGURE 3: *Amplifier Output Stage*

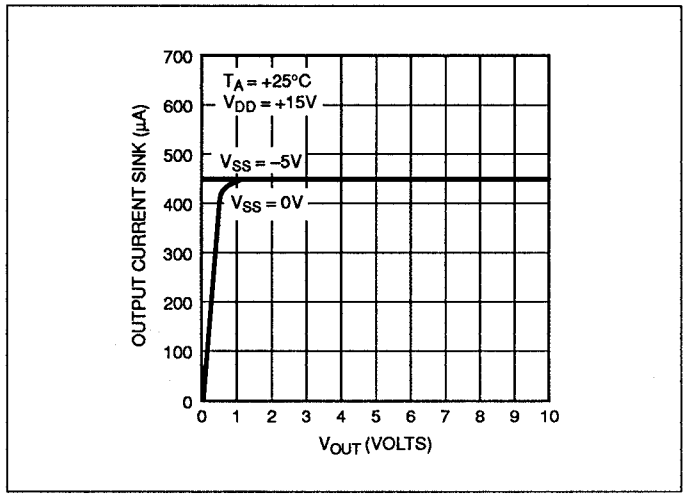


FIGURE 4: *DAC Output Current Sink*

With a dual supply, the current source is still in its high impedance (saturation) state when the output is at 0V. Therefore, the current source has 5V of bias in dual supply operation. When V_{SS} = 0V, however, the current sink capability is reduced as the output voltage approaches 0V; the current source is coming out of its saturation region and starts appearing resistive.

The amplifier's current limiting and buffering abilities are achieved by using an NMOS transistor and a series resistor. The transistor is configured as a source follower and is driving the resistor and NPN output transistor. This is also shown in Figure 3.

Figure 5 displays the combined amplifier source and sink capability to the point of current limiting. This plot was made with the digital inputs set at zero code. Note that the maximum source current available is dependent on the V_{DD} supply voltage.

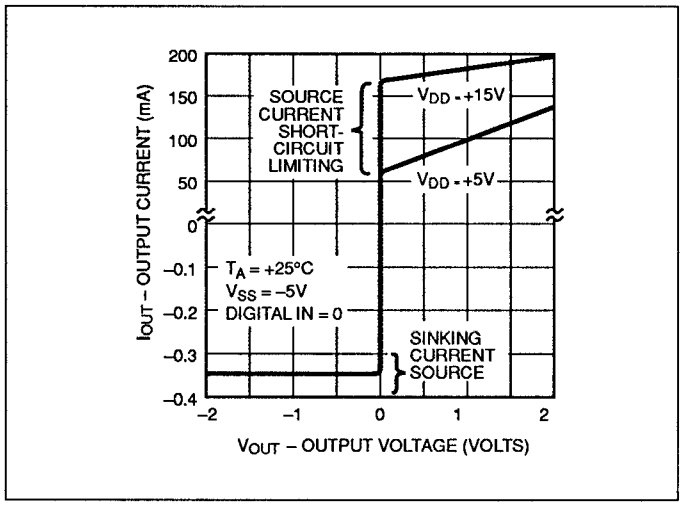


FIGURE 5: *Output Sink-Source Current vs. Voltage*

The amplifier's internal gain stages were designed so that they maintain good gain over its common-mode range; the objective was to maintain good offset performance over the specified voltage range. The amplifier's offset voltage is laser-trimmed during the manufacturing process; this eliminates offset trimming by the user in most applications. The effect of amplifier offset is included in the data sheet under "total unadjusted error" specification.

DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed such that TTL and CMOS (5V) input levels are converted into internal CMOS logic levels; they are used to drive the internal circuitry. A simple 5V regulator is used to ensure the high-speed timing.

The PM-7226's digital inputs are TTL and CMOS (5V) compatible between the V_{DD} range of +11.4V to +16.5V. The inputs are protected from electrostatic discharge and build-up with two internal distributed diodes; they are connected from V_{DD} and DGND to each CMOS input gate. Each input has a typical input current of less than 1nA. A simplified input protection scheme is shown in Figure 6.

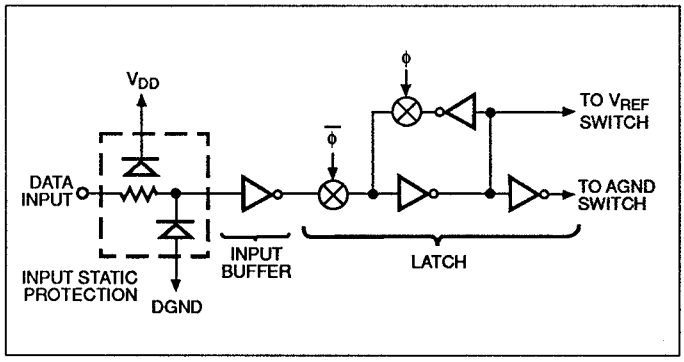


FIGURE 6: *One Digital Input Structure*

Figure 6 also shows an equivalent logic circuit for one digital input structure. This logic circuit drives the ladder switches shown in Figure 7; it also drives the control logic circuitry. The digital controls ø and $\overline{ø}$ shown are internally generated from the external $\overline{WR}$, A_1, and A_0 signals. The logic combination of A_0 and A_1 decide which DAC is selected.

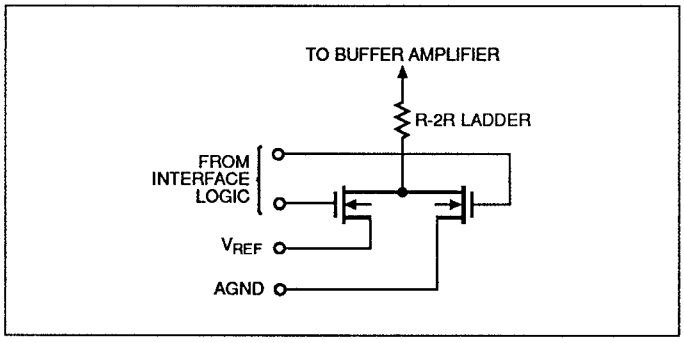


FIGURE 7: *Simplified N-Channel Voltage Steering Switches*

INTERFACE CONTROL LOGIC SECTION

Figure 8 shows the PM-7226's input control logic, and Table 1 the DAC control table. The address lines A_0 and A_1 determines which DAC will accept the input data. The $\overline{WR}$ input determines whether the selected DAC is transparent (output follows the input), latched, or no operation.

Figure 9 shows the PM-7226's write timing diagram. It shows that the selected DAC is transparent when the $\overline{WR}$ signal is low. Some bus systems do not always have data valid for the entire period during which the $\overline{WR}$ signal is low. This allows invalid data to briefly appear at the DAC's digital inputs and cause unwanted glitches at the output. Retiming the write pulse ($\overline{WR}$) so that it only occurs when data is valid will eliminate this problem.

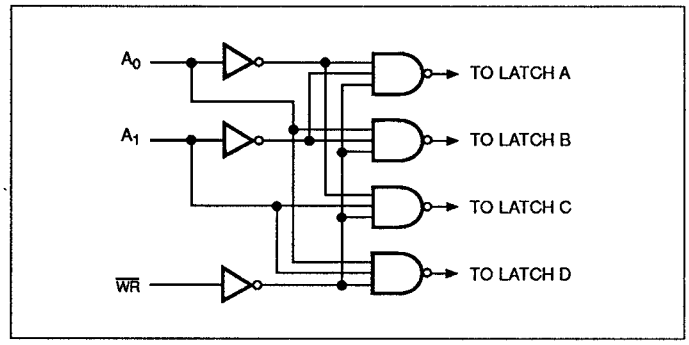


FIGURE 8: *Input Control Logic*

TABLE 1: DAC Control Table

LOGIC CONTROL $\overline{WR}$	A_1	A_0	PM-7226 OPERATION
			No Operation
H	X	X	Device Not Selected
L	L	L	DAC A Transparent
↓	L	L	DAC A Latched
L	L	H	DAC B Transparent
↓	L	H	DAC B Latched
L	H	L	DAC C Transparent
↓	H	L	DAC C Latched
L	H	H	DAC D Transparent
↓	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

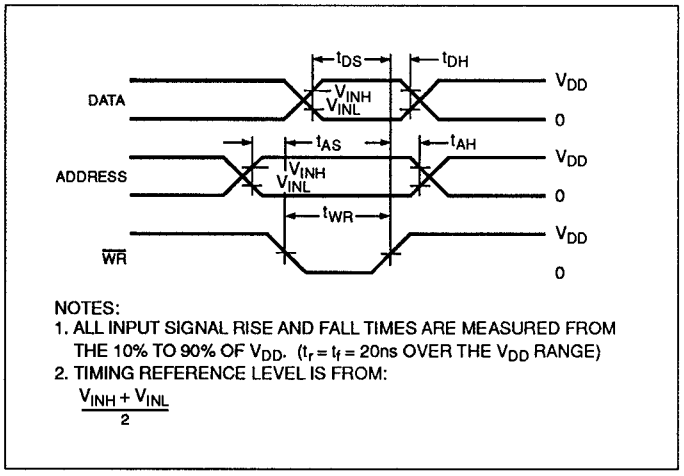


FIGURE 9: *Simplified circuit configuration for one DAC. (Switches are shown for all "1s" on the digital inputs.)*

APPLICATIONS INFORMATION

POWER SUPPLY

The PM-7226 data sheet is specified with dual and single power supply conditions. The dual supply specifications are specified with a positive supply (V_{DD}) range of +11.4V to +16.5V, and a negative supply (V_{SS}) of –5V. The specified reference voltage (V_{REF}) under these conditions range from +2V to V_{SS} –4V. For those applications requiring +10V at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits.

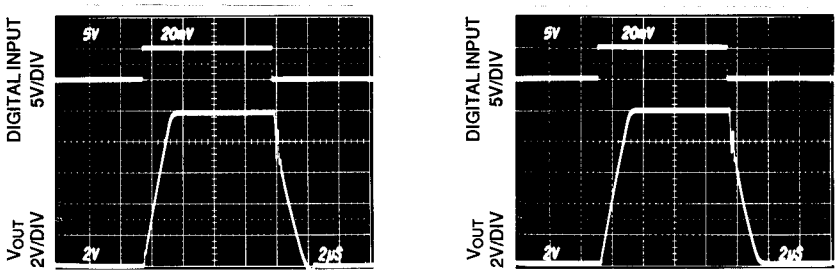
The specified V_{REF} for the single supply specifications is +10V. The V_{REF} voltage range for both dual and single power supply applications must be observed if the PM-7226's multiplying capabilities are to be preserved.

Although the PM-7226 can operate with either a single or dual power supply, improved zero-code error can be obtained by using dual supplies.

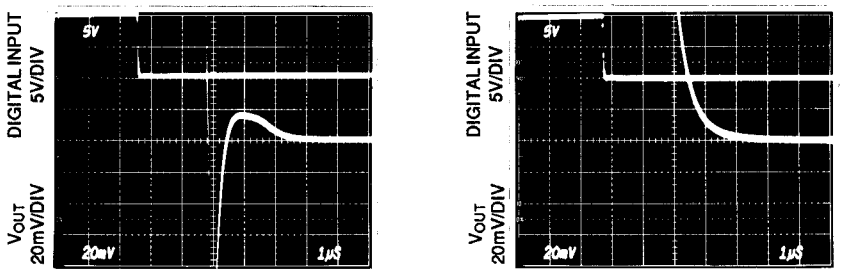
DYNAMIC PERFORMANCE

The PM-7226's settling time is limited by the internal amplifier's slew rate as shown in Figure 10. Depicted is the dynamic response for a positive full-scale output voltage swing. Figure 10c shows the expanded view with no evidence of signal overshoot or ringing; note that the typical settling time is 1.85µs. An expanded view of the negative full-scale output voltage swing is shown in Figure 10b. It also shows overshoot at a minimum, and the typical settling time is 2.6µs.

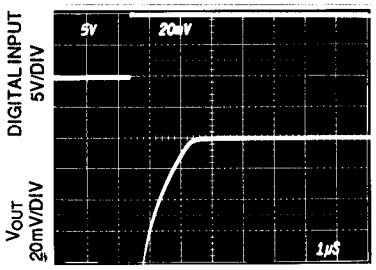
a) LARGE SIGNAL



b) SETTLING TIME RESPONSE (NEGATIVE TRANSITION)



c) SETTLING TIME RESPONSE (POSITIVE TRANSITION)



TEST CONDITIONS, ALL PHOTOS:
V_{DD} = +15V
V_{REF} = +10V
R_L = 2kΩ
DIGITAL INPUT SEQUENCE 0,255, 0

FIGURE 10: *Dynamic Response*

AGND BIASING

Some applications may require the DAC's output voltage level to be offset above ground. This is easily accomplished with the PM-7226; the desired DC offset voltage can be applied to the AGND pin. Raising AGND above DGND affects all four DACs because AGND is common to them. The digital input voltage levels are not affected. Figure 11 shows the circuit configuration and Figure 12 shows the relative accuracy with AGND biased at 0V, +2V, and +5V. The graph shows both a dual and single supply operation with V_{DD} at +15V. It is important to remember that other parameters degrade more pronouncedly than relative accuracy. Note, V_{DD} and V_{SS} must be referenced to DGND.

The DAC's output voltage expression under this condition is:
V_{OUT} = AGND bias + V_{IN} x D/256

where AGND bias is the voltage level above DGND and D is the digital input code integer number that is between 0 and 255.

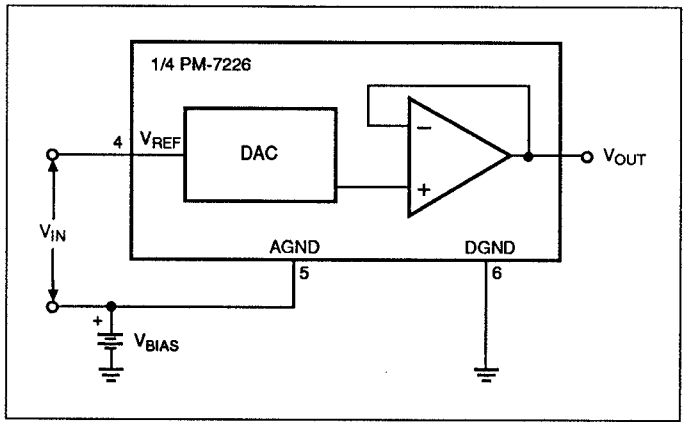


FIGURE 11: *AGND Biasing Scheme*

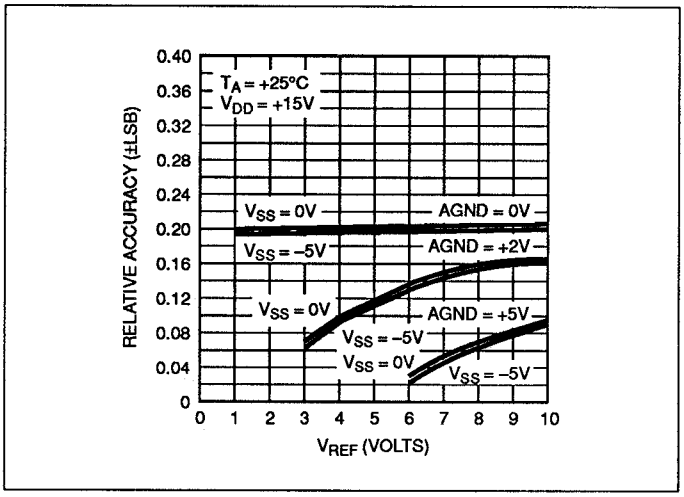


FIGURE 12: *Relative Accuracy vs. V_{REF} (AGND = 0V, +2V, +5V)*

MULTIPLYING OPERATION

Good multiplying capabilities are realized with the PM-7226 if the reference signal level is kept within +2V and V_{DD} –4V. The maximum input signal level is +12.5V for a V_{DD} supply voltage of +16.5V; however, it is recommended that V_{DD} = +15V ±5% and the AC voltage swing vary from +2V to +11V. The signal must be AC coupled and biased up with a voltage divider as shown in Figure 13. A buffer amplifier should be used to ensure that the DAC's V_{REF} impedance (the R-2R ladder input resistance varies from 2kΩ to infinity) does not load the resistor divider.

The V_{REF} small-signal frequency response (–3dB bandwidth) for the PM-7226 is typically 1.5MHz. Its small-signal harmonic distortion is less than –57dB at 1kHz and –55dB at 100kHz.

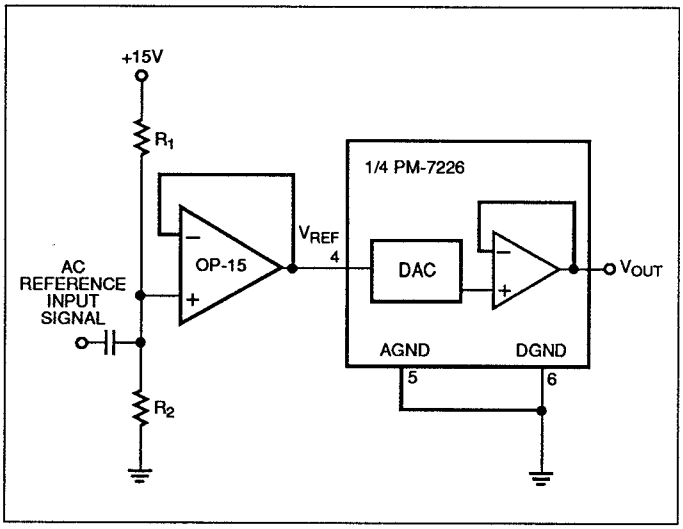


FIGURE 13: *AC Signal Input Scheme*

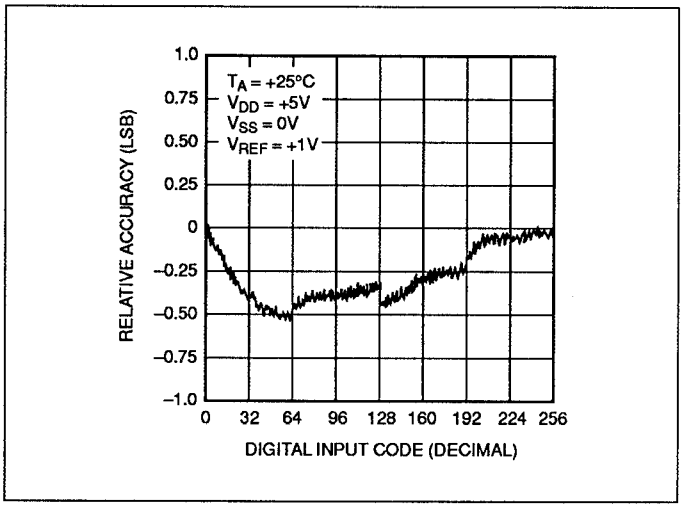


FIGURE 14: *Relative Accuracy with Single +5V Operation*

+5V SINGLE SUPPLY OPERATION

Operation of the improved PM-7226A at a +5V V_{DD} is guaranteed in the separate specification table. Linearity performance specified by DNL is still maintained within ±1 LSB maximum. DNL and offset performance is improved with a –5V supply, see graph in Typical Performance Characteristics section. Input reference voltages must be limited to 1.3V maximum with V_{DD} = 5V. Microprocessor interface timing is slower, but guaranteed to the values provided.

GENERAL GROUND MANAGEMENT

Ground management implies the placement of a system's analog and digital ground currents. Analog and digital ground returns are a source of system errors and must be addressed. Remember, the analog signal is only as good as the integrity of its analog ground.

Different ground management techniques are used depending on the size and type of the overall system. Proper grounding techniques require tying the analog and digital grounds together at the DAC's socket, and each ground return line be brought out separately to their respective power supply grounds. Tying the grounds together at the device socket and at the power supplies, or at more than one location, can create ground loops. This causes noisy digital ground currents to flow through the analog ground paths destroying the analog's ground integrity. Voltage differences of millivolts (and hundreds of millivolts in some systems) can be found in these ground paths.

Other sources of system errors can be introduced by the product of ground noise currents and ground bus impedances. Using large conductors or ground planes between the converter and power supplies will minimize the ground impedances and thus, reduce system errors.

If system requirements dictate the use of common return lines to the power supplies for both the analog and digital grounds, the converter should then be placed as close to the power supplies as possible.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors are important to suppress oscillations and noise transients from entering the system. Noise transients are generated from digital switching or switching power supplies; and oscillations on the power supply lines are caused by lead inductances combined with stray capacitance. These transients and oscillations can also cause system errors.

Bypassing the PM-7226 at the socket with only high frequency decoupling capacitors may not remove these oscillations. An LC tank circuit can be formed by the stray power lead inductance and capacitance. These reactive components can allow oscillations to occur during a digital current step. It is necessary, then, to remove or lower the tank's resonant frequency. The easiest method is to parallel the high frequency decoupling capacitor with a low frequency capacitor.

The high frequency decoupling capacitors should be ceramic and in the range of 0.01µF; the low frequency decoupling capacitors should be tantalum and between 1 to 10µF as close as possible to the device socket.

BASIC APPLICATIONS

UNIPOLAR OPERATION

Figure 15 shows the PM-7226 configured in the unipolar mode of operation; the analog output voltage is of a single positive polarity only. Table 2 shows the code for this mode of operation.

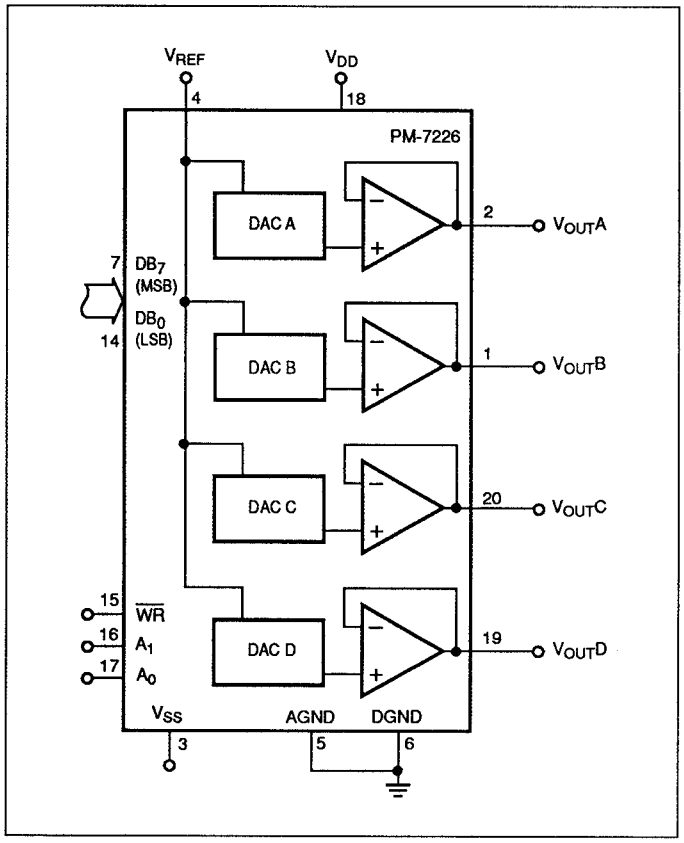


FIGURE 15: *Unipolar Operation*

TABLE 2: Unipolar Code Table (Refer to Figure 15)

DAC DATA INPUT MSB LSB								ANALOG OUTPUT (DAC A, B, C, or D)
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{256}\right) = \frac{+V_{REF}}{2}$
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

The table shows that there is no signal inversion between $+V_{REF}$ and V_{OUT}. Note that the analog output voltage is equal to V_{REF} multiplied by the digital input code (hence, multiplying DAC).

The expression for 1 LSB and V_{OUT} is:

1 LSB = V_{REF} x 2^{-8}, or V_{REF} x 1/256

and

$V_{OUT} = V_{REF}$ x D/256,

where D is the digital input integer between 0 and 255.

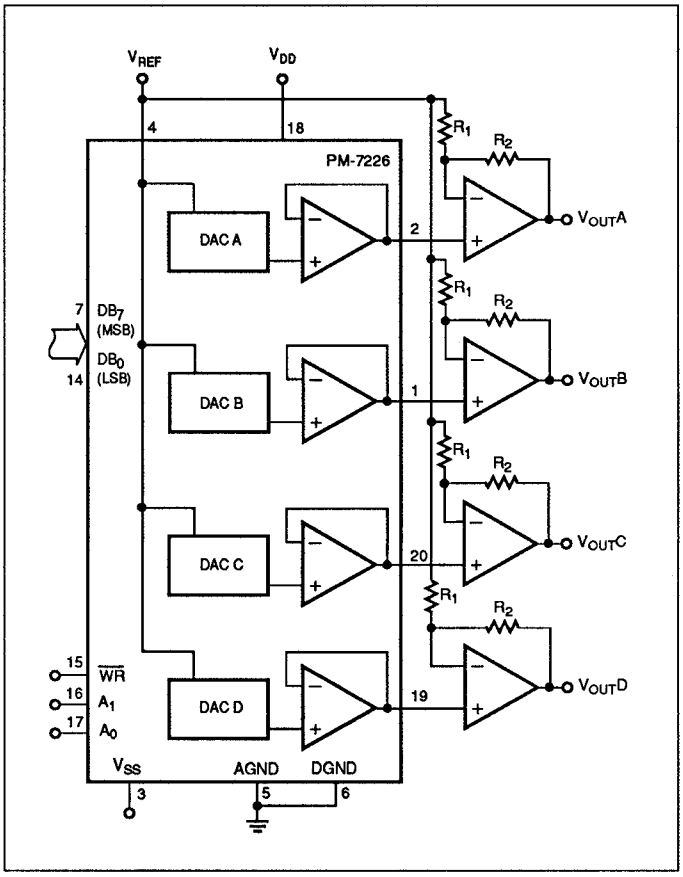


FIGURE 16: *Bipolar Operation*

TABLE 3: Bipolar Code Table (Refer to Figure 16)

DAC DATA INPUT MSB LSB								ANALOG OUTPUT (DAC A, B, C, or D)
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

BIPOLAR OPERATION

Figure 16 illustrates the PM-7226 in the bipolar mode of operation. This mode allows the output voltage to swing plus or minus and is determined by the digital input code; this can be seen in Table 3. This configuration requires an external amplifier and two resistors for each channel requiring bipolar operation.

The output voltage expression is given by:

$V_{OUT} = \left((1 + R_2/R_1) \times D/256 \times V_{REF}\right) - (R_2/R_1 \times V_{REF})$

where D is the digital input code integer between 0 and 255. If $R_1 = R_2$, then V_{OUT} becomes:

$V_{OUT} = (2 \times D/256 - 1) \times V_{REF}$

To keep gain and offset errors at a minimum, R_1 and R_2 should be matched to ±0.1% and track over the operating temperature range of interest.

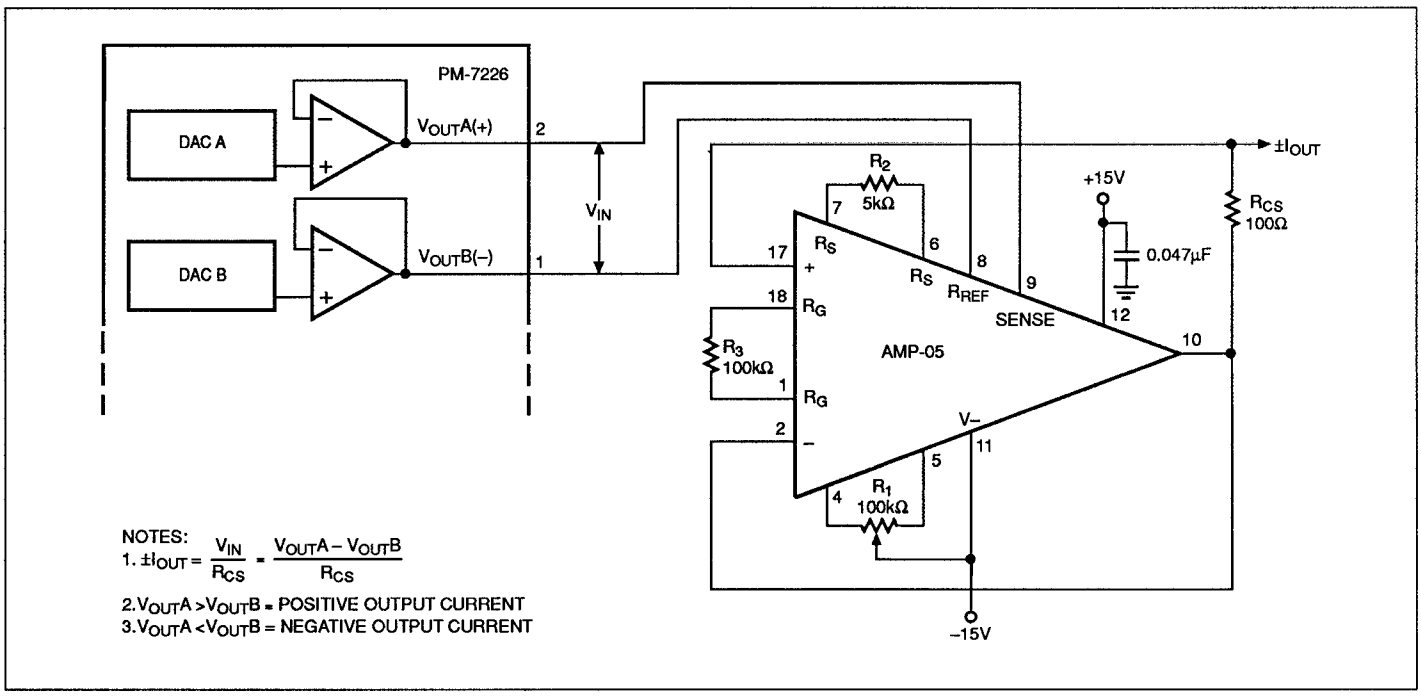


FIGURE 17: *High-Compliance, Digitally-Controlled Current Source*

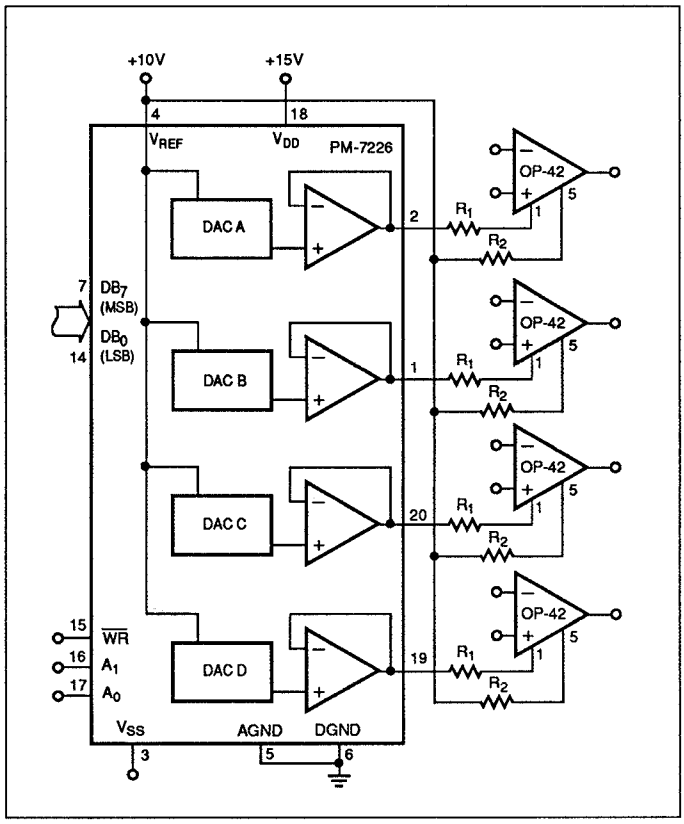


FIGURE 18: *Op Amp Offset Adjust (See Text)*

HIGH-COMPLIANCE BIPOLAR PRECISION CURRENT-SOURCE

Figure 17 shows the PM-7226 controlling a high-compliance, bipolar precision current source using PMI's AMP-05 instrumentation amplifier. The AMP-05's reference and sense pins become differential inputs, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS} in Figure 17. Voltage gain is set at unity, so the transfer function is simply: $I_{OUT} = (V_{OUT}A - V_{OUT}B)/R_{CS}$. Using a 100Ω resistor for R_{CS} limits the output current to ±10mA with a ±1V input.

Potentiometer R_1 trims the output current to zero with the two inputs at 0V. Fine gain adjustment may be accomplished by trimming R_2 or R_3.

PROGRAMMABLE OP AMP OFFSET ADJUST

The PM-7226 can be used for op amp offset trimming adjustments under microprocessor control. Offset caused by temperature drifts can be trimmed by the microprocessor during a periodic calibration cycle.

The PM-7226 uses the input offset voltage nulling pins normally provided on most amplifiers as shown in Figure 18. A fixed bias current is provided to pin 5 of the op amps offset null pins with R_2, and R_1 (connected to the DAC's voltage output pin) providing the variable current to pin 1.

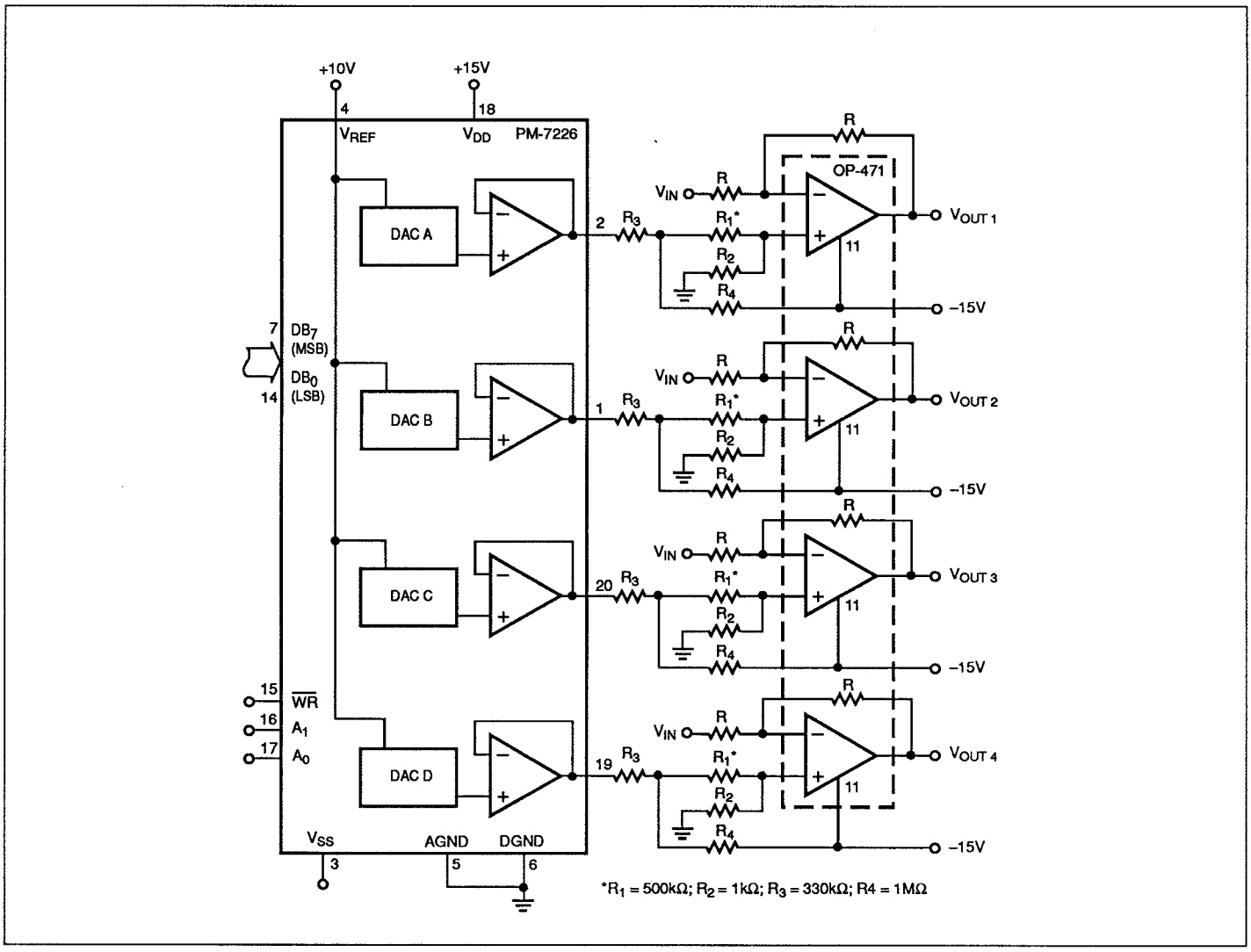


FIGURE 19: *Alternate Offset Adjust (See Text)*

In order to have a plus or minus (±) offset adjust control, the current through R_1 must equal the current through R_2 when the PM-7226 is at half scale, binary code = 1000 0000.

The resistor values (R_1, R_2) should be chosen to give the required offset adjustment range desired. Lower values provide a larger range; however, resolution will be sacrificed. Reversing connections at pins 1 and 5 (of the op amp) will reverse the offset adjustment direction.

Some op amps are not provided with offset adjustment pins, in these cases, the circuit configuration of Figure 19 can be used. Again, the current through resistor R_4 must equal the current through R_3 with the PM-7226 at half scale, digital code = 1000 0000.

With the circuit components shown, the maximum adjustment range is ±5mV. Incremental adjustment resolution is 39µV per bit.

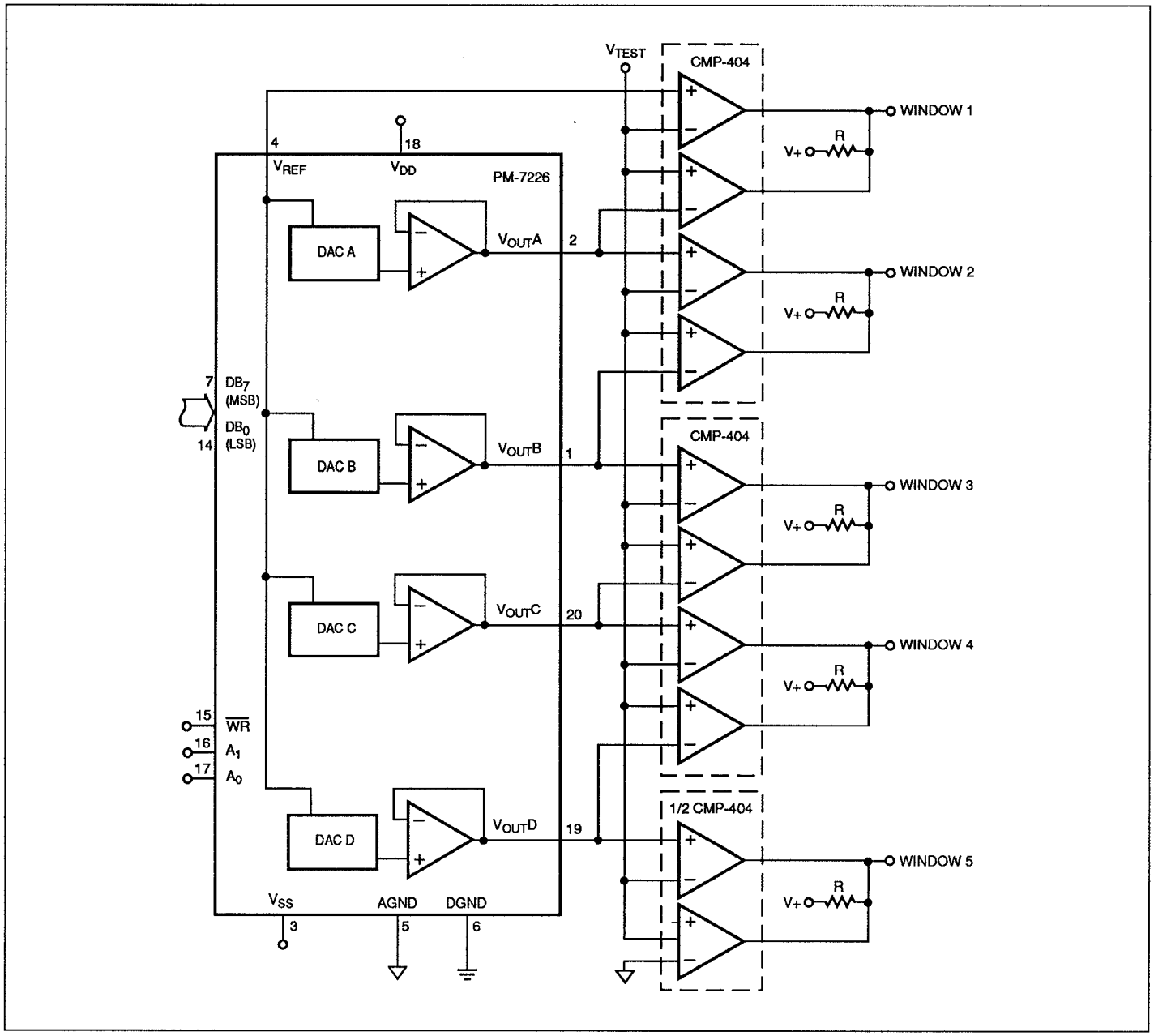


FIGURE 20: *Non-Overlapping Window Comparator*

STAIRCASE WINDOW COMPARATOR

Many applications need to determine whether voltage levels are within predetermined limits. Some requirements are for non-overlapping windows and others for overlapping windows. Both circuit configurations are shown in Figures 20 and 21, respectively.

The non-overlapping circuit uses one PM-7226 and ten comparators; this allows for five voltage windows. These windows range between V_{REF} and analog ground. Figure 20 shows that the first window is between V_{REF} and $V_{OUT}A$. $V_{OUT}A$ is also the upper limit of window 2, the lower limit being $V_{OUT}B$, etc. These limits (window size) can be microprocessor controlled. The relationship $V_{REF} > V_{TEST} >$ AGND apply.

More versatility can be obtained by connecting the output of DAC D ($V_{OUT}D$) to V_{REF}; this allows V_{REF} (which is common to all four DACs) to be under microprocessor control (see Programmable DAC Reference Voltage section). This, however, reduces the windows to four. Overlapping windows (Figure 21) will reduce the windows to three.

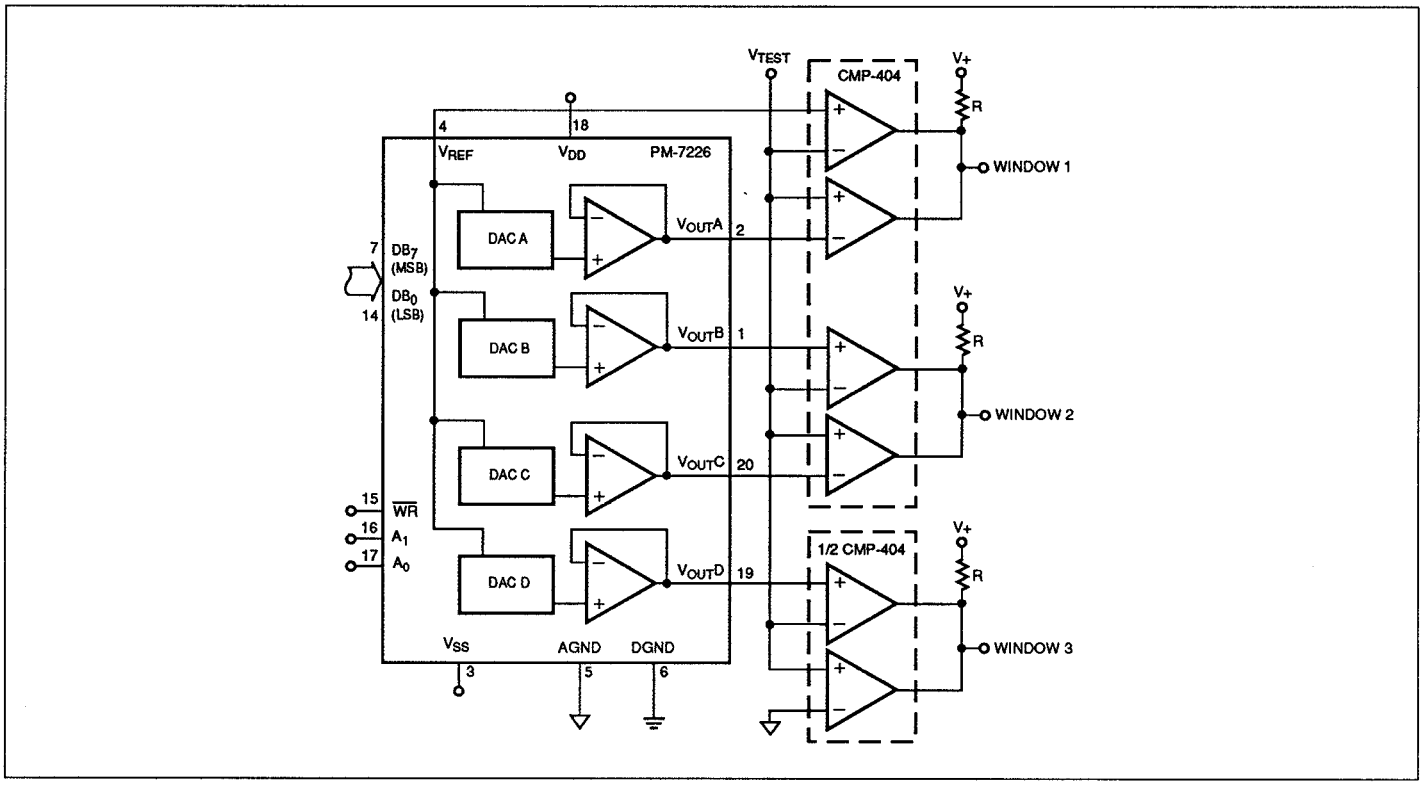


FIGURE 21: *Overlapping Window Comparator*

PROGRAMMABLE DAC REFERENCE VOLTAGE

With the PM-7226's flexibility, one of the internal DACs can be used to control V_{REF} for all of the DACs, and under microprocessor control.

The circuit configuration is shown in Figure 22. The relationship of V_{REF} to V_{IN} is dependent upon the digital code and the ratio of R_1 and R_2, and is given by:

$V_{REF} = [(1 + R)/(R \times D/256)] \times V_{IN}$

where $R = R_2/R_1$ (Figure 22)

D = Digital Input Code

Table 4 shows V_{REF} for various ratios of R_1 and R_2.

TABLE 4: V_{REF} vs. R_1, R_2 (see Figure 22)

R_1, R_2	DIGITAL INPUT CODE	V_{REF}
$R_1 = R_2$	0000 0000 (0/256)	$2V_{IN}$
$R_1 = R_2$	1000 0000 (128/256)	$1.3V_{IN}$
$R_1 = R_2$	1111 1111 (255/256)	V_{IN}
$R_2 = 3R_1$	0000 0000 (0/256)	$4V_{IN}$
$R_2 = 3R_1$	1000 0000 (128/256)	$1.6V_{IN}$
$R_2 = 3R_1$	1111 1111 (255/256)	V_{IN}

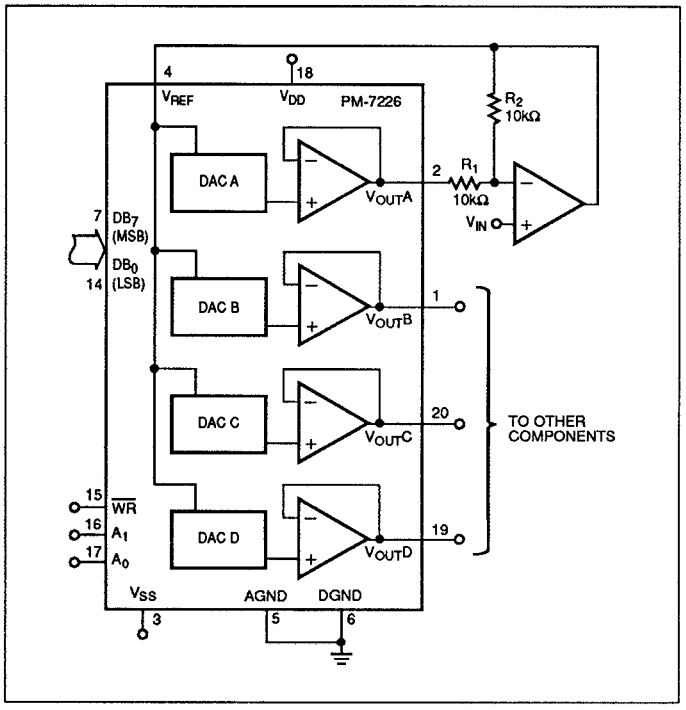


FIGURE 22: *Programmable DAC Reference*

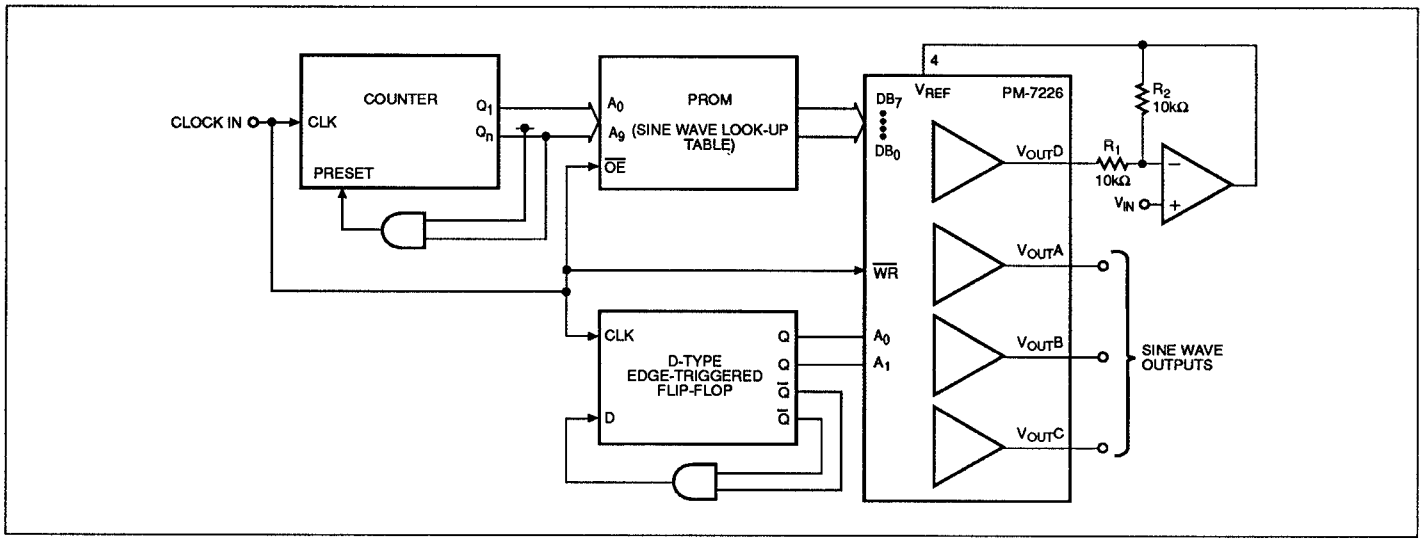


FIGURE 23: *3-Phase Sine Wave Generator Circuit (Using Counter)*

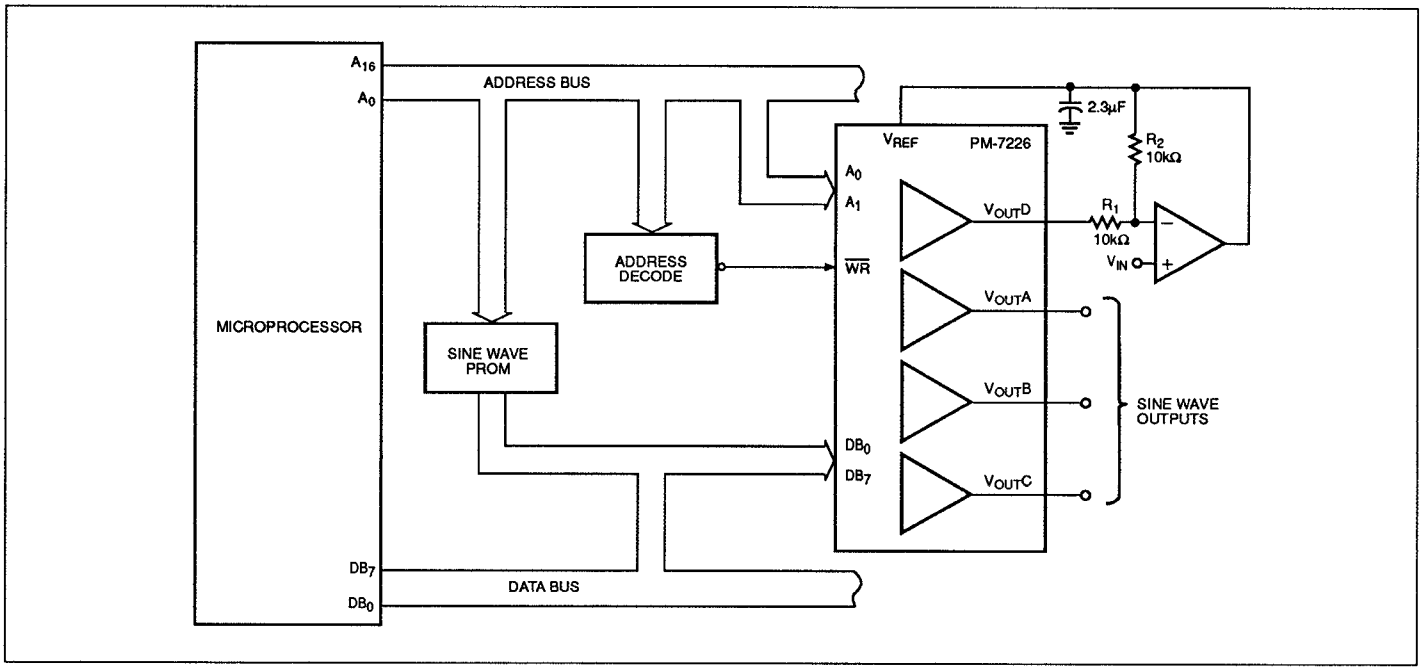


FIGURE 24: *3-Phase Sine Wave Generator Circuit (Under Microprocessor Control)*

This application works best with dual supplies. This is due to the DAC's output-current sink capability as V_{OUT} approaches 0V.

3-PHASE SINE WAVE GENERATION

The PM-7226 is well suited for 3-phase sine wave generation and with amplitude control. These sine waves can be used to control a shaft's rotational angle in small 3-phase synchro motors; some applications are antennas, robotics, and process controls. Other waveforms (such as triangular) may also be generated. The concept revolves around a PROM, counter, and a clock (or a microprocessor).

The sine wave codes are stored in a PROM in sets of three. Each set is 120° apart and has a 1.4° resolution (360°/256). These codes will use 768 memory address spaces (256 x 3).

Figure 23 shows the circuit using a counter, flip-flop, and a PROM; note that a clock is used to control the circuit. The counter counts through the PROM's addresses until the counter has stepped through the PROM's full look-up table; this completes a full cycle. The counter then resets and begins the cycle again when the last address data has been loaded into the PM-7226.

Sine wave generation can also be under microprocessor control; see Figure 24. The processor's software runs 3 phases to three DACs. Each phase is drawn from the PROM's look-up table.

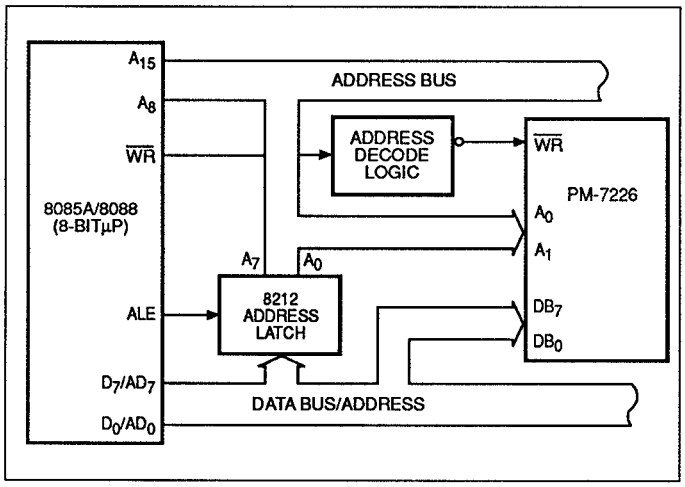


FIGURE 25: *PM-7226 to 8085A INTERFACE (Simplified circuit, only lines of interest are shown.)*

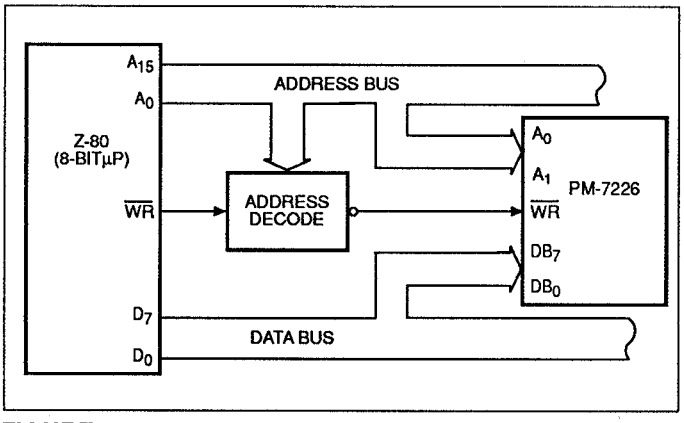


FIGURE 26: *PM-7226 to Z-80 INTERFACE (Simplified circuit, only lines of interest are shown.)*

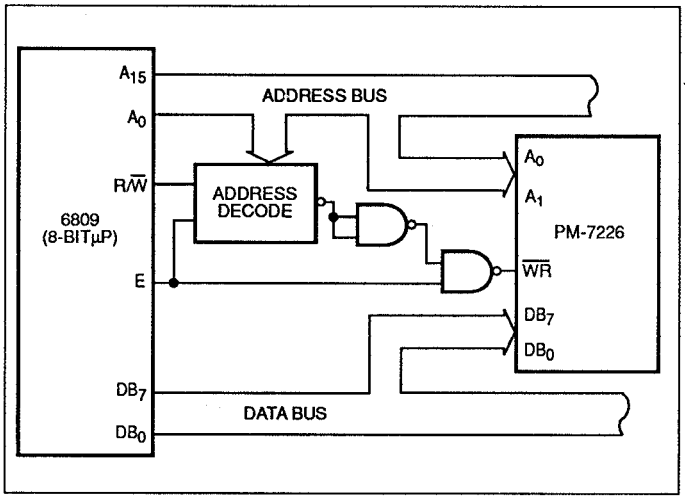


FIGURE 27: *PM-7226 to 6809 INTERFACE (Simplified circuit, only lines of interest are shown.)*

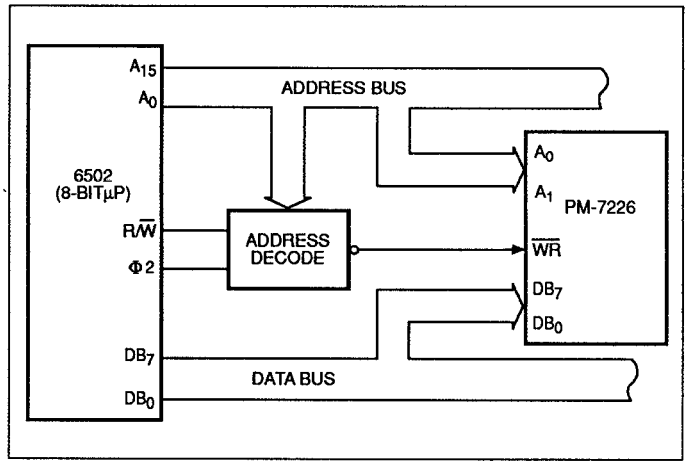


FIGURE 28: *PM-7226 to 6502 INTERFACE (Simplified circuit, only lines of interest are shown.)*

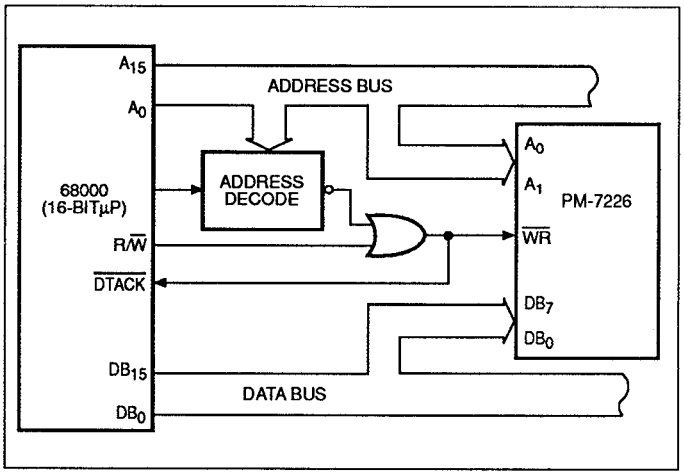


FIGURE 29: *PM-7226 to 68000 INTERFACE (Simplified circuit, only lines of interest are shown.)*

Any combination of wave shapes may be simultaneously generated. It only requires the functions to be programmed into the PROM on an interlace basis. The output amplitudes can also be microprocessor controlled; see previous section on Programmable DAC Reference Voltage.

MICROPROCESSOR INTERFACING

Interfacing the PM-7226 to a microprocessor is simplified by virtue of its loading structure simplicity. Data is loaded into the DAC by use of only three control lines, the write strobe ($\overline{WR}$) and two DAC selection control signals (A_0, A_1).

Figures 25 through 29 show various popular microprocessor interface configurations.

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