CCD image sensor
S9840

High UV sensitivity CCD image sensor

S9840 is a back-thinned type CCD image sensor specifically designed for spectrometers. S9840 has low noise, low dark signal and wide dynamic range. These enable low-light-level detection by setting a long integration time.
S9840 has a pixel size of 14 × 14 µm and active area of 28.672 (H) × 0.196 (V) mm (2048 × 14 pixels).

Features

- Optimized structure for full line binning (1D operation)
- High quantum efficiency in UV region
- Stable UV response
- Low dark current (MPP operation)
- No image-lag

Applications

- Spectrometer, etc.

■ General ratings

Parameter	Specification
Pixel size	14 (H) × 14 (V) µm
Number of pixels	2080 × 20 pixels
Number of active pixels	2048 × 14 pixels
Active area	28.672 (H) × 0.196 (V) mm
Vertical clock phase	2-phases
Horizontal clock phase	2-phases
Output circuit	Two-stage MOSFET source follower
Package	22-pin ceramic PGA
Window	Quartz glass

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
OFD voltage	V_{OFD}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGH voltage	V_{IGH}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

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■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Over flow drain voltage		V_{OFD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (input source)		V_{ISH}	-	V_{RD}	-	V
Test point (input gate)		V_{IGH}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Over flow gate voltage	High	V_{OFGH}	4	6	8	V
	Low	V_{OFGL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	4	6	8	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical shift register capacitance	C_{P1V}, C_{P2V}	-	300	-	pF
Horizontal shift register capacitance	C_{P1H} C_{P2H}	-	160	-	pF
Summing gate capacitance	C_{SG}	-	5	-	pF
Reset gate capacitance	C_{RG}	-	10	-	pF
Transfer gate capacitance	C_{TG}	-	60	-	pF

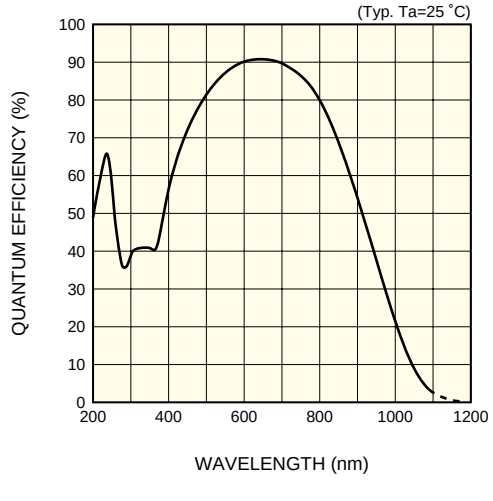
■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × Sv	-	V
Full well capacity	Fw	-	130	-	ke^-
CCD node sensitivity	Sv	-	4.0	-	$\mu V/e^-$
Dark current *1	DS	-	40	120	pA/cm^2
Readout noise *2	Nr	-	25	30	e^- rms
Readout speed	fc	-	-	5	MHz
Dynamic range *3	DR	-	5200	-	-
Spectral response range	λ	-	200 to 1100	-	nm
Photo response non-uniformity *4	PRNU	-	±3	±10	%

*1: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*2: At 2 MHz readout.
*3: Dynamic range (DR) = Full well/Readout noise
*4: Measured at the half of the full well capacity output.

$$PRNU = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

■ Spectral response (without window)



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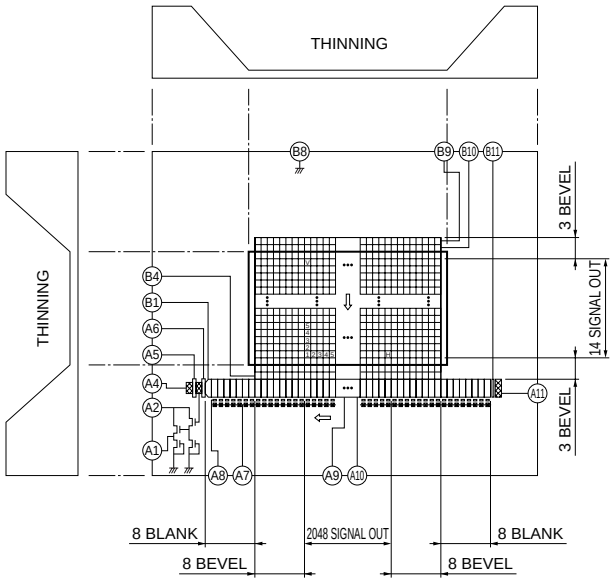
■ Device structure (Conceptual drawing of top view)



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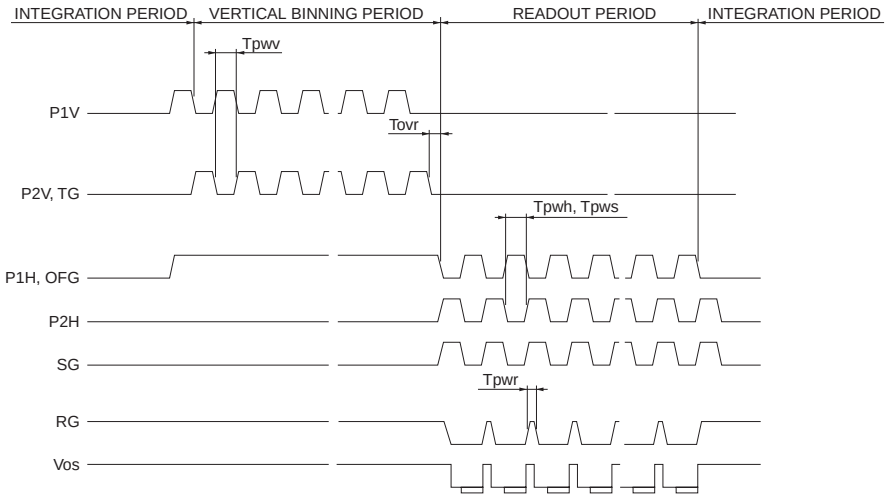
■ Timing chart (Line binning)



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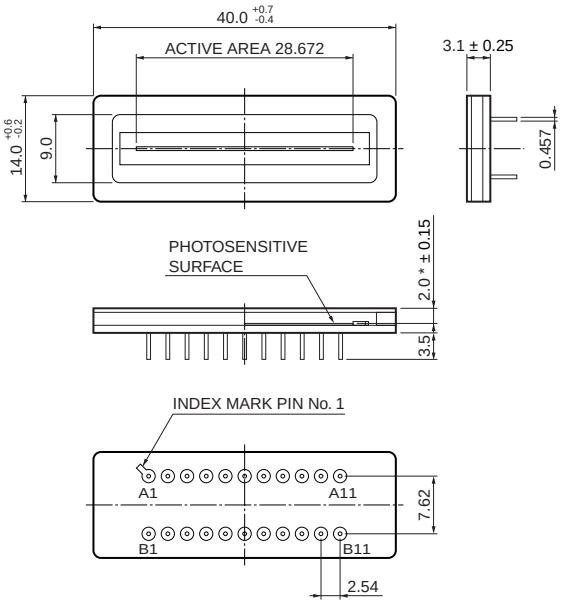
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*5	1	-	-	µs
	Rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H, OFG	Pulse width	Tpwh	*5	50	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	50	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	15	-	-	ns
	Rise and fall time	Tprr, Tpfr		10	-	-	ns
TG (P2V) - P1H	Overlap time	Tovr	-	3	-	-	µs

*5: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■ Dimensional outline (unit: mm)



* Distance between window surface and photosensitive surface

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■ Pin connections

Pin No.	Symbol	Function	Remark (standard operation)
A1	OS	Output transistor source, internal RL	Output signal
A2	OD	Output transistor drain	DC (+20 V)
A3	SS	Substrate (GND)	GND
A4	RD	Reset drain	DC (+12 V)
A5	RG	Reset gate	Clock (+6/-8 V)
A6	OG	Output gate	DC (+3 V)
A7	OFD	Output flow drain	DC (+12 V)
A8	OFG	Output flow gate	Same pulse as P1H
A9	P2H	CCD horizontal register clock-2	Clock (+6/-8 V)
A10	P1H	CCD horizontal resister clock-1	Clock (+6/-8 V)
A11	ISH	Test point (input source)	DC (+12 V)
B1	SG	Summing gate	Same pulse as P2H
B2	P2V	CCD vertical register clock-2	Clock (+6/-8 V)
B3	P1V	CCD vertical register clock-1	Clock (+6/-8 V)
B4	TG *6	Transfer gate	Same pulse as P2V
B5	-	-	-
B6	-	-	-
B7	RD	Reset drain	DC (+12 V)
B8	SS	Substrate (GND)	GND
B9	P1V	CCD vertical register clock-1	Clock (+6/-8 V)
B10	P2V	CCD vertical register clock-2	Clock (+6/-8 V)
B11	IGH	Test point (input gate)	GND

*6: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184, www.hamamatsu.com
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777
North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01
Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741

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