CY2DP1502

1:2 LVPECL Fanout Buffer

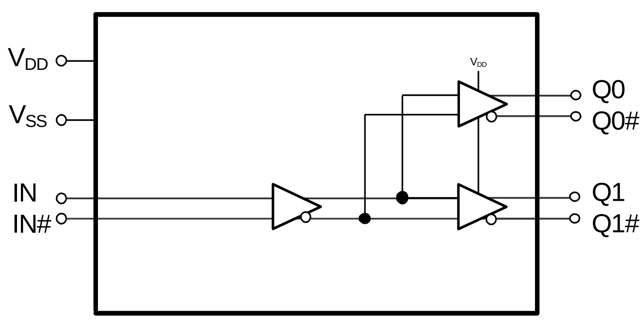
Features

- One low-voltage positive emitter-coupled logic (LVPECL) input pair distributed to two LVPECL output pairs
- 20-ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.15-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- 8-pin small outline integrated circuit (SOIC) or 8-pin thin shrunk small outline package (TSSOP) package
- 2.5-V or 3.3-V operating voltage[1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DP1502 is an ultra-low noise, low-skew, low-propagation delay 1:2 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

Logic Block Diagram



Note
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pinouts

Figure 1. Pin Diagram – 8-Pin SOIC and 8-Pin TSSOP Package

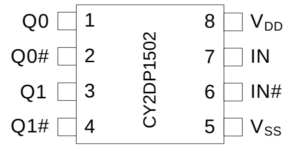


Table 1. Pin Definitions

Pin Number	Pin Name	Pin Type	Description
1,3	Q(0:1)	Output	LVPECL output clocks
2,4	Q(0:1)#	Output	LVPECL complementary output clocks
5	V_{SS}	Power	Ground
6	IN#	Input	LVPECL complementary input clock
7	IN	Input	LVPECL input clock
8	V_{DD}	Power	Power supply

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Nonfunctional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O voltage, relative to V_{SS}	Nonfunctional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Nonfunctional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC Latchup Test		
UL–94	Flammability rating	At 1/8 in	V-0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

Note
2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVPECL outputs floating (internal I_{DD})	–	45	mA
V_{IH}	Input high voltage, LVPECL inputs IN and IN#		–	V_{DD} + 0.3	V
V_{IL}	Input low voltage, LVPECL inputs IN and IN#		–0.3	–	V
V_{ID}[3]	Input differential amplitude	See Figure 2 on page 6	0.4	1.0	V
V_{ICM}	Input common mode voltage	See Figure 2 on page 6	0.5	V_{DD} – 0.2	V
I_{IH}	Input high current, LVPECL inputs IN and IN#	Input = V_{DD}[4]	–	150	µA
I_{IL}	Input low current, LVPECL inputs IN and IN#	Input = V_{SS}[4]	–150	–	µA
V_{OH}	LVPECL output high voltage	Terminated with 50 Ω to V_{DD} – 2.0[5]	V_{DD} – 1.20	V_{DD} – 0.70	V
V_{OL}	LVPECL output low voltage	Terminated with 50 Ω to V_{DD} – 2.0[5]	V_{DD} – 2.0	V_{DD} – 1.63	V
C_{IN}	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

Notes
3. V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
4. Positive current flows into the input pin, negative current flows out of the input pin.
5. Refer to Figure 3 on page 6.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency		DC	–	1.5	GHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
V_{PP}	LVPECL differential output voltage peak to peak, single-ended. terminated with 50 Ω to V_{DD} – 2.0[6]	Fout = DC to 150 MHz	600	–	–	mV
		Fout = >150 MHz to 1.5 GHz	400	–	–	mV
t_{PD}[7]	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	480	ps
t_{ODC}[8]	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz	48	–	52	%
t_{SK1}[9]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	20	ps
$t_{SK1\ D}$[9]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25-MHz Input Rise/fall time < 150 ps (20% to 80%) V_{ID} > 400 mV	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–145	dBc/Hz
		Offset = 10 MHz	–	–	–153	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
t_{JIT}[10]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	–	0.15	ps
t_R, t_F[11]	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%)	–	–	250	ps

Notes
6. Refer to Figure 3 on page 6.
7. Refer to Figure 4 on page 6.
8. Refer to Figure 5 on page 6.
9. Refer to Figure 6 on page 7.
10. Refer to Figure 7 on page 7.
11. Refer to Figure 8 on page 7.

Figure 2. Input Differential and Common Mode Voltages

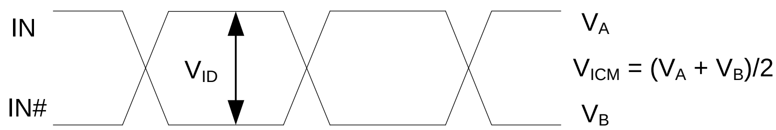


Figure 3. Output Differential Voltage

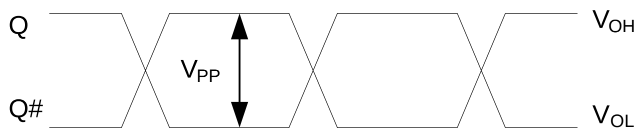


Figure 4. Input to Any Output Pair Propagation Delay

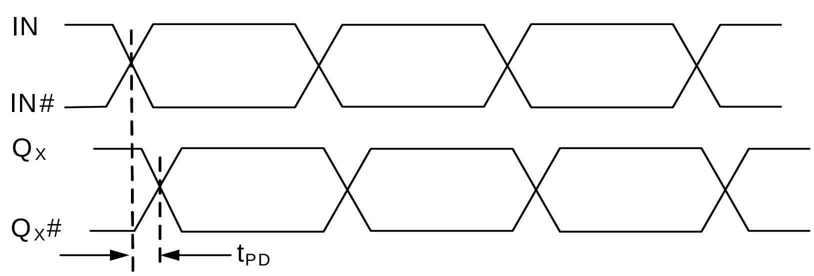


Figure 5. Output Duty Cycle

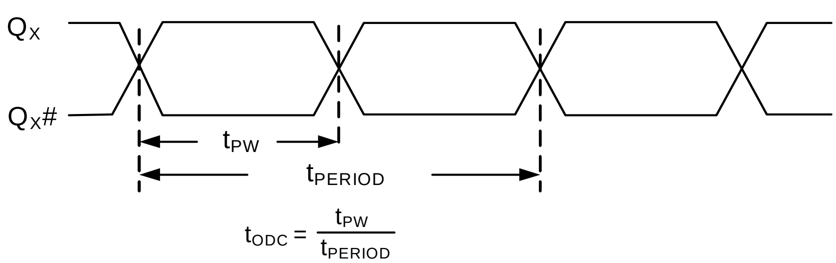


Figure 6. Output-to-Output and Device-to-Device Skew

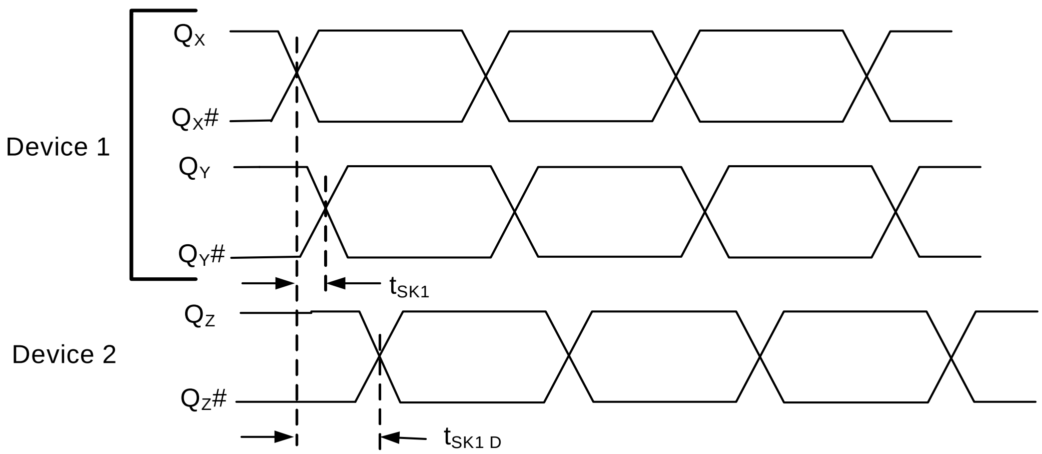


Figure 7. RMS Phase Jitter

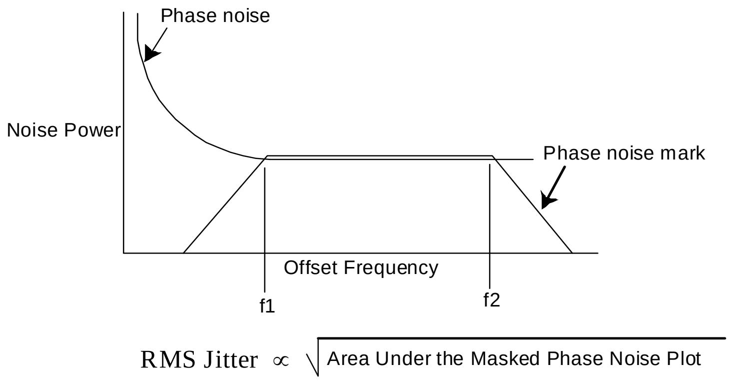
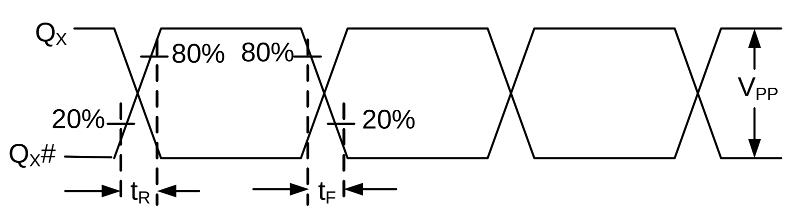


Figure 8. Output Rise/Fall Time



Ordering Information

Part Number	Type	Production Flow
Pb-free		
CY2DP1502SXC	8-Pin SOIC	Commercial, 0 °C to 70 °C
CY2DP1502SXCT	8-Pin SOIC tape and reel	Commercial, 0 °C to 70 °C
CY2DP1502SXI	8-Pin SOIC	Industrial, –40 °C to 85 °C
CY2DP1502SXIT	8-Pin SOIC tape and reel	Industrial, –40 °C to 85 °C
CY2DP1502ZXC	8-Pin TSSOP	Commercial, 0 °C to 70 °C
CY2DP1502ZXCT	8-Pin TSSOP tape and reel	Commercial, 0 °C to 70 °C
CY2DP1502ZXI	8-Pin TSSOP	Industrial, –40 °C to 85 °C
CY2DP1502ZXIT	8-Pin TSSOP tape and reel	Industrial, –40 °C to 85 °C

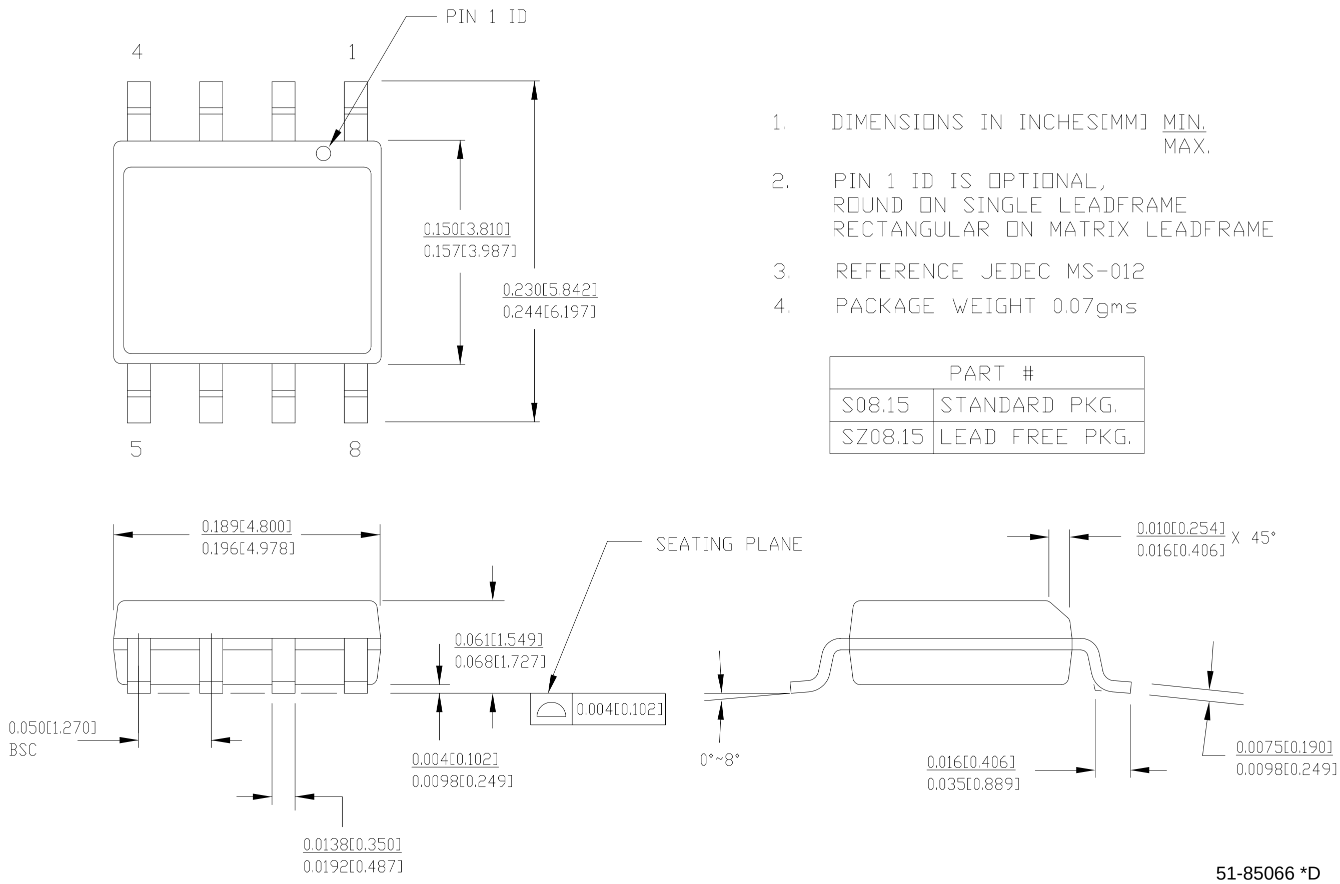
Ordering Code Definition

CY 2DP15 02 SX/ZX C/I T

- T: Tape and reel
- C/I: Temperature range
  C = Commercial
  I = Industrial
- SX/ZX: Pb-free packages
  SX: SOIC
  ZX: TSSOP
- 02: Number of differential output pairs
- 2DP15: Base part number
- CY: Company ID: CY = Cypress

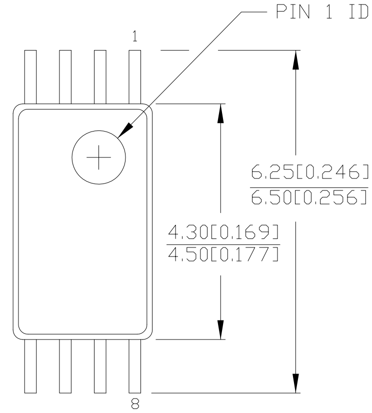
Package Dimensions

Figure 9. 8-Pin (150-Mil) SOIC S8



51-85066 *D

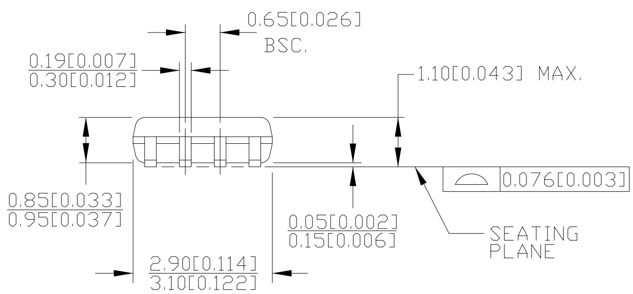
Figure 10. 8-Pin Thin Shrunk Small Outline Package (4.40 MM Body) Z8

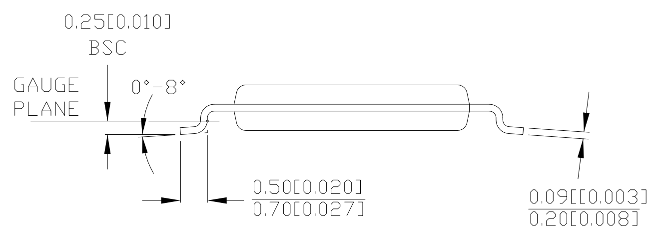


DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PART #	
Z08.173	STANDARD PKG.
ZZ08.173	LEAD FREE PKG.





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Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
JEDEC	Joint electron devices engineering council
LVDS	low-voltage differential signal
LVCMOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
OE	Output enable
RMS	root mean square
TSSOP	thin shrunk small outline package

Document Conventions

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	giga hertz
Hz	hertz
kΩ	kilo ohm
µA	microamperes
µF	micro Farad
µs	microsecond
mA	milliamperes
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	pico Farad
ps	pico second
V	volts
W	watts

Document History Page

Document Title: CY2DP1502 1:2 LVPECL Fanout Buffer Document Number: 001-56308				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2782891	CXQ	10/09/09	New Datasheet.
*A	2838916	CXQ	01/05/2010	Changed status from “ADVANCE” to “PRELIMINARY”. Changed from 0.34 ps to 0.25 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 4. Added t_{PU} spec to the Operating Conditions table on page 2. Change V_{OH} in the DC Electrical Specs table on page 3: minimum from V_{DD} - 1.15V to V_{DD} - 1.20V; maximum from V_{DD} - 0.75V to V_{DD} - 0.70V. Removed V_{OD} spec from the DC Electrical Specs table on page 3. Added R_P spec in the DC Electrical Specs table on page 3. Min = 60 kΩ, Max = 140 kΩ. Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 3. Added V_{PP} spec to the AC Electrical Specs table on page 4. V_{PP} min = 600 mV for DC - 150 MHz and min = 400 mV for 150 MHz to 1.5 GHz. Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 4 to be consistent with EROS. Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 4. Added condition to t_R and t_F specs in the AC Electrical specs table on page 4 that input rise/fall time must be less than 1.5 ns (20% to 80%). Changed letter case and some names of all the timing parameters in Figures 3, 4, 5, 6 and 8, to be consistent with EROS.
*B	3011766	CXQ	08/20/2010	Changed from 0.25 ps to 0.11 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table. Added note 3 to describe I_{IH} and I_{IL} specs. Removed reference to data distribution from “Functional Description”. Changed R_P for differential inputs from 100 kΩ to 150 kΩ in the Logic Block Diagram and from 60 kΩ min / 140 kΩ max to 90 kΩ min / 210 kΩ max in the DC Electrical Specs table. Added max V_{ID} of 1.0V in DC Electrical Specs table. Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table. Added “Frequency range up to 1 GHz” condition to t_{ODC} spec. Updated package diagrams. Added Acronyms and Ordering Code Definition.
*C	3017258	CXQ	08/27/2010	Corrected Output Rise/Fall time diagram.
*D	3100234	CXQ	11/18/2010	Updated Phase jitter to 0.15ps max from 0.11ps max. Changed V_{IN} and V_{OUT} specs from 4.0V to “lesser of 4.0 or V_{DD} + 0.4” Removed 200mA min LU spec, replaced with “Meets or exceeds JEDEC Spec JESD78B IC Latchup Test” Removed R_P spec for differential input clock pins IN_X and IN_X#. Changed C_{IN} condition to “Measured at 10 MHz”. Changed PN_{ADD} specs for 1MHz, 10MHz, and 20MHz offsets.
*E	3137726	CXQ	01/13/2011	Removed “Preliminary” status heading. Removed resistors on IN/IN# from Logic Block Diagram.
*F	3137726	CXQ	01/13/2011	Rev’ed and posted
*G	3234654	VED	04/19/2011	Minor change, no content change.

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