CPU Clock Generator

Description

The **ICS2492** CPU Clock Generator is an integrated circuit dual phase locked loop frequency synthesizer capable of generating 16 CPU frequencies and two other clock frequencies for use with high performance personal computer motherboards. Utilizing CMOS technology to implement all linear, digital and memory functions, the **ICS2492** provides a low-power, small footprint, low-cost solution to the generation of CPU clocks. Provision is made via a single level custom mask to implement customer-specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies.

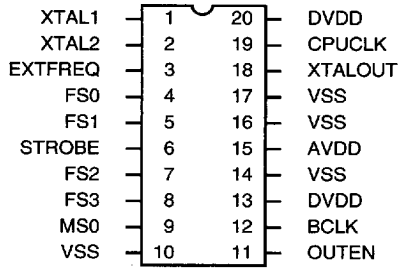
The **ICS2492** is fully pin and function compatible with ICS's industry-standard ICS2494 dual clock generator except that an output enable function has been added to pin 11. A pre-programmed version with a full selection of CPU clocks is available as part number **ICS2492-453**. The frequencies in this pattern are essentially identical to those in the ICS2494-244 standard pattern.

Features

- Low cost - eliminates need for multiple crystal clock oscillators in motherboard applications
- Mask-programmable frequencies
- Pre-programmed versions for a selection of CPU clocks
- Glitch-free frequency transitions
- Provision for external frequency input
- Internal clock remains locked when the external frequency input is selected
- Low power CMOS device technology
- Small footprint - 20-pin DIP or SOIC
- Buffered XTAL Out
- Integral Loop Filter components
- Fast acquisition of selected frequencies, strobed or non-strobed
- Guaranteed performance up to 135 MHz
- Excellent power supply rejection
- Advanced PLL for low phase-jitter
- Output Enable function for tristate control of the two clock outputs.

C

Pin Configuration



20-Pin DIP or SOIC
K-4, K-7

Notes:

1. In applications where the external frequency input is not specified, EXTFREQ must be tied to V_{SS}.
2. ICS2492M(SOIC) pinout is identical to ICS2492N(DIP).

Circuit and Application Options

The **ICS2492** will typically derive its frequency reference from a series-resonant crystal connected between pins 1 and 2. Where a high quality reference signal is available, such as in an application where the graphics subsystem is resident on the motherboard, this reference may directly replace the crystal. This signal should be coupled to pin 1. If the reference signal amplitude is less than 3.5 volts, a .047 microfarad capacitor should be used to couple the reference signal into **XTAL1**. Pin 2 must be left open.

The **ICS2492** is capable of multiplexing an externally generated frequency source of **VCLK** via a mask option, in addition to its internally-generated clock.

This is input via **EXTFREQ (3)**. When an external source is selected, the PLL remains locked to the value specified in the selected address. This provision facilitates the ability to rapidly change frequencies. When this option is not specified in the ROM pattern, pin 3 is internally tied to V_{SS} and should be connected to V_{SS} on the PCB.

Power Supply Conditioning

The **ICS2492** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in most applications it is judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 Volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 Volt analog supply is available, although the improved performance comes at a cost of an extra component; however, the cost of the discretes used in Figure 2 is less than the cost of Figure 1's discrete components.

The number and differentiation of the analog and digital supply pins are intended for maximum performance products. In most applications, all V_{DDS} may be tied together. The function of the multiple pins is to allow the user to realize the maximum performance from the silicon with a minimum degradation due to the package and PCB. At the frequencies of interest, the effects of the inductance of the bond wires and package lead frame are non-trivial. By using the multiple pins, ICS has minimized the effect of packaging and has minimized the interaction of the digital and analog supply currents.

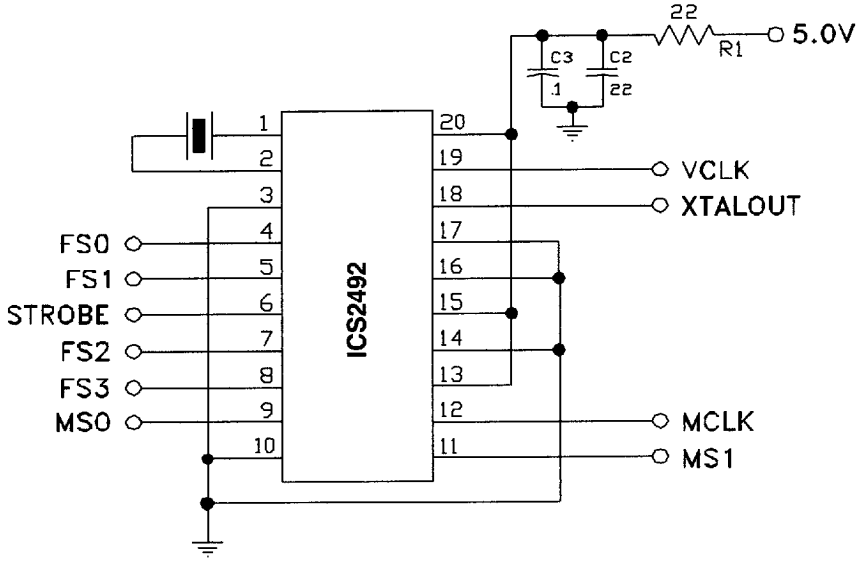


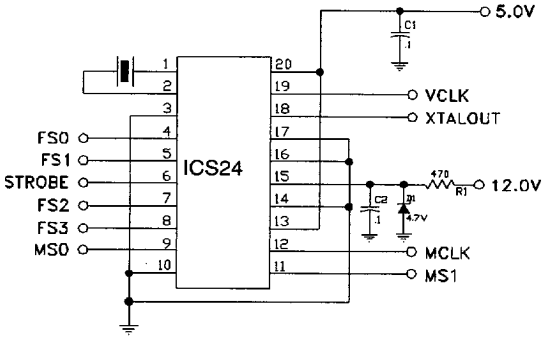
Figure 1

Applications

Layout Considerations

Utilizing the **ICS2492** in video graphics adapter cards or on PS2 motherboards is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. Care should be exercised in ensuring that components not related to the **ICS2492** do not share its ground. In applications utilizing a multi-layer board, V_{SS} should be directly connected to the ground plane. Multiple pins are utilized for all analog and digital Vss and Vdd connections to permit extended frequency **VCLK** operation to 135 MHz. However, in all cases, all V_{SS} and V_{DD} pins should be connected.

Figure 2



Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between **XTAL1 (1)** and **XTAL2 (2)**. In IBM-compatible applications this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2492**. In some applications, it may be desirable to utilize the bus clock. If the signal amplitude is equal to or greater than 3.5 volts, it may be connected directly to **XTAL1 (1)**. If the signal amplitude is less than 3.5 volts, connect the clock through a .047 microfarad capacitor to **XTAL1 (1)**, and keep the lead length of the capacitor to **XTAL1 (1)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD}/2$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity.

The **ICS2492** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of this signal is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (2)** must be left open in this configuration.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2492** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator in the system, saving money as well as board space. To do this, the **XTALOUT (18)** output should be buffered with a CMOS driver.

Output Circuit Considerations

As the dot clock is usually the highest frequency present in a video graphics system, consideration should be given to EMI. To minimize problems with meeting FCC EMI requirements, the trace which connects **VCLK (19) or MCLK (12) and other components in the system should be kept as short as possible. The ICS2492** outputs have been designed to minimize overshoot. In addition, it may be helpful to place a ferrite bead in these signal paths to limit the propagation of high order harmonics of this signal. A suitable device would be a Ferroxcube 56-590-65/4B or equivalent. This device should be placed physically close to the **ICS2492**. A 33 to 47 Ohm series resistor, sometimes called source termination, in this path may be necessary to reduce ringing and reflection of the signal and may reduce phase-jitter as well as EMI.

External Frequency Sources

EXTFREQ (3) on versions so equipped by the programming, is an input to a digital multiplexer. When this input is enabled, signals driving the input will appear at **VCLK (19)** instead of the PLL output. Internally, the PLL will remain in lock at the frequency selected by the ROM code.

Digital Inputs

FS0 (4), FS1 (5), FS2 (7), and **FS3 (8),** are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (6),** when high, allows new data into the frequency select latches; and when low, prevents address changes per Figure 3. The internal power-on-clear signal will force an initial frequency code corresponding to an all-zeros input state. **MS0 (9)** and **MS1 (11)** are the corresponding memory select inputs and are not strobed.

Absolute Maximum Ratings

Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD}+0.5V
Output Voltage	V_{OUT}	-0.5V to VDD+0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+/ -30mA
Output Current per Pin	I_{OUT}	+/ -50mA
Operating Temperature	T_o	0°C to 70°C
Storage Temperature	T_S	-85 °C to +150°C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to >= V_{SS} and <=V_{DD}.

DC Characteristics (0°C to 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.0	5.5	V
Input Low Voltage	V_{IL}	V_{DD} = 5V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN} = V_{cc}	-	10	uA
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 4.0 mA	2.4	-	V
Supply Current	I_{DD}	V_{DD} = 5V, VCLK = 80 MHz	-	27	mA
Internal Pull-up Resistors	R_{UP} *	V_{dd} = 5V, V_{in} = 0V	50	200	k ohm
Input Pin Capacitance	C_{in}	F_c = 1 MHz	-	8	pf
Output Pin Capacitance	C_{out}	F_c = 1 MHz	-	12	pf

* The following inputs have pull-ups: FS0-3, MS0-1, STROBE.

AC Timing Characteristics

The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Rise and fall time is between 0.8 and 2.0 VDC.
5. Output pin loading = 25pF
6. Duty cycle is measured at 1.4V.
7. Supply Voltage Range = 4.0 to 5.5 Volts
8. Temperature Range = 0 °C to 70 °C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	MCLK AND VCLK TIMINGS			
Tr	Rise Time	-	3	Duty Cycle 40% min. to
Tf	Fall Time	-	3	60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz
-	Propagation Delay for Pass Through Frequency	-	15	ns

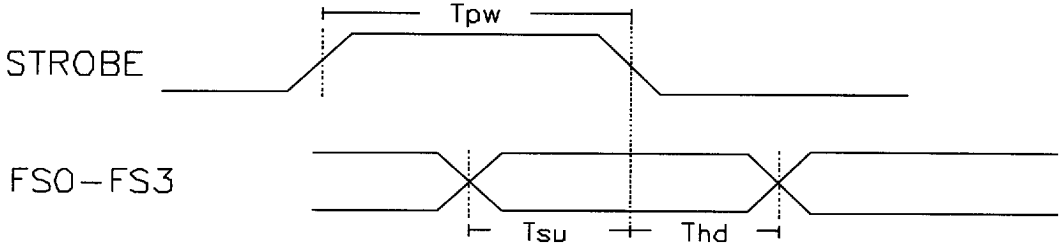


Figure 3

ICS2492 Pattern Request Form

In addition to the pattern below, custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS sales for details.

ICS Part Number	ICS2492-453		ICS2492-Custom Pattern #1
Address FS3-0 (Hex)	Frequency (MHz)	Application	Frequency (MHz)
0	20	286-10	
1	24	-12	
2	32	386-16	
3	40	-20	
4	50	-25	
5	66.6	-33	
6	80	-40	
7	100	-50	
8	54	TURBO-27	
9	70	-35	
0	90	-45	
B	110	-55	
C	25	486-25	
D	33.3	-33	
E	40	-40	
F	50	-50	
Address MS0 (Hex)	Frequency (MHz)	Application	Frequency (MHz)
0	16	AT-BUS	
1	24	FDC	

Custom pattern #1 reference frequency = _____

The standard frequency shown has been specified by and is supported by the respective VGA manufacturer.

The standard pattern shown above uses _____ MHz as the input reference frequency.

Order Information: ICS2492M-XXX or ICS2492N-XXX (XXX=Pattern number)

Ordering Information

ICS2492N-XXX or ICS2492M-XXX

Example:

ICS XXXX N -XXX

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  - N=DIP (Plastic)
  - M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device