Data Sheet | May 12, 2008 | FN6044.4

Low-Voltage, Single Supply, DPDT High Performance Analog Switch

The Intersil ISL43410 is a precision, bidirectional, analog switch configured as a double pole/double throw (DPDT) switch. The ISL43410 is designed to operate from a single +2V to +12V supply. It is equipped with an inhibit pin to simultaneously open all signal paths.

ON-resistance is 115Ω with a +5V supply, 45Ω with a +12V supply, and 190Ω with a +3V supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 3nA at +25°C or 5nA at +85°C. All digital inputs have 0.8V to 2.4V logic thresholds ensuring TTL/CMOS logic compatibility when using a single +5V supply. Some of the smallest packages are available, alleviating board space limitations, and making Intersil's newest line of low-voltage switches an ideal solution.

The ISL43410 is a DPDT, which is perfect for use in 2-to-1 multiplexer applications.

Table 1 summarizes the performance of this switch.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	DPDT
12V r_{ON}	45Ω
12V t_{ON}/t_{OFF}	25ns/24ns
4.5V r_{ON}	115Ω
4.5V t_{ON}/t_{OFF}	60ns/30ns
3V r_{ON}	190Ω
3V t_{ON}/t_{OFF}	120ns/45ns
Packages	10 Ld MSOP, 16 Ld 3x3 QFN

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Application Note AN557 "Recommended Test Procedures for Analog Switches"
- Application Note AN520 "CMOS Analog Multiplexers and Switches; Specifications and Application Considerations"
- Application Note AN1034 "Analog Switch and Multiplexer Applications"

Features

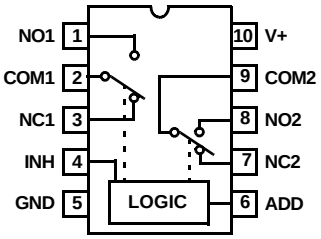
- Fully Specified at 3V, 5V, and 12V Supplies for 10% Tolerances
- ON-Resistance (r_{ON}), V_S = 5V 100Ω
- r_{ON} Matching Between Channels . . . . . <2Ω
- Low Charge Injection . . . . . 3pC (Max)
- Single Supply Operation . . . . . +2V to +12V
- Low Power Consumption (P_D) . . . . . <3µW
- Low Off Leakage Current 5nA
- Fast Switching Action (V_S = 5V)
  - t_{ON} 60ns
  - t_{OFF} 30ns
- Guaranteed Break-Before-Make
- TTL, CMOS Compatible
- Available in 10 Ld MSOP and 16 Ld QFN Packages
- Pb-Free Available (RoHS Compliant)

Applications

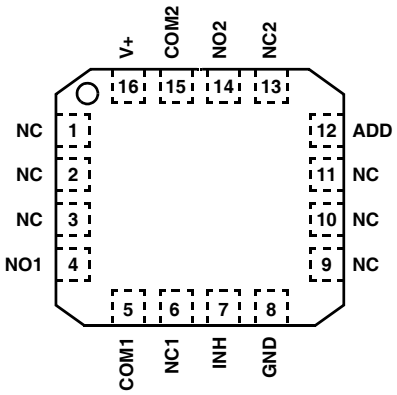
- Battery-Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Electrocardiograph
  - Magnetic Resonance Imaging
  - CT and PET Scanners (MRI)
  - ATE
- Audio and Video Switching
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinouts (Note 1)

ISL43410
(10 LD MSOP)
TOP VIEW



ISL43410
(16 LD 3X3 QFN)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Inputs.

Truth Table

ISL43410

INH	ADD	SWITCH ON
1	X	NONE
0	0	NCx
0	1	NOx

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V, with V_S between 3.3V and 11V.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+2V to +12V)
GND	Ground Connection
INH	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
COMx	Analog Switch Common Pin
NOx	Analog Switch Normally Open Pin
NCx	Analog Switch Normally Closed Pin
ADD	Address Input Pin
NC	No Internal Connection

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL43410IU	3410	-40 to +85	10 Ld MSOP	M10.118
ISL43410IU-T*	3410	-40 to +85	10 Ld MSOP	M10.118
ISL43410IUZ (Note)	3410Z	-40 to +85	10 Ld MSOP (Pb-free)	M10.118
ISL43410IUZ-T* (Note)	3410Z	-40 to +85	10 Ld MSOP (Pb-free)	M10.118
ISL43410IR	410I	-40 to +85	16 Ld QFN	L16.3x3
ISL43410IR-T*	410I	-40 to +85	16 Ld QFN	L16.3x3
ISL43410IRZ (Note)	341Z	-40 to +85	16 Ld QFN (Pb-free)	L16.3x3
ISL43410IRZ-T* (Note)	341Z	-40 to +85	16 Ld QFN (Pb-free)	L16.3x3

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3V to 15V
Input Voltages
INH, NO, NC, ADD (Note 2) . . . . . -0.3V to ((V+) + 0.3V)
Output Voltages
COM (Note 2) . . . . . -0.3V to ((V+) + 0.3V)
Continuous Current (Any Terminal) 30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) 40mA

Operating Conditions

Temperature Range
ISL43410Ix. . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld MSOP Package (Note 3)	190	N/A
16 Ld QFN Package (Notes 4, 5).	58	11

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Moisture Sensitivity (See Technical Brief TB363)
All Packages . . . . . Level 1
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on NC, NO, COM, ADD, or INH exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications +5V Supply

Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 12)	TYP	MAX (Notes 7, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, (See Figure 5, Note 11)	25	-	115	125	Ω
		Full	-	-	150	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, (Notes 9, 11)	25	-	1	3	Ω
		Full	-	-	5	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 5.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V, 2.5V, 3.5V, (Notes 10, 11)	25	-	12	13	Ω
		Full	-	13	18	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V (Note 8)	25	-3	-	3	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 4.5V, 1V, V_{NO} or V_{NC} = 1V, 4.5V (Note 8)	25	-3	-	3	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V, or V_{NO} or V_{NC} = 1V, 4.5V, or Floating (Note 8)	25	-3	-	3	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.4	1.4	-	V
Input Voltage Low, V_{INL}		Full	-	1.3	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 5.5V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)	25	-	60	-	ns
		Full	-	75	-	ns

Electrical Specifications +5V Supply Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 12)	TYP	MAX (Notes 7, 12)	UNITS
Inhibit Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)	25	-	30	-	ns
		Full	-	35	-	ns
Address Transition Time, t_{TRANS}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (See Figure 1)	25	-	61	-	ns
		Full	-	76	-	ns
Break-Before-Make Time Delay, t_D	V+ = 5.5V, R_L = 300Ω, C_L = 35pF, V_{NO} = V_{NC} = 3V, V_{IN} = 0 to 3 (See Figure 3)	Full	-	16	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	0.3	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz (see Figure 4)	25	-	75	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz (see Figure 6)	25	-	-85	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	4	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	6	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	12	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.0001	1	µA

Electrical Specifications +3V Supply Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{AH} = 2.4V, V_{AL}= 0.8V (Note 6), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 12)	TYP	MAX (Notes 7, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (see Figure 5, Note 11)	25	-	190	220	Ω
		Full	-	-	250	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (Notes 9, 11)	25	-	1	3	Ω
		Full	-	-	5	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1.5V (Notes 10, 11)	25	-	48	90	Ω
		Full	-	-	90	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 1V, 3V, V_{NO} or V_{NC} = 3V, 1V (Note 8)	25	-3	-	3	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, 1V, V_{NO} or V_{NC} = 1V, 3V (Note 8)	25	-3	-	3	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 1V, 3V, or V_{NO} or V_{NC} = 1V, 3V, or floating (Note 8)	25	-3	-	3	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.0	1.0	-	V
Input Voltage Low, V_{INL}		Full	-	0.8	0.5	V
Input Current, I_{INH}, I_{INL}	V+ = 3.6V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA

Electrical Specifications +3V Supply

Test Conditions: V+ = +2.7V to +3.6V, GND = 0V, V_{AH} = 2.4V, V_{AL} = 0.8V (Note 6), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 12)	TYP	MAX (Notes 7, 12)	UNITS
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF V_{IN} = 0 to 3 (see Figure 1)	25	-	144	-	ns
		Full	-	165	-	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF V_{IN} = 0 to 3 (see Figure 1)	25	-	53	-	ns
		Full	-	60	-	ns
Address Transition Time, t_{TRANS}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF V_{IN} = 0 to 3 (see Figure 1)	25	-	145	-	ns
		Full	-	180	-	ns
Break-Before-Make Time Delay, t_D	V+ = 3.6V, R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 1.5V V_{IN} = 0 to 3 (see Figure 3)	Full	-	35	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	0.5	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz (see Figure 4)	25	-	75	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz (see Figure 6)	25	-	-85	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	4	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	6	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	12	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.0001	1	µA

Electrical Specifications + 12V Supply

Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 12)	TYP	MAX (Notes 7, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 12.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (see Figure 5, Note 11)	25	-	45	50	Ω
		Full	-	-	70	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 12.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V (Notes 9,11)	25	-	0.5	3	Ω
		Full	-	-	5	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 13.2V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V (Notes 10, 11)	25	-	5	6	Ω
		Full	-	-	10	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13.0V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V (Note 7)	25	-3	-	3	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13.0V, V_{COM} = 12V, 1V, V_{NO} or V_{NC} = 1V, 12V (Note 7)	25	-3	-	3	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13.0V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V or floating (Note 7)	25	-3	-	3	nA
		Full	-5	-	5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}		Full	2.9	2.5	-	V
Input Voltage Low, V_{INL}		Full	-	2.3	0.8	V
Input Current, I_{INH}, I_{INL}	V+ = 13V, V_{IN} = 0V or V+	Full	-0.5	-	0.5	µA

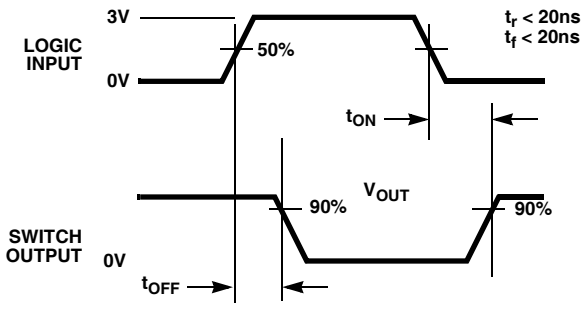
Electrical Specifications + 12V Supply Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 6), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 12)	TYP	MAX (Notes 7, 12)	UNITS
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF V_{IN} = 0 to 4, (see Figure 1)	25	-	25	-	ns
		Full	-	30	-	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF V_{IN} = 0 to 4, (see Figure 1)	25	-	24	-	ns
		Full	-	30	-	ns
Address Transition Time, t_{TRANS}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF V_{IN} = 0 to 4, (see Figure 1)	25	-	35	-	ns
		Full	-	50	-	ns
Break-Before-Make Time Delay, t_D	V+ = 13.0V, R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 10V V_{IN} = 0 to 4 (see Figure 3)	Full	-	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25	-	1.2	-	pC
OFF-Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz, (see Figure 4)	25	-	75	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz, (see Figure 6)	25	-	-85	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 7)	25	-	4	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 7)	25	-	6	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (see Figure 7)	25	-	12	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.0V, V_{IN} = 0V or V+, all channels on or off	Full	-1	0.0001	1	µA

NOTES:

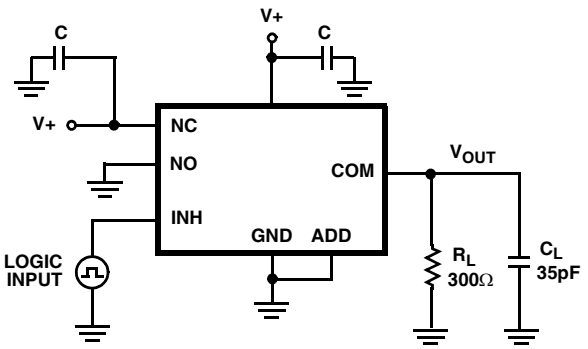
6. V_{IN} = input voltage to perform proper function.
7. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
8. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at +25°C.
9. $\Delta r_{ON} = r_{ON}$ (MAX) - r_{ON} (MIN).
10. Flatness is defined as the difference between the maximum and minimum value of ON-resistance over the specified analog signal range.
11. Limits established by characterization and are not production tested.
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

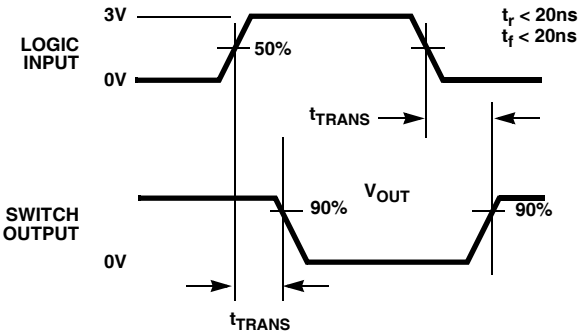


Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + r_{ON}}$$

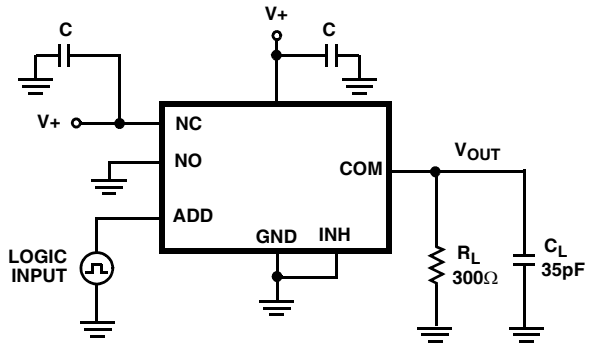
FIGURE 1B. TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1D. ADDRESS TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

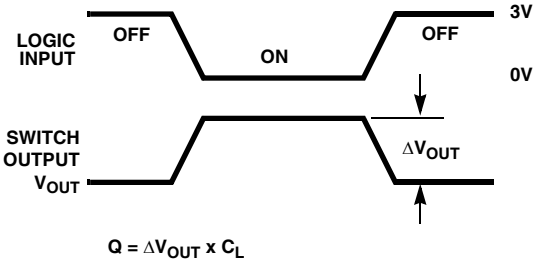


FIGURE 2A. MEASUREMENT POINTS

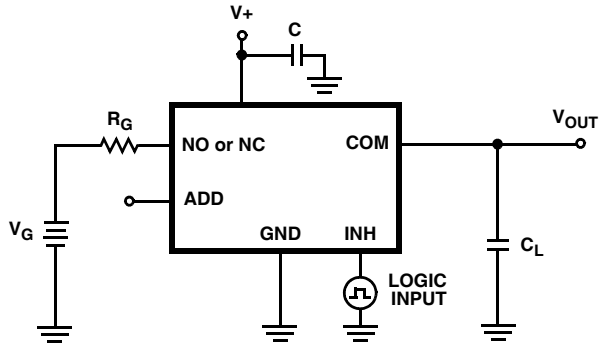


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

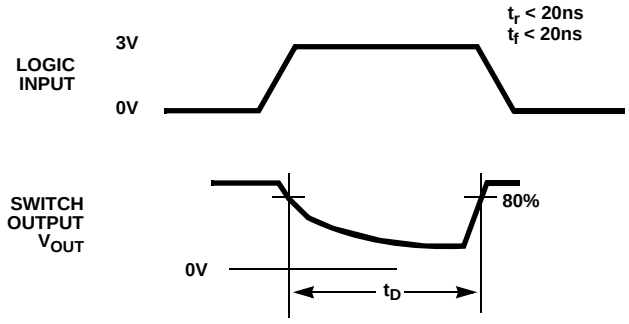
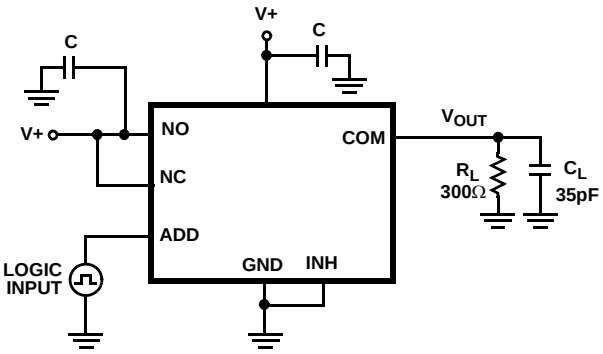


FIGURE 3A. MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

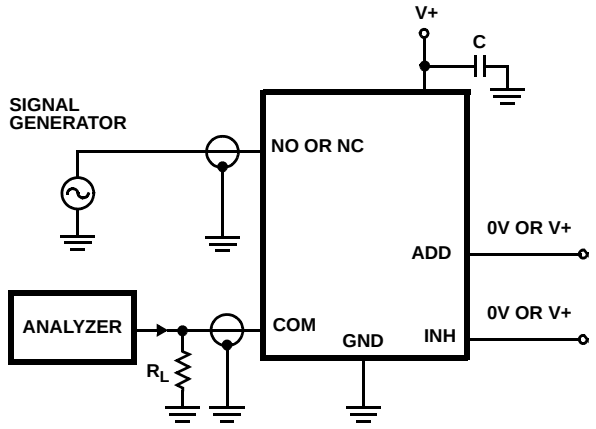


FIGURE 4. OFF-ISOLATION TEST CIRCUIT

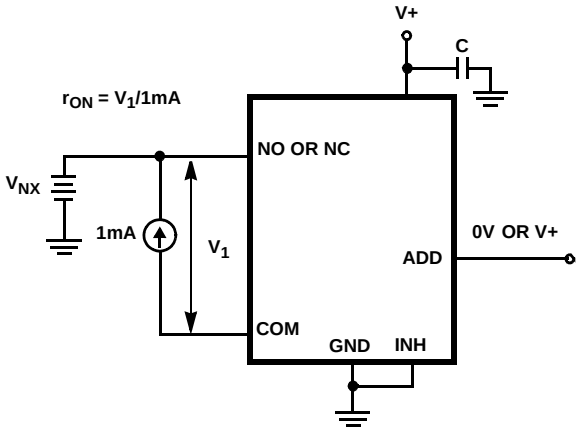


FIGURE 5. r_{ON} TEST CIRCUIT

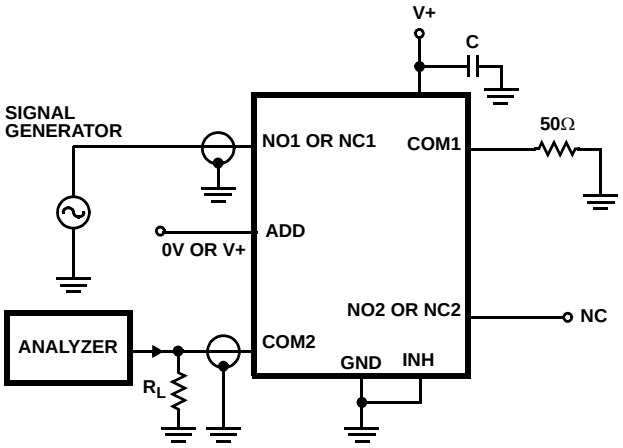


FIGURE 6. CROSSTALK TEST CIRCUIT

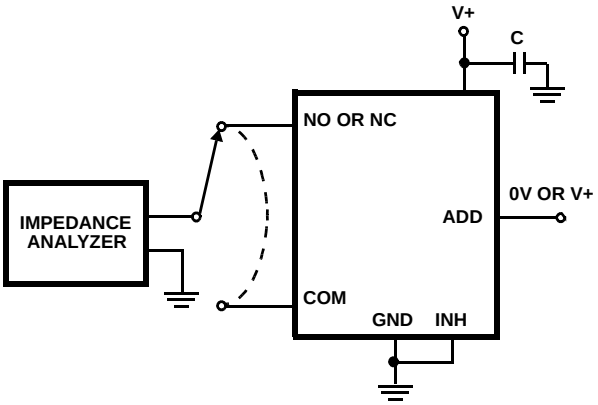


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Descriptions

The ISL43410 operates from a single 2V to 12V supply with low ON-resistance (115Ω) and high speed operation (t_{ON} = 60ns, t_{OFF} = 30ns). The ISL43410 is especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2.0V), low power consumption (3µW), low leakage currents (5nA max), and the tiny MSOP and QFN packaging. High frequency applications also benefit from the wide bandwidth, and the very high OFF-isolation (75dB) and crosstalk rejection (-85dB).

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

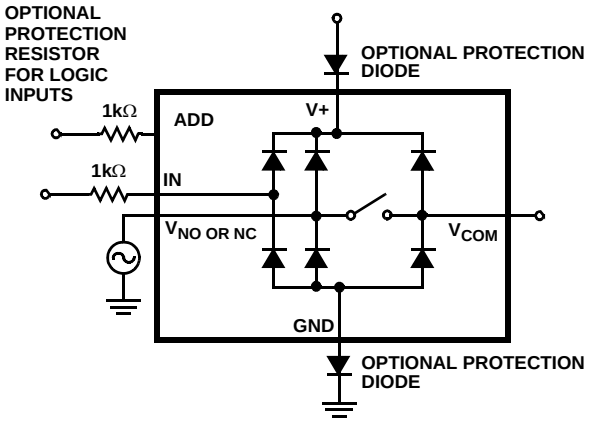


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43410 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL43410's 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.0V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the Electrical Specification" tables beginning on page 3 and "Typical Performance Curves" on page 10 for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This device cannot be operated with bipolar supplies because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

The ISL43410 is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V (see Figure 11). At 12V, the V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails (see Figure 12). Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL43410 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example, driving the device with 3V logic (0V to 3V) while operating with a 5V supply, the device draws only 10µA of current (see Figure 12 for V_{IN} = 3V). Similar devices of competitors can draw 8x this amount of current.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figure 17). Figure 17 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. OFF-Isolation is the resistance to this feed through, while crosstalk indicates the amount of feed through from one switch to another. Figure 18 details the high OFF-Isolation and crosstalk rejection provided by this family. At 10MHz, OFF-Isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease OFF-Isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified.

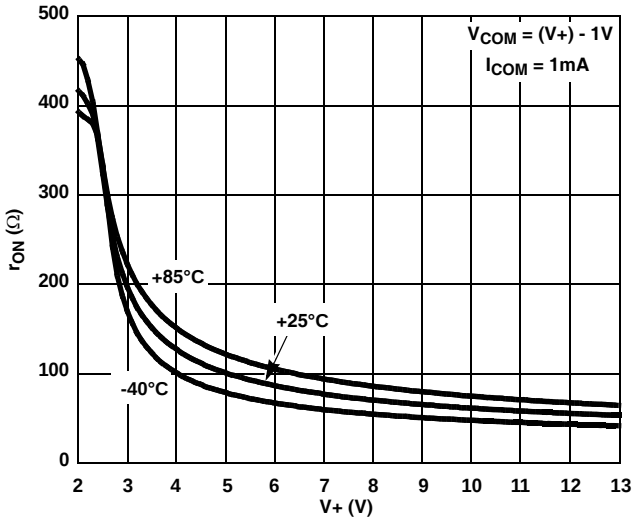


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE

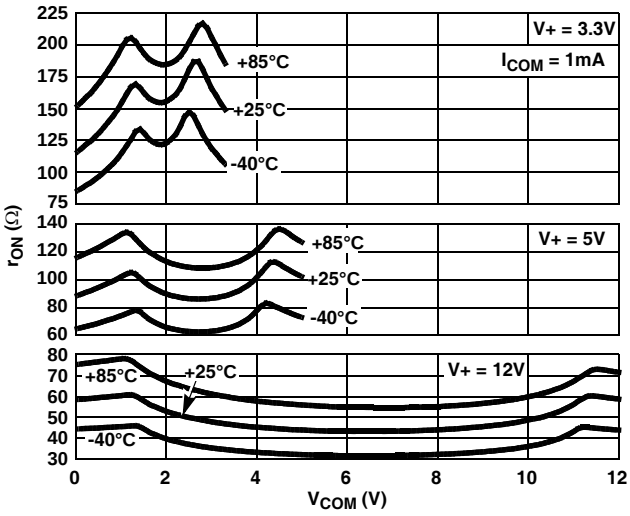


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

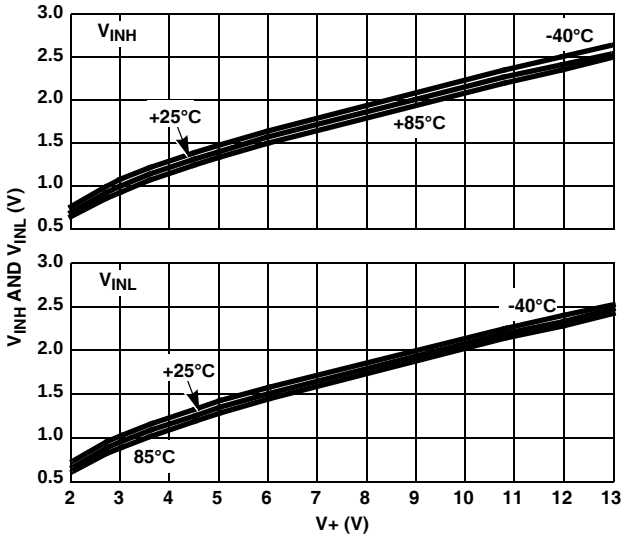


FIGURE 11. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

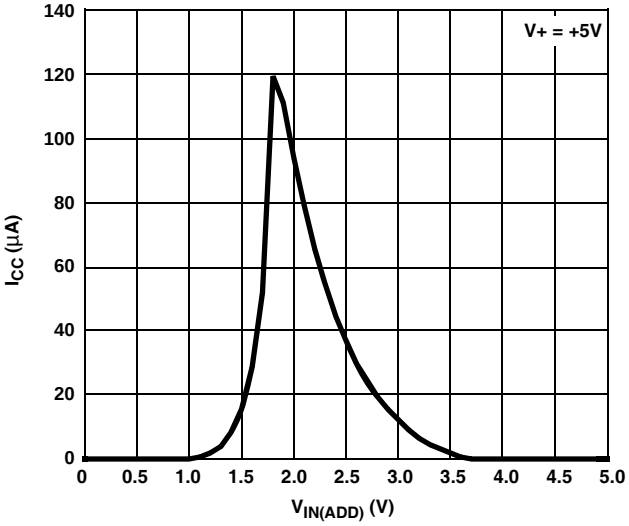


FIGURE 12. SUPPLY CURRENT vs DIGITAL ADDRESS INPUT VOLTAGE

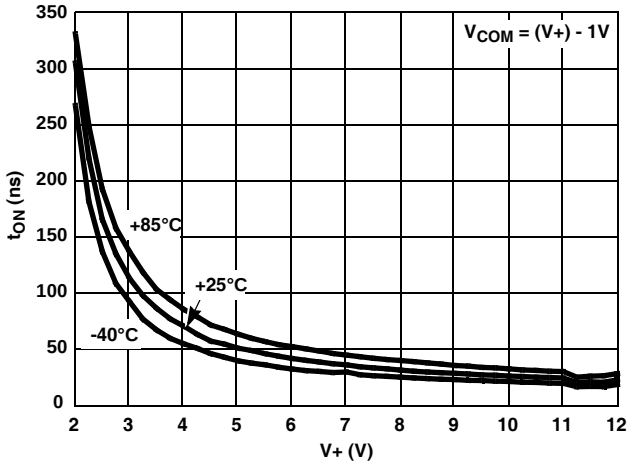


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

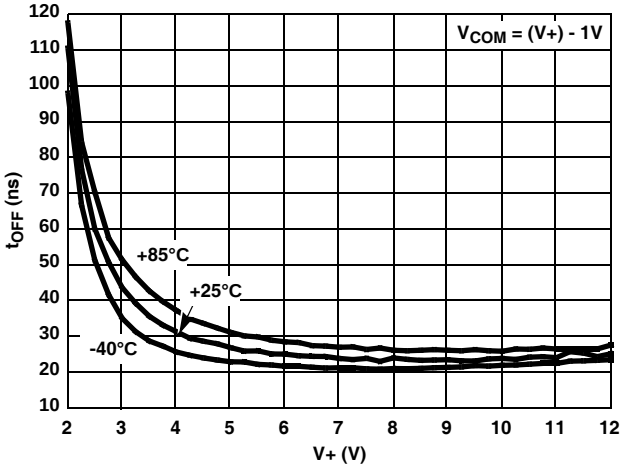


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

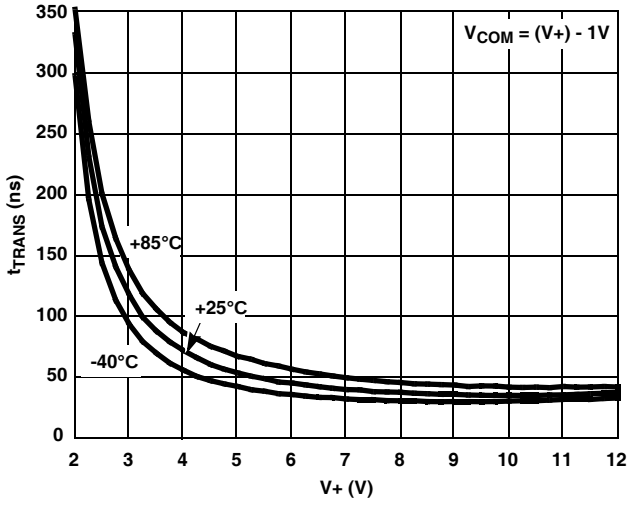


FIGURE 15. ADDRESS TRANS TIME vs SUPPLY VOLTAGE

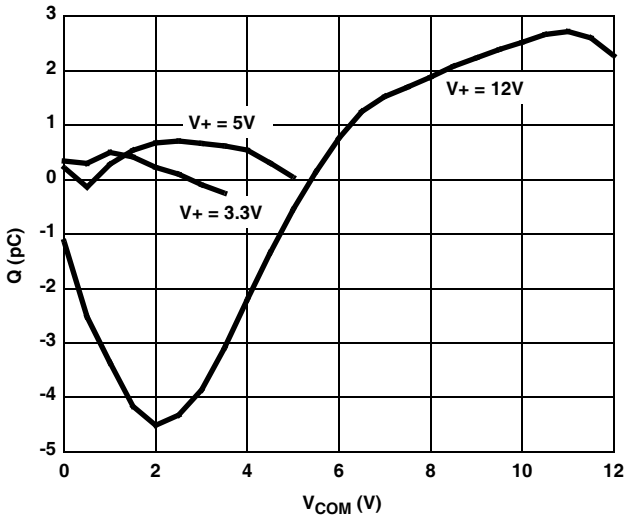


FIGURE 16. CHARGE INJECTION vs SWITCH VOLTAGE

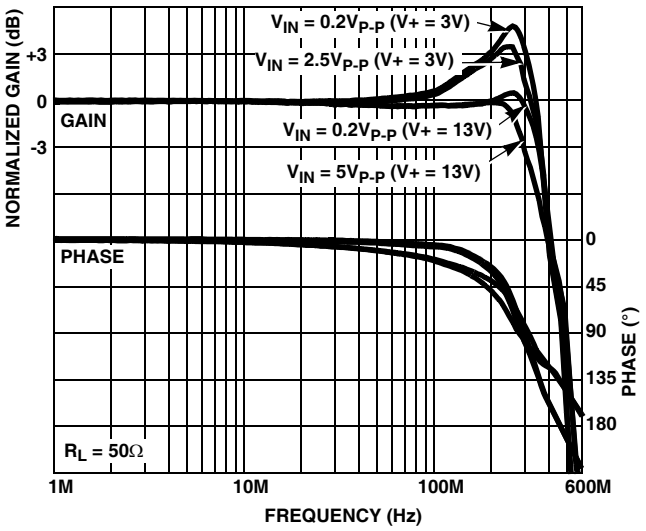


FIGURE 17. FREQUENCY RESPONSE

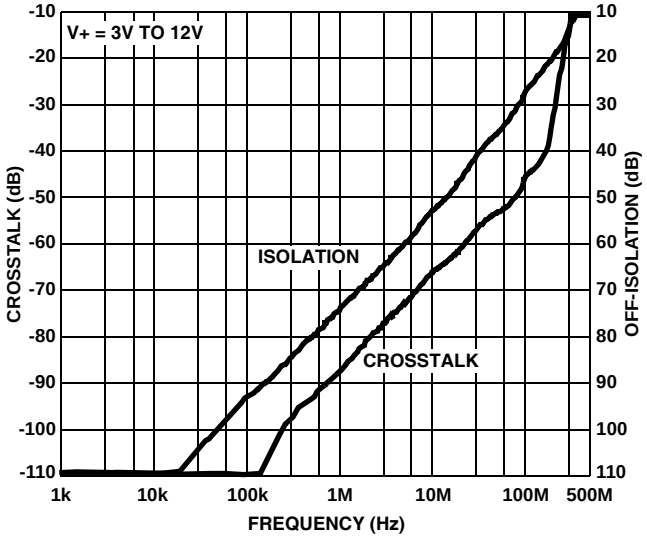


FIGURE 18. CROSSTALK AND OFF-ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

193

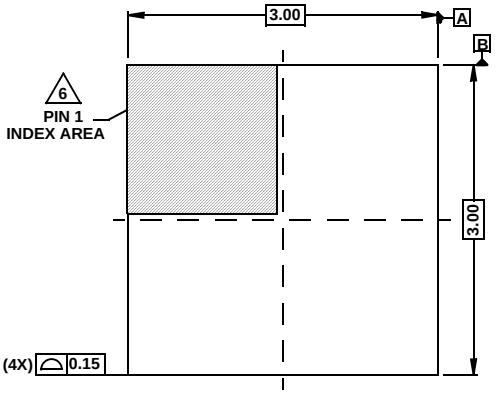
PROCESS:

Si Gate CMOS

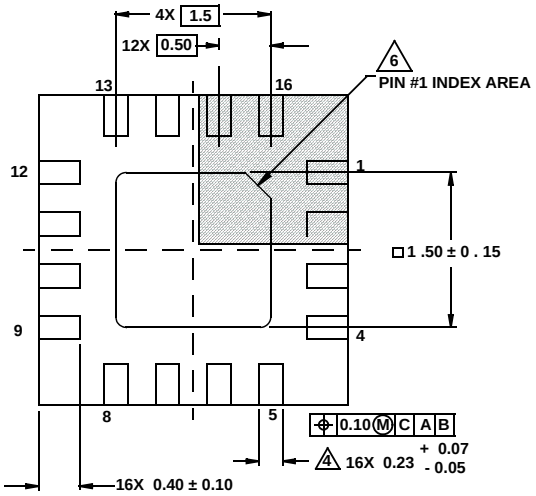
Package Outline Drawing

L16.3x3

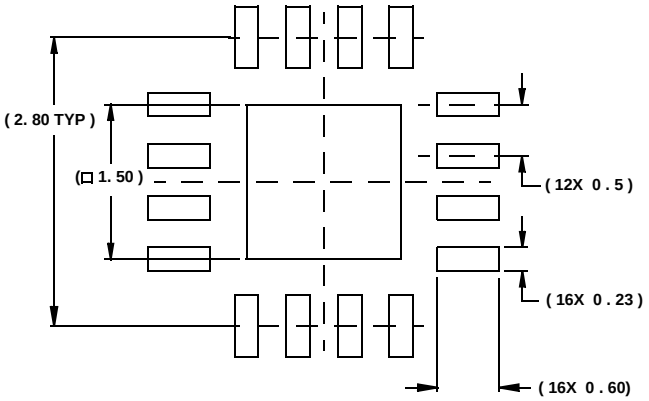
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 4/07



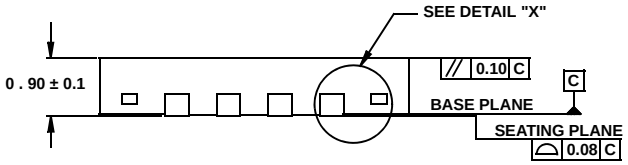
TOP VIEW



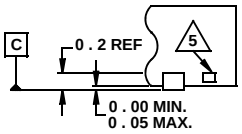
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

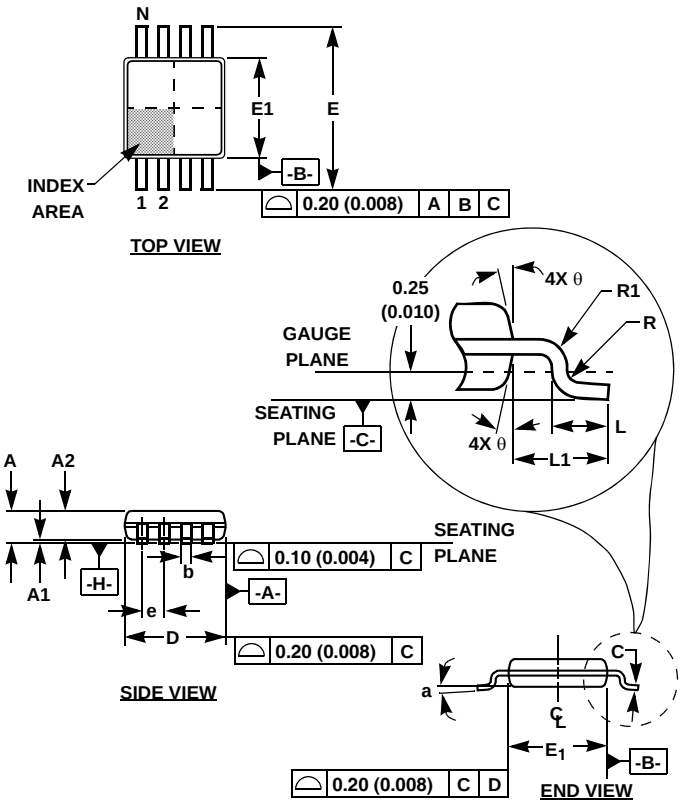


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only