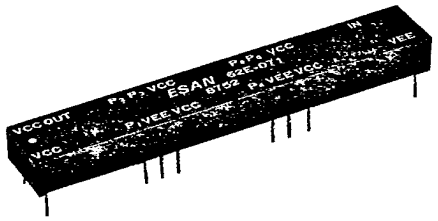
Programmable Delay Line (ECL Lok Series)

62E Series

- **48 Pin Dip Package**
- **Digitally Programmable in 64 Delay Steps (4 Bits)**



Specifications:

- Operating Temperature : −30°C to 85°C
- Temperature Coefficient : 500 ppm/°C
- Supply Voltage : −5.2V
- Logic 1 (output) : −.96V min
- Logic 1 Current : .26mA
- Logic 0 Current : .5μA
- Logic 0 (outpu) : −1.65 max
- Logic 1 (input) : −0.98V min
- Logic 0 (input) : −1.63V max
- Rise Time : 5ns max. (20% to 80%)
- Delay Tolerance : ±5% or 2ns whichever is greater
- Power Dissipation : 200mW Typ. (No Load)

MODEL NO.	ZERO STEP DELAY (ns)	MAX. DELAY (ns) (nom)	DELAY PER STEP (ns)
62E-071	8±2	71	1±0.5
62E-134	8±2	134	2±0.5
62E-197	8±2	197	3±0.6
62E-260	8±2	260	4±0.8
62E-323	8±2	323	5±1.0

Truth Table

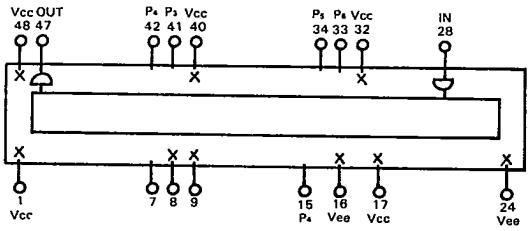
ADDRESS						DELAY
P_6	P_5	P_4	P_3	P_2	P_1	OUT
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{17}
1	0	0	0	0	0	T_{32}
1	1	1	1	1	1	T_{63}

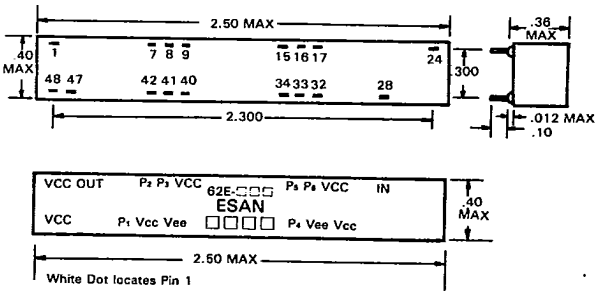
0 = Logic 1 = Logic 1
T_0 = Reference or inherent delay of unit.
$T_1 \rightarrow T_{63}$ = Multiplier of incremental delay.

Test Conditions:

- Temp. = 25°C Vee = 5.2VDC Vcc = Grd
- Input Pulse amplitude: 1.0V (−.75V H to −1.75 L)
- Pulse width : 3 * max Td
- Pulse spacing : 10 * max Td
- Time delay measured at the −1.3V level
- Output connected through on external pulldown resistor of 100Ω to −2 VDC

**Input pulse provided by a standard open emitter ECL 10K gate.





Unit: Inch