Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt218

20 MSPS Monolithic CMOS 8-bit Flash Video A/D Converter

Distinguishing Features

- 20 MSPS Operation
- Bt208 Pin Compatilibity
- No Video Amplifier Requirement
- ±1/4 LSB Typical DL Error
- ±1/2 LSB Typical IL Error
- External Zero and Clamp Control
- Overflow Output
- On-Chip Reference
- Output Enable Control
- TTL Compatiblility
- +5 V CMOS Monolithic Construction
- 24-pin 0.3" DIP or 28-pin PLCC Package
- Typical Power Dissipation: 500 mW

Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt252, Bt254
- Bt261

Product Description

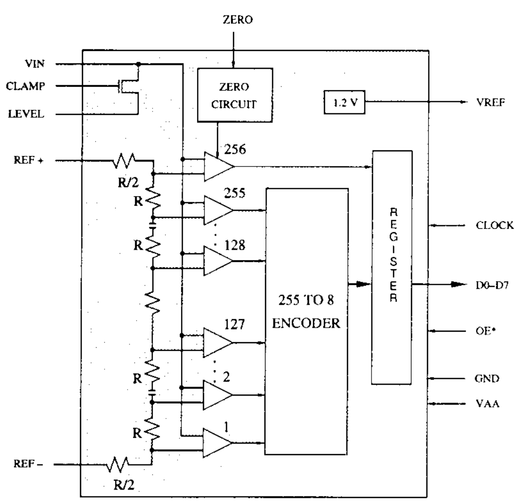
The Bt218 is an 8-bit flash A/D converter designed specifically for video digitizing applications. A flash converter topology is used with 256 high-speed comparators in parallel to digitize the analog input signal.

Flexible input ranges enable NTSC and CCIR video signals to be digitized without requiring a video amplifier.

The TTL-compatible output data and OVERFLOW are registered synchronously with the clock signal. The OE* three-states the D0–D7 outputs asynchronously to CLOCK.

The ZERO input is used to zero the comparators, while CLAMP allows DC restoration of an AC-coupled video signal (by forcing the VIN input to the voltage on the LEVEL pin).

Functional Block Diagram



Brooktree Corporation • 9950 Barnes Canyon Rd. • San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC • TLX: 383 596 • FAX: (619) 452-1249
L218001 Rev. C

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt218 contains 256 high-speed comparators, a 255-to-8 encoder, an output register, and a resistor divider network. Of the 256 comparators, 255 are used to digitize the analog signal; the additional comparator is used to generate the OVERFLOW bit.

General Operation

The Bt218 converts an analog signal in the range of REF– ≤ Vin ≤ REF+, generating a binary number from $00 to $FF, and an OVERFLOW output (see Table 1).

The values of REF+ and REF– are flexible to enable various video signals to be digitized without requiring a video amplifier. Refer to the Recommended Operating Conditions and Application Information sections for suggested configurations.

Figure 1 shows the input/output timing of the Bt218. The sample is taken following the falling edge of CLOCK. The binary data and OVERFLOW are registered and output onto the D0–D7 and OVERFLOW pins on the second rising edge of CLOCK.

Comparator Zeroing

The ZERO input is used to periodically zero the comparators. The comparators have an initial threshold mismatch caused by manufacturing tolerances. Zeroing charges capacitors in the comparators that offset this threshold mismatch. But because capacitors discharge, the comparators must be periodically zeroed.

While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, D0–D7 and OVERFLOW are not updated. They retain the data loaded before the ZERO cycle.

Input Signal Clamping

CLAMP and LEVEL are used only in applications where the video signal is AC coupled to VIN. While CLAMP is a logical one, the VIN input is forced to the voltage level of the LEVEL pin to DC restore the video signal.

In applications where the video signal is DC coupled to VIN, the LEVEL pin should float or be connected to VIN, or CLAMP should always be a logical zero (on the 28-pin PLCC package only) .

Vin (V) (Note 1)	Overflow	D0–D7	OE*
> 0.998	1	$FF	0
0.996	0	$FF	0
0.992	0	$FE	0
:	:	:	:
0.500	0	$81	0
0.496	0	$80	0
0.492	0	$7F	0
:	:	:	:
0.004	0	$01	0
< 0.002	0	$00	0
		3-state	1

Note 1: With REF+ = 1.000 V and REF– = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV.

Table 1. Output Coding Example.

Timing Waveforms

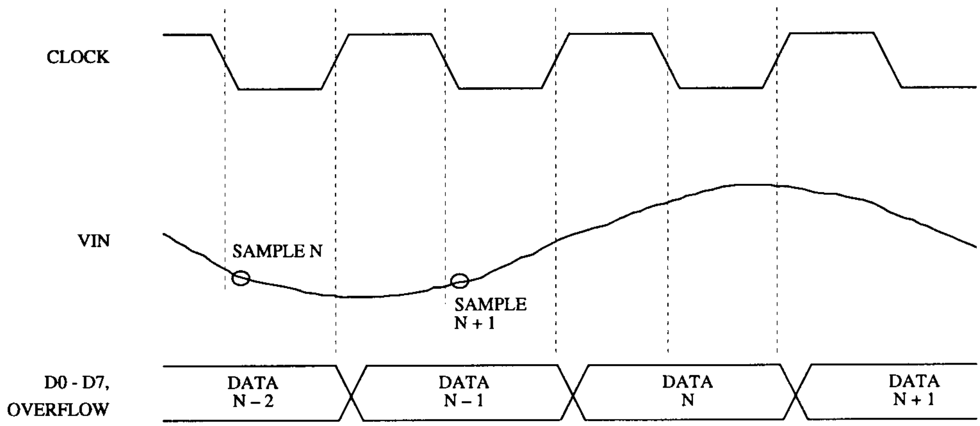


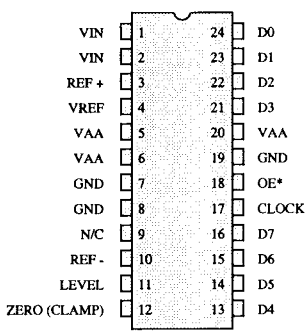
Figure 1. General Operation.

Pin Descriptions

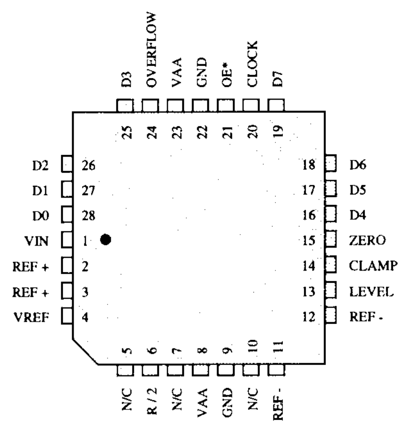
Pin Name	Description
D0–D7	Data outputs (TTL compatible). D0 is the least significant data bit. These outputs are latched and output following the second rising edge of CLOCK. Coding is binary. For optimum performance, D0–D7 should have minimal loading. If a large capacitive load is being driven, an external buffer is recommended.
OE*	Output enable control input (TTL compatible). Negating OE* three-states D0–D7 asynchronously. The OVERFLOW output is not affected by the state of OE*.
OVERFLOW	Overflow output (TTL compatible). OVERFLOW is latched and output following the second rising edge of CLOCK. OE* does not affect the OVERFLOW output signal. OVERFLOW is not available on the DIP package.
CLOCK	Clock input (TTL compatible). It is recommended that this pin be driven by a dedicated TTL buffer to minimize sampling jitter.
REF+	Top of ladder voltage reference (voltage input). REF+ sets the VIN voltage level that corresponds to $FF on the D0–D7 outputs. All REF+ pins must be connected together as close to the device as possible. For noise immunity reasons, a decoupling capacitor is not recommended on REF+.
REF–	Bottom of ladder voltage reference (voltage input). Typically, this input is connected to GND. REF– sets the VIN voltage level that corresponds to $00 on the D0–D7 outputs. All REF– pins must be connected together as close to the device as possible.
R/2	Midtap of reference ladder (voltage output). R/2 is not available on the DIP package. If not used, this pin should remain floating. If used, it should be buffered by a voltage follower. For noise immunity reasons, a decoupling capacitor is not recommended on R/2.
VIN	Analog signal inputs (voltage input). All VIN pins must be connected together as close to the device as possible.
ZERO/CLAMP	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators are zeroed and D0–D7 output data is held to the current state. ZERO is latched on the rising edge of CLOCK. On the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, zeroing and clamping occur simultaneously. Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN inputs are forced to the voltage level on the LEVEL pin to perform DC restoration of an AC-coupled video signal. CLAMP is asynchronous to clock. On the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, ZERO and CLAMP are asserted simultaneously.

Pin Descriptions *(continued)*

Pin Name	Description
LEVEL	Level control input (voltage input). This input is used to specify what voltage level is to be used for clamping while CLAMP is a logical one. LEVEL is used only to DC restore AC coupled video signals. In applications where the video signal is DC coupled to VIN, the LEVEL pin should float or be connected to VIN.
VREF	Voltage reference output pin. This pin provides a 1.2 V (typical) output. A decoupling capacitor is not recommended on VREF.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup. A 0.1 μF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup.



24-pin 0.3" DIP Package



28-pin Plastic J-Lead (PLCC) Package

Note: N/C pins are reserved and must remain floating.

PC Board Layout Considerations

PC Board Considerations

For optimum performance, before PCB layout is begun, the CMOS digitizer layout examples in the Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements, Application Notes AN-13, 14, and 15, respectively, should be studied. These application notes can be found in the Brooktree Applications Handbook.

The layout should be optimized for lowest noise on the Bt218 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

A single ground plane covering both digital and analog logic should be used.

Power Planes

The Bt218 and any associated analog circuitry should have their own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt218.

The regular PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt218 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that the regular PCB power plane does not overlay the analog power plane.

Supply Decoupling

The bypass capacitors should be installed with the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

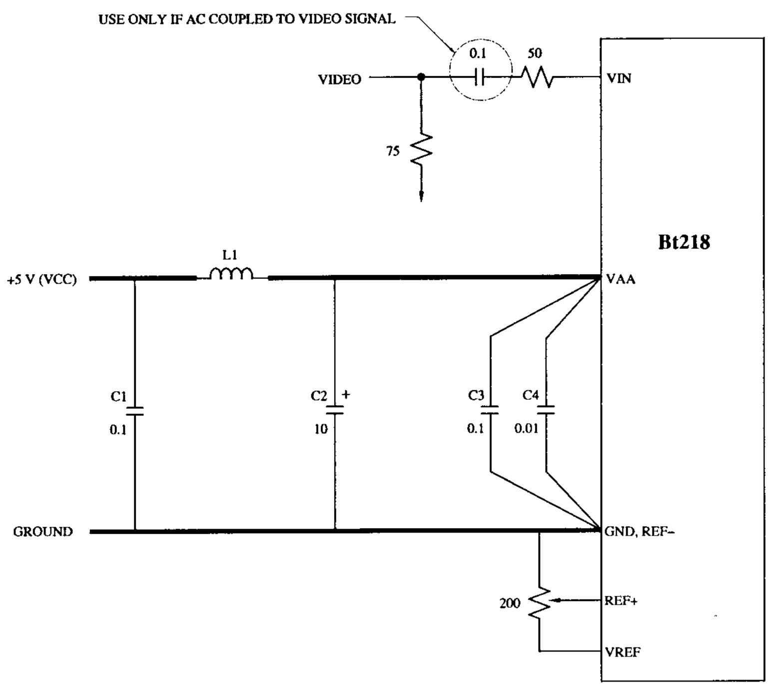
Each group of VAA and GND pins should have a 0.1 µF ceramic chip capacitor located as close as possible to the device pins. The capacitors should be connected directly to the VAA and GND pins with short, wide traces.

Signal Interconnect

The digital signals of the Bt218 must be isolated as much as possible from the analog inputs and other analog circuitry to prevent crosstalk. Also, these digital signals should not overlay the analog power plane.

Termination resistors for the digital signals should be connected to the digital PCB power and ground planes.

PC Board Layout Considerations *(continued)*



Location	Description	Vendor Part Number
C1, C3	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2	10 µF capacitor	Mallory CSR13G106KM
C4	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt218.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

Using the Internal Reference

The Bt218 has a 1.2 V on-chip reference available (VREF). VREF may be divided down and used to drive the REF+ input, as shown in Figure 2. The 200 Ω potentiometer serves three purposes: to allow adjustment for different video signal levels, to allow for video level tolerances, and to adjust for tolerance of the internal reference.

VREF should supply at least 6 mA of current to maintain voltage stability over temperature. Thus, VREF should drive a resistive load between 90 and 240 Ω.

Using An External Reference

Figure 3 illustrates the use of a 1.2 V LM385 and a TLC272 to generate a 0–1.2 V reference for applications that require a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that can operate from a single +5 V supply.

To prevent ringing in the TLC272 from clock kickback, a 100 Ω resistor is recommended, as shown in Figure 3. If an op-amp is chosen that has a better transient response than the TLC272, the resistor may not be needed. This circuit may also be used to drive the Ref– if a value other than ground is desired. Because single-supply op-amps are limited, Ref– may not be set below ~300 mV. To drive Ref– to true 0 V in the op-amp configuration, a dual supply must be used. *Extreme care must be used in power sequencing to ensure all positive supplies (op-amp and A/D) power on before the negative supply. This will prevent latchup of the A/D.*

AC-Coupled vs. DC-Coupled Input

The Bt218 may be either AC or DC coupled to the video signal, as shown in Figure 2. The 75 Ω resistor to ground provides the typical 75 Ω termination required by video signals. The 50 Ω resistor provides isolation from any clock kickback noise on VIN and prevents it from being coupled onto the video signal. If the Bt218 is DC coupled to the video signal, the 0.1 µF capacitor is not used and CLAMP should be grounded.

Zeroing

Unlike many CMOS A/D converters requiring the comparators to be zeroed every clock cycle, the comparators in the Bt218 are designed to be only periodically zeroed. It is convenient to assert ZERO during each horizontal blanking interval.

Before the Bt218 is used after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent because of the number of horizontal scan lines that will have occurred before the Bt218 was used.

While the recommended zeroing interval is maintained, the Bt218 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

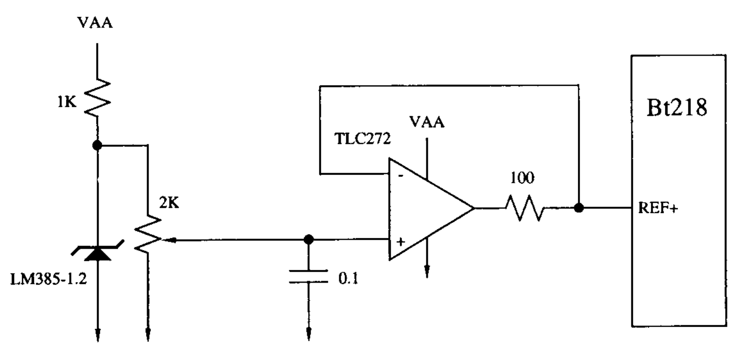


Figure 3. Using an External Reference.

Application Information *(continued)*

Input Ranges

Table 2 lists some common video signal amplitudes. If a signal may possibly exceed 1.2 V, it should be attenuated (with a resistor divider network) so as not to exceed the 1.2 V input range.

When a full-scale range less than 0.7 V is used to digitize, the Bt218's integral linearity errors are constant in terms of voltage, regardless of the value of the reference voltage. Lower reference voltages will, therefore, produce larger integral linearity errors in terms of LSBs.

For example, with a reference difference of 0.6 V, 0.6 V video signals may be digitized. However, the Integral Linearity (IL) error will increase to about ±1.8 LSB, and the SNR will be about 40 db. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB, and the SNR will be about 39 db.

Output Noise

Although the Bt218 does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth (see the AC Characteristics section). Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 641746–2 for the PLCC package.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors can cause a power supply time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 2. Video Signal Tolerances.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.00	5.5	V
Voltage References					
Top	REF+	0.7	1	2.0	V
Bottom	REF–	0	0	1.3	V
Difference (Top–Bottom)		0.7	1	1.2	V
Input Amplitude Range		0.7	1	1.2	V
Analog Input Range			REF– to REF+		V
LEVEL Input Voltage		GND–0.5	REF–	REF+	V
Time between Zeroing Intervals			60	150	µs
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Input Voltage		GND–0.5		VAA + 0.5	V
R/2 Output Current				25	µA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error (Note 1)	IL		±0.5	±1	LSB
Differential Linearity Error	DL		±0.25	±1	LSB
Output Noise (Note 2)			±1		LSB
Coding					Binary
No Missing Codes			guaranteed		
VIN Analog Inputs (Note 3)					
CLAMP = 0					
Input Current (Leakage)	IB			1	µA
Input Capacitance	CAIN		35		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
REF+ Reference Input					
Input Impedance	RREF+		500		Ω
Digital Inputs					
Input High Voltage	VIH	2.0			V
Input Low Voltage	VIL			0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = –50 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Three-State Current	IOZ			10	µA
Output Capacitance	COUT			10	pF
Internal Voltage Reference	VREF		1.2		V
Regulation (at 6 mA)			5		mV
Output Current	IREF			15	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, and LEVEL = float. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Using best-fit linearity (offset independent).
Note 2: Clock duty cycle adjusted for minimum output noise for a DC input. For a DC input, output noise may increase if clock duty cycle is not adjusted.
Note 3: LEVEL = GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			20	MHz
Clock Cycle Time (Figure 4)	1	50			ns
Clock Low Time	2	20			ns
Clock High Time	3	20			ns
Data Output Delay Time (Figure 5)	4			40	ns
Data Output Hold Time	5	9			ns
OE* Asserted to D0–D7 Valid	6			25	ns
OE* Negated to D0–D7 3-Stated	7			25	ns
ZERO Setup Time	8	0			ns
ZERO Hold Time	9	20			ns
ZERO, CLAMP High Time (Note 1)		1			Clock
Aperture Delay	10		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW			Fs/2	MHz
Transient Response (Note 2)			1		Clock
Overload Recovery (Note 3)			1		Clock
Zero Recovery Time (Note 4)			1		Clock
RMS Signal-to-Noise Ratio	SNR				
Fin = 4.20 MHz, Fs = 12.27 MHz			44		db
Fin = 4.20 MHz, Fs = 13.50 MHz			44		db
Fin = 4.20 MHz, Fs = 14.32 MHz			44		db
Fin = 5.75 MHz, Fs = 13.50 MHz			43		db
Fin = 5.75 MHz, Fs = 14.75 MHz			43		db
Fin = 5.75 MHz, Fs = 17.72 MHz			43		db
Fin = 10.0 MHz, Fs = 20.00 MHz			39		db
RMS Signal & Distortion-to-Noise Ratio	SINAD				
Fin = 4.20 MHz, Fs = 12.27 MHz			42		db
Fin = 4.20 MHz, Fs = 13.50 MHz			42		db
Fin = 4.20 MHz, Fs = 14.32 MHz			42		db
Fin = 5.75 MHz, Fs = 13.50 MHz			41		db
Fin = 5.75 MHz, Fs = 14.75 MHz			41		db
Fin = 5.75 MHz, Fs = 17.72 MHz			41		db
Fin = 10.0 MHz, Fs = 20.00 MHz			37		db
Total Harmonic Distortion	THD				
Fin = 4.20 MHz, Fs = 12.27 MHz			47		db
Fin = 4.20 MHz, Fs = 13.50 MHz			47		db
Fin = 4.20 MHz, Fs = 14.32 MHz			47		db
Fin = 5.75 MHz, Fs = 13.50 MHz			47		db
Fin = 5.75 MHz, Fs = 14.75 MHz			47		db
Fin = 5.75 MHz, Fs = 17.72 MHz			47		db
Fin = 10.0 MHz, Fs = 20.00 MHz			44		db

See test conditions and notes on next page.

AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Spurious Free Dynamic Range	SFDR				
Fin = 4.20 MHz, Fs = 12.27 MHz			50		db
Fin = 4.20 MHz, Fs = 13.50 MHz			50		db
Fin = 4.20 MHz, Fs = 14.32 MHz			50		db
Fin = 5.75 MHz, Fs = 13.50 MHz			50		db
Fin = 5.75 MHz, Fs = 14.75 MHz			50		db
Fin = 5.75 MHz, Fs = 17.72 MHz			50		db
Fin = 10.0 MHz, Fs = 20.00 MHz			47		db
Differential Gain Error (Note 5)	DG		2		%
Differential Phase Error (Note 5)	DP		1		Degree
Supply Current (Note 6) (Excluding REF+)	IAA		100	160	mA
Pipeline Delay (Note 7)		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF–≤ Vin≤ REF+ and, LEVEL = float. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 1.5 V for digital inputs and outputs. D0–D7 and OVERFLOW output load ≤ 40 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, and Fs = 14.32 MHz, T_{CASE} = Ambient.
IAA (max) at VAA = 5.5 V, Fin = 10 MHz, and Fs = 20 MHz, T_{CASE} = 0° C.
Note 7: Pipeline delay is defined as discrete clock period delays in addition to the half-cycle analog sampling delay.

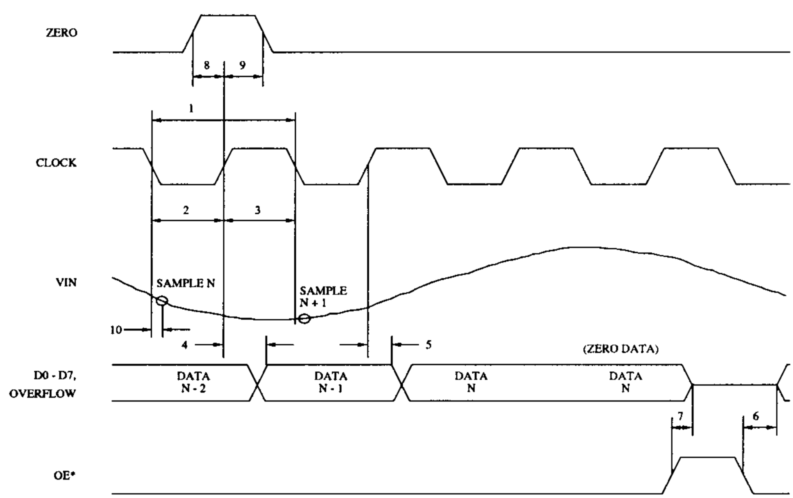
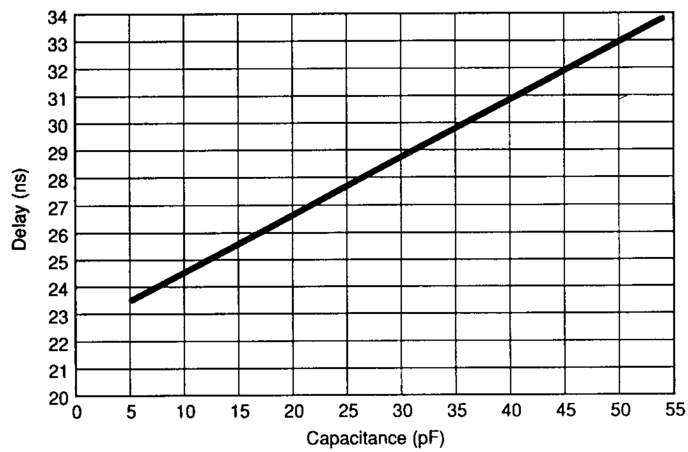


Figure 4. Input/Output Timing.

AC Characteristics *(continued)*



Note: Nominal device at ambient, timing reference points = 1.4 V

Figure 5. Bt218KPJ Output Delay vs. Capacitive Loading.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt218KP20	20 MHz	24-pin 0.3" Plastic DIP	0° to +70° C
Bt218KPJ20	20 MHz	28-pin Plastic J-Lead	0° to +70° C
Bt218EVM	Evaluation Board for the Bt218KP. Includes a Bt218KP30.		