2–Input NOR Gate

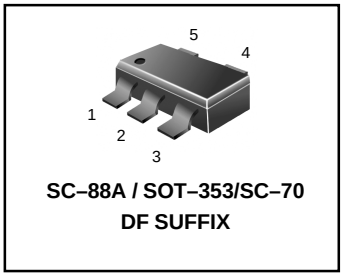
L74VHC1G02

The L74VHC1G02 is an advanced high speed CMOS 2–input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

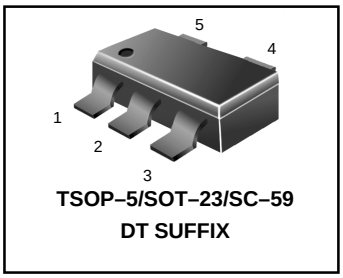
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The L74VHC1G02 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the L74VHC1G02 to be used to interface 5 V circuits to 3 V circuits.

- High Speed: t_{PD} = 3.0 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 mA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 56; Equivalent Gates = 14

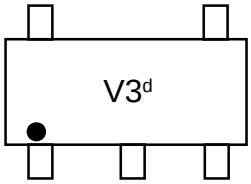


SC–88A / SOT–353/SC–70
DF SUFFIX

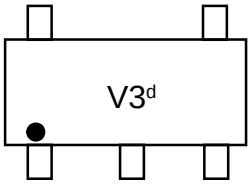


TSOP–5/SOT–23/SC–59
DT SUFFIX

MARKING DIAGRAMS



Pin 1
d = Date Code



Pin 1
d = Date Code

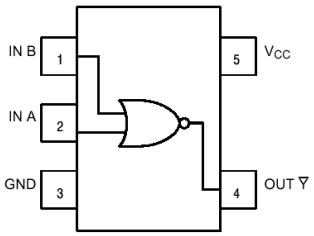


Figure 1. Pinout (Top View)

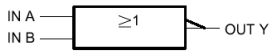


Figure 2. Logic Symbol

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	V_{CC}

FUNCTION TABLE

Inputs		Output
A	**B**	**$\overline{Y}$**
L	L	H
L	H	L
H	L	L
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

L74VHC1G02

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage		– 0.5 to 7.0	V
V_{OUT}	DC Output Voltage	V_{CC}=0	– 0.5 to 7.0	V
		High or Low State	–0.5 to V_{CC} + 0.5	
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current	V_{OUT} < GND; V_{OUT} > V_{CC}	+20	mA
I_{OUT}	DC Output Current, per Pin		+ 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+50	mA
P_D	Power dissipation in still air	SC–88A, TSOP–5	200	mW
θ_{JA}	Thermal resistance	SC–88A, TSOP–5	333	°C/W
T_L	Lead Temperature, 1 mm from Case for 10 s		260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
T_{stg}	Storage temperature		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2)	>2000	V
		Machine Model (Note 3)	> 200	
		Charged Device Model (Note 4)	N/A	
$I_{LATCH-UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22–A114–A
3. Tested to EIA/JESD22–A115–A
4. Tested to JESD22–C101–A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage		0.0	5.5	V
V_{OUT}	DC Output Voltage		0.0	V_{CC}	V
T_A	Operating Temperature Range		– 55	+ 125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 ± 0.3 V	0	100	ns/V
		V_{CC} = 5.0 ± 0.5 V	0	20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

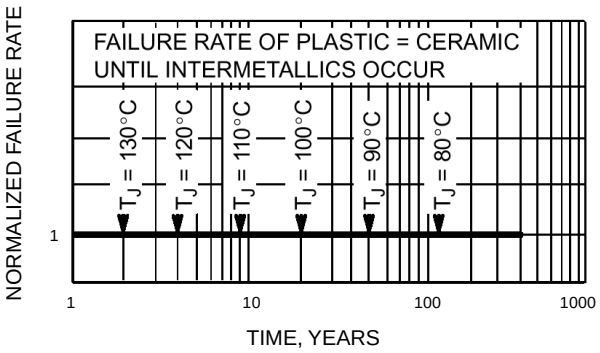


Figure 3. Failure Rate vs. Time Junction Temperature

L74VHC1G02

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	−55°C≤T_A≤125°C Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0	1.5			1.5		1.5		V
			3.0	2.1			2.1		2.1		
			4.5	3.15			3.15		3.15		
			5.5	3.85			3.85		3.85		
V_{IL}	Maximum Low–Level Input Voltage		2.0			0.5		0.5		0.5	V
			3.0			0.9		0.9		0.9	
			4.5			1.35		1.35		1.35	
			5.5			1.65		1.65		1.65	
V_{OH}	Minimum High–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = – 50 µA	2.0	1.9	2.0		1.9		1.9		V
			3.0	2.9	3.0		2.9		2.9		
			4.5	4.4	4.0		4.4		4.4		
		V_{IN} = V_{IH} or V_{IL}									
		I_{OH} = –4 mA	3.0	2.58			2.48		2.34		
		I_{OH} = –8 mA	4.5	3.94			3.80		3.66		
V_{OL}	Maximum Low–Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 µA	2.0		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
			4.5		0.0	0.1		0.1		0.1	
		V_{IN} = V_{IH} or V_{IL}									
		I_{OL} = 4 mA	3.0			0.36		0.44		0.52	
		I_{OL} = 8 mA	4.5			0.36		0.44		0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		20		40	µA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T_A = 25°C Min	Typ	Max	$T_A \leq$ 85°C Min	Max	−55°C≤T_A≤125°C Min	Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Y	V_{CC} = 3.3± 0.3 V C_L = 15 pF		4.0	7.9		9.5		11.0	ns
		C_L = 50 pF		5.4	11.4		13.0		15.5	
		V_{CC} = 5.0± 0.5 V C_L = 15 pF		3.0	5.5		6.5		8.0	
		C_L = 50 pF		3.8	7.5		8.5		10.0	
C_{IN}	Maximum Input Capacitance			5.5	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = C_{PD} • V_{CC} • f_{in} + I_{CC} . C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC} .

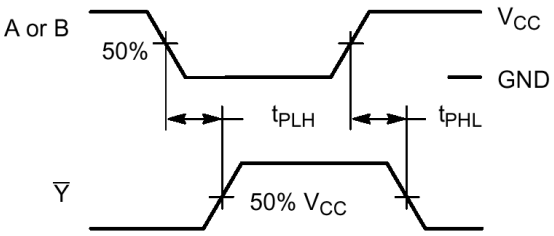
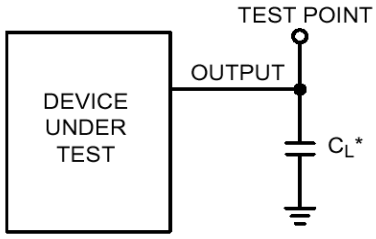


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

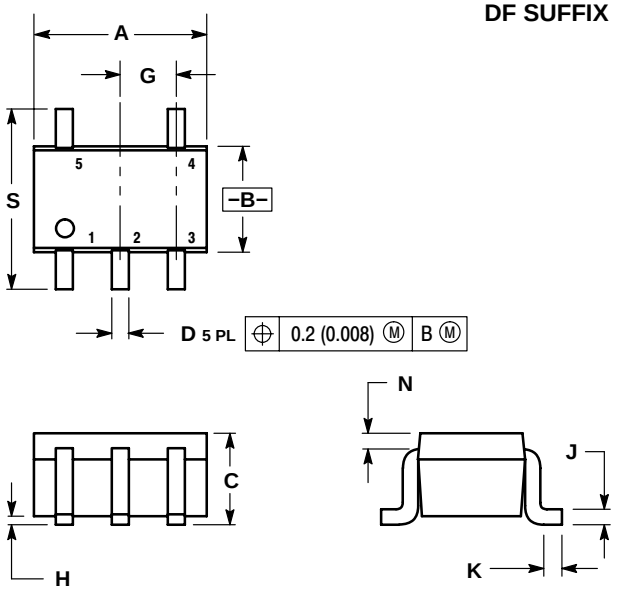
Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
L74VHC1G02DFT1	L	74	VHC1G	02	DF	T1	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
L74VHC1G02DFT2	L	74	VHC1G	02	DF	T2	SC–70/SC–88A/ SOT–353	178 mm (7 in) 3000 Unit
L74VHC1G02DFT4	L	74	VHC1G	02	DF	T4	SC–70/SC–88A/ SOT–353	330 mm (13 in) 10,000 Unit
L74VHC1G02DTT1	L	74	VHC1G	02	DT	T1	SOT–23/TSOPS/ SC–59	178 mm (7 in) 3000 Unit
L74VHC1G02DTT3	L	74	VHC1G	02	DT	T3	SOT–23/TSOPS/ SC–59	330 mm (13 in) 10,000 Unit

PACKAGE DIMENSIONS

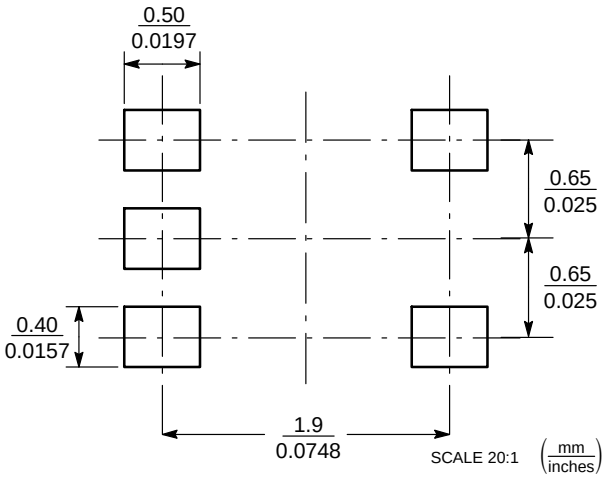
SC70−5/SC−88A/SOT−353
DF SUFFIX



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

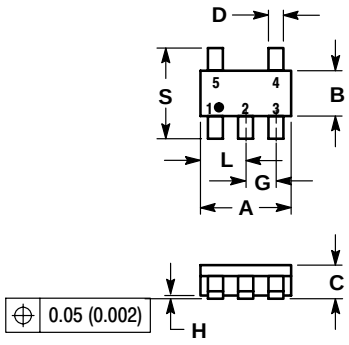
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

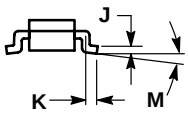
SOLDERING FOOTPRINT*



PACKAGE DIMENSIONS

SOT23−5/TSOP−5/SC59−5
DT SUFFIX





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*