1 PRODUCT OVERVIEW

OVER VIEW

The S3C7031/7032 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core.

With comparator inputs, high-current LED direct-drive pins, serial I/O interface, and a versatile 8-bit timer/counter, the S3C7031/7032 offers an excellent design solution for a wide range of applications such as mouse controllers, subsystem controllers, and toys.

Up to 15 pins of the 20-pin DIP or 20-pin SOP package can be dedicated to I/O. Pull-up resistors are assignable to all of the pins by software. Four vectored interrupts provide fast response to internal and external events.

In addition, the S3C7031/7032's advanced CMOS technology provides for very low power consumption and a wide operating voltage range.

DEVELOPMENT SUPPORT

The Samsung Microcontroller Development System, SMDS, provides you with a complete PC-based development environment for KS57-series microcontrollers that is powerful, reliable, and portable. In addition to its easy to use window-oriented program development structure, the SMDS toolset includes versatile debugging, trace, instruction timing, and performance measurement applications.

The Samsung Generalized Assembler (SAMA) has been designed specifically for the SMDS environment and accepts assembly language sources in a variety of microprocessor formats.

SAMA generates industry-standard object files that also contain program control data for SMDS compatibility.

FEATURES

Memory

— 1024 × 8-bit program memory (S3C7031) (ROM)

— 2048 × 8-bit program memory (S3C7032) (ROM)

— 128 × 4-bit data memory (S3C7031) (RAM)

— 256 × 4-bit data memory (S3C7032) (RAM)

I/O Pins

— Up to 15 pins for 20-DIP and 20-SOP package

Comparator Inputs

— 4-channel mode
Internal reference: 4-bit resolution

— 3-channel mode
External reference

8-Bit Basic Timer

— Programmable interval timer

8-Bit Timer/Counter

— Programmable interval timer

— External event counter function

— Timer clock output to TIO pin

Watch Timer

— Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz

— Four frequency outputs to BUZ pin

Bit Sequential Carrier

— 16-bit serial data transfer in arbitrary format

8-Bit Serial I/O Interface

— 8-bit transmit/receive mode

— 8-bit receive-only mode

— LSB-first or MSB-first transmission selectable

— Internal or external clock source

Interrupts

— One external interrupt vector

— Three internal interrupt vectors

— Two quasi-interrupts

Memory-Mapped I/O Structure

Two Power-Down Modes

— Idle mode: Only the CPU clock stops

— Stop mode: Main system clock stops

On-Chip Crystal, Ceramic, Or RC Oscillator

— Crystal/ceramic: 4.19 MHz (typical)

— RC: 1 MHz (typical)

— CPU clock divider circuit (by 4, 8, or 64)

Frequency Outputs

— Eight frequency outputs to the CLO pin

Instruction Execution Times

— 0.95, 1.91, 15.3 µs at 4.19 MHz (5 V),
4 µs at 1 MHz (2.7 V)

Operating Temperature:

— – 40°C to 85°C

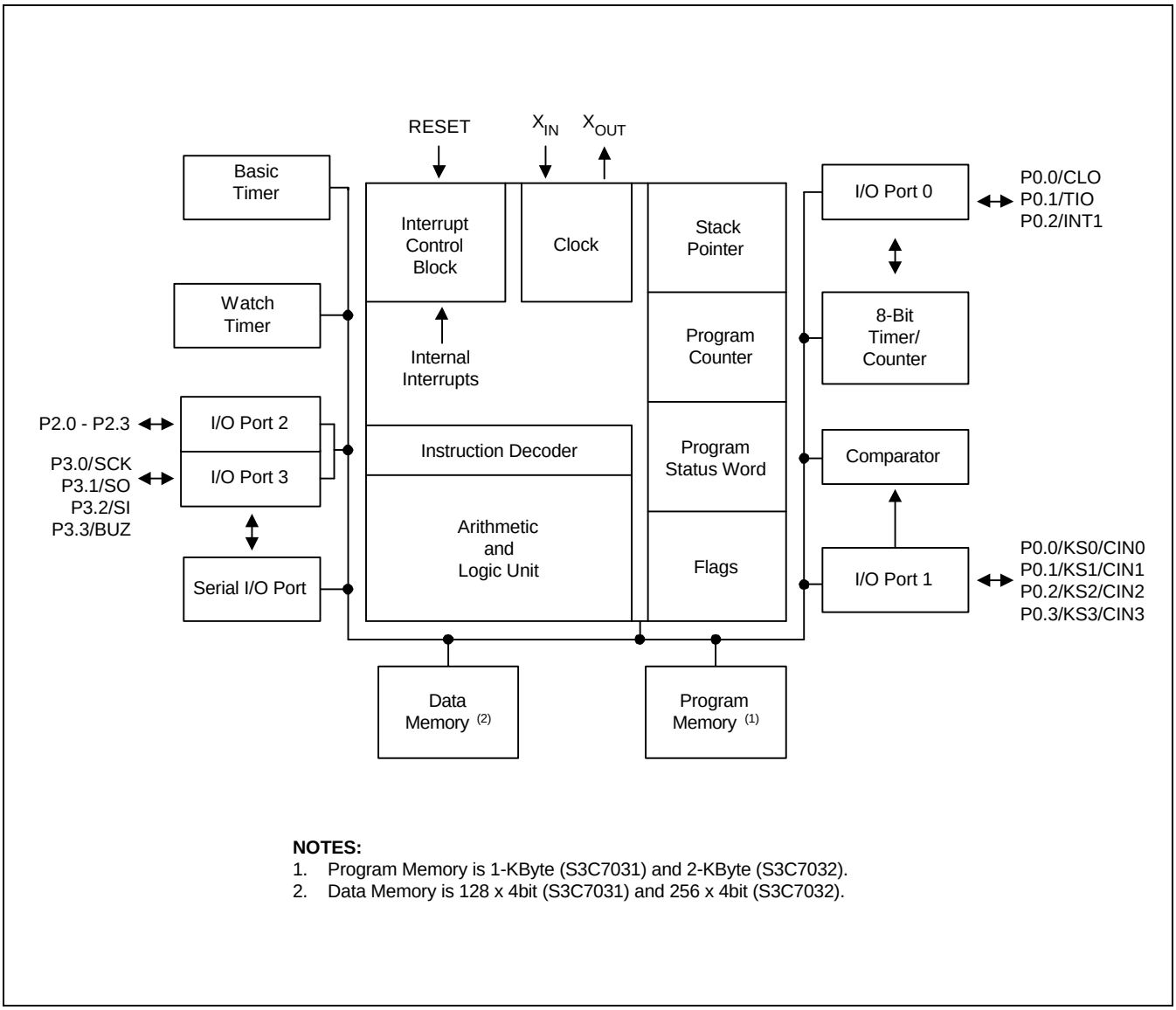
Operating Voltage Range:

— 2.7 V to 6.0 V

Package Type:

— 20-DIP, 20-SOP

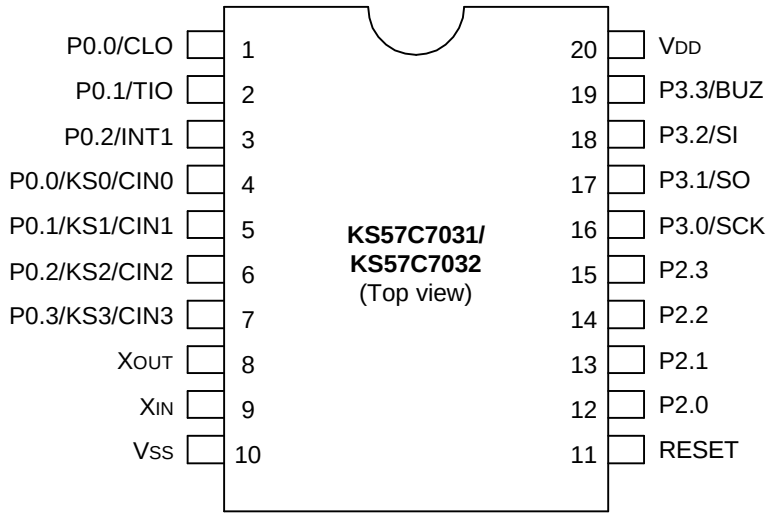
BLOCK DIAGRAM



NOTES:
1. Program Memory is 1-KByte (S3C7031) and 2-KByte (S3C7032).
2. Data Memory is 128 x 4bit (S3C7031) and 256 x 4bit (S3C7032).

Figure 1-1. S3C7031/7032 Block Diagram

PIN ASSIGNMENTS



NOTE: Pin assignments are identical for the 20-pin DIP and SOP package.

Figure 1-2. S3C7031/7032 Pin Assignment Diagram (20-pin DIP/SOP Package)

PIN DESCRIPTIONS

Table 1-1. S3C7031/7032 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2	I/O	3-bit I/O port. 1-bit or 3-bit read/write and test is possible. Pull-up resistors are individually assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	1 2 3	CLO TIO INT1
P1.0 P1.1 P1.2 P1.3	I/O	Same as port 0 except that port 1 is a 4-bit I/O port.	4 5 6 7	KS0/CIN0 KS1/CIN1 KS2/CIN2 KS3/CIN3

Table 1-1. S3C7031/7032 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
P2.0-P2.3 P3.0 P3.1 P3.2 P3.3	I/O	4-bit I/O port. 1-bit, 4-bit or 8-bit read/write and test is possible. Pins are individually configurable as input or output. Pull-up resistors are individually assignable to input pins by software and are automatically disabled for output pins. Ports are software configurable as n-channel open-drain outputs or push-pull output by software. Ports 2 and 3 can be paired to enable 8-bit data transfer.	12-15 16 17 18 19	–- SCK SO SI BUZ
CLO	I/O	Eight frequency outputs	1	P0.0
TIO	I/O	External clock input or timer clock output	2	P0.1
INT1	I/O	External interrupts with rising or falling edge detection	3	P0.2
KS0-KS3	I/O	Quasi-interrupts with falling edge detection	4-7	P1.0-P1.3
CIN0-CIN3	I/O	4-channel comparator input. CIN0-CIN2: comparator input only. CIN3: comparator input or external reference input	4-7	P1.0-P1.3
SCK	I/O	Serial interface clock signal	16	P3.0
SO	I/O	Serial data output	17	P3.1
SI	I/O	Serial data input	18	P3.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound	19	P3.3
X_{IN}, X_{OUT}	–-	Crystal, ceramic, or RC signal for system clock	9, 8	–-
RESET	I	Reset signal	11	–-
V_{DD}	–-	Power supply	20	–-
V_{SS}	–-	Ground	10	–-

Table 1-2. Overview of S3C7031/7032 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1-3	P0.0-P0.2	CLO, TIO, INT1	I/O	Input	2
4-7	P1.0-P1.3	KS0/CIN0-KS3/CIN3	I/O	Input	4
12-5	P2.0-P2.3	–	I/O	Input	3
16-19	P3.0-P3.3	SCK, SO, SI, BUZ	I/O	Input	3
11	RESET	–-	I	–-	1
20, 10	V_{DD}, V_{SS}	–-	–-	–-	–-
9, 8	X_{IN}, X_{OUT}	–-	–-	–-	–-

PIN CIRCUIT DIAGRAMS

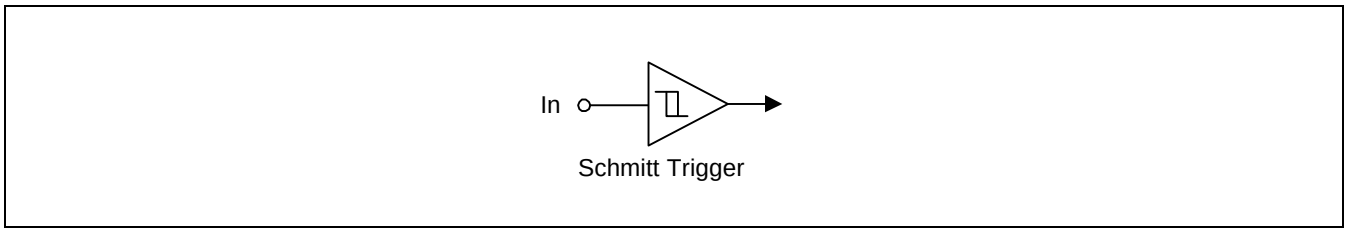


Figure 1-3. Pin Circuit Type 1

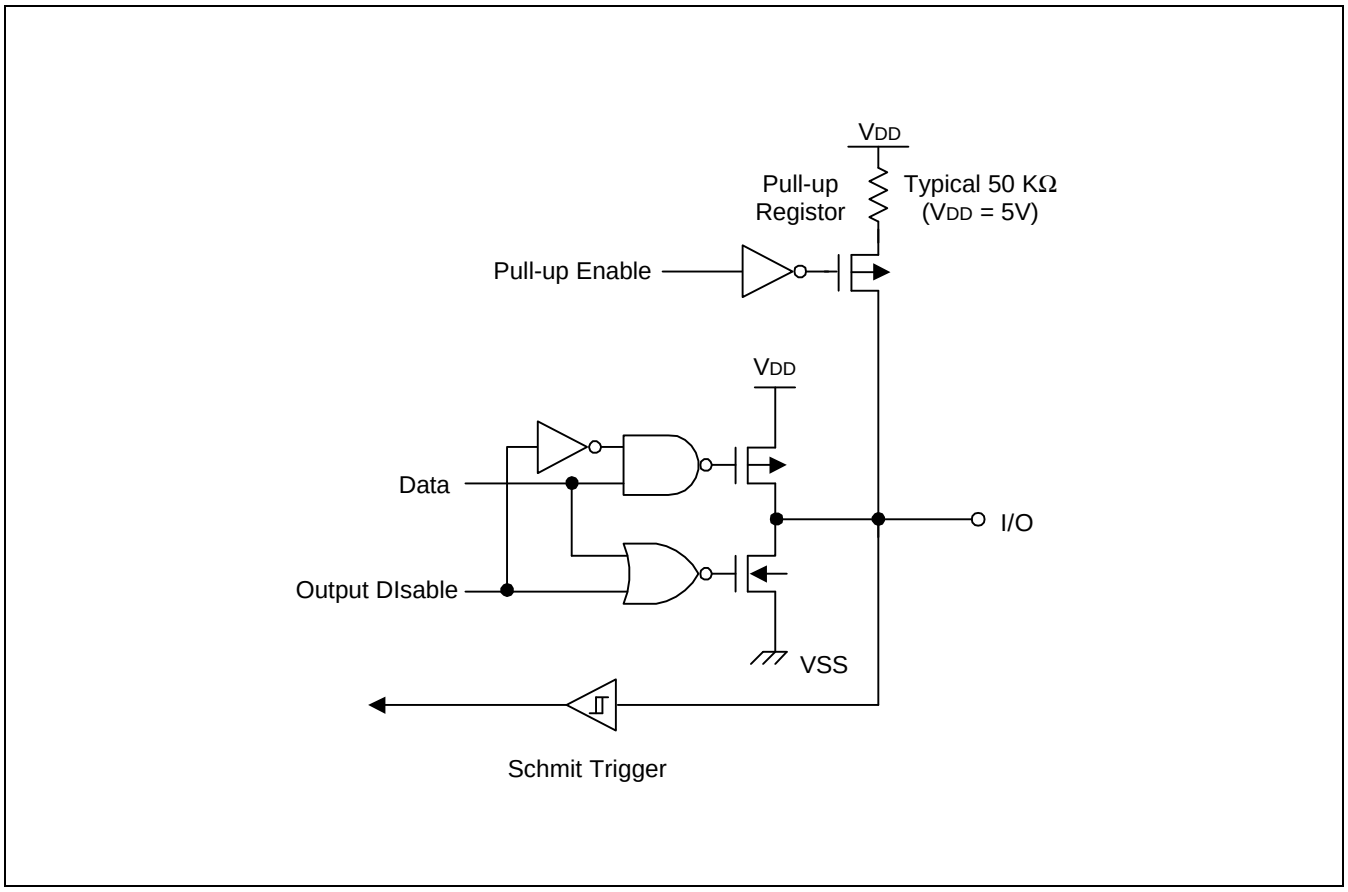


Figure 1-4. Pin Circuit Type 2

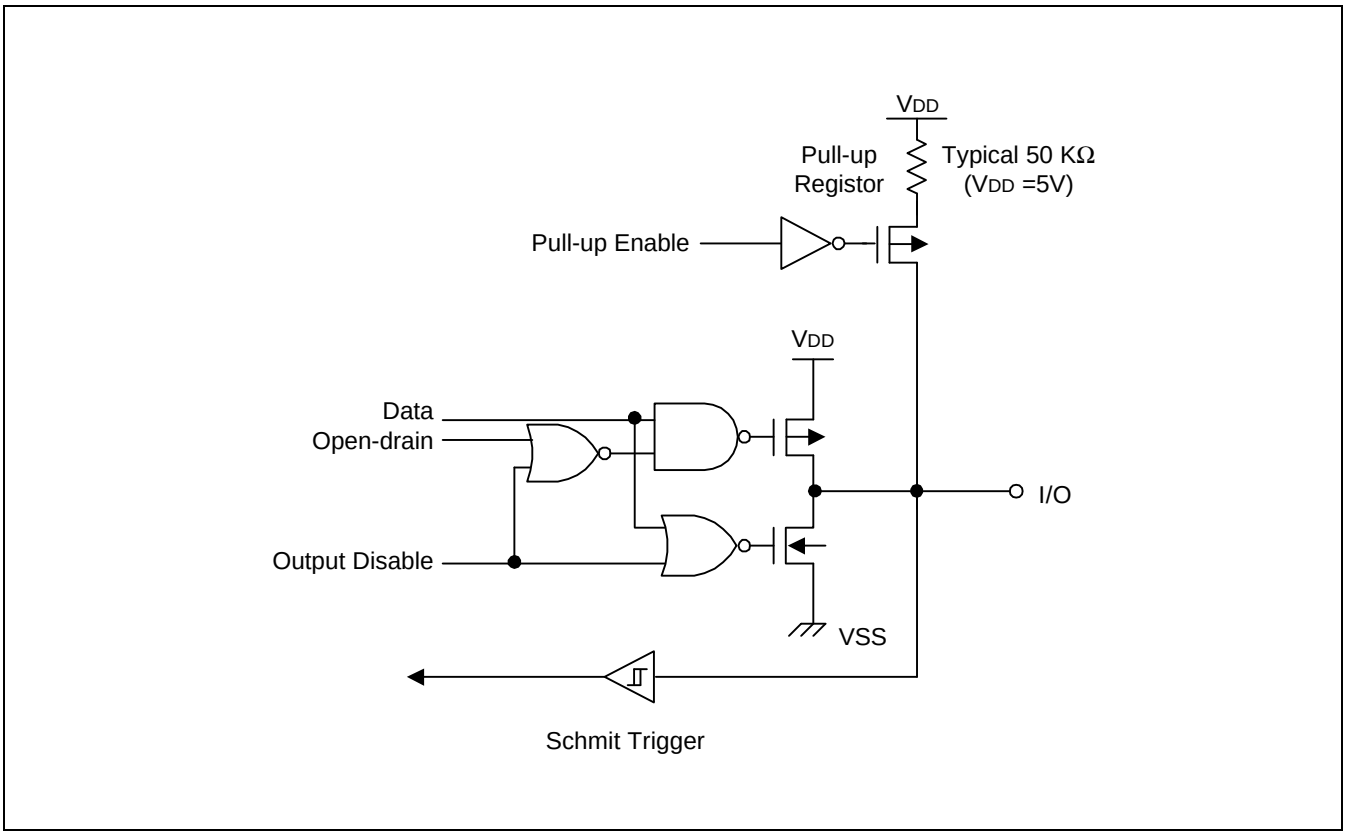


Figure 1-5. Pin Circuit Type 3

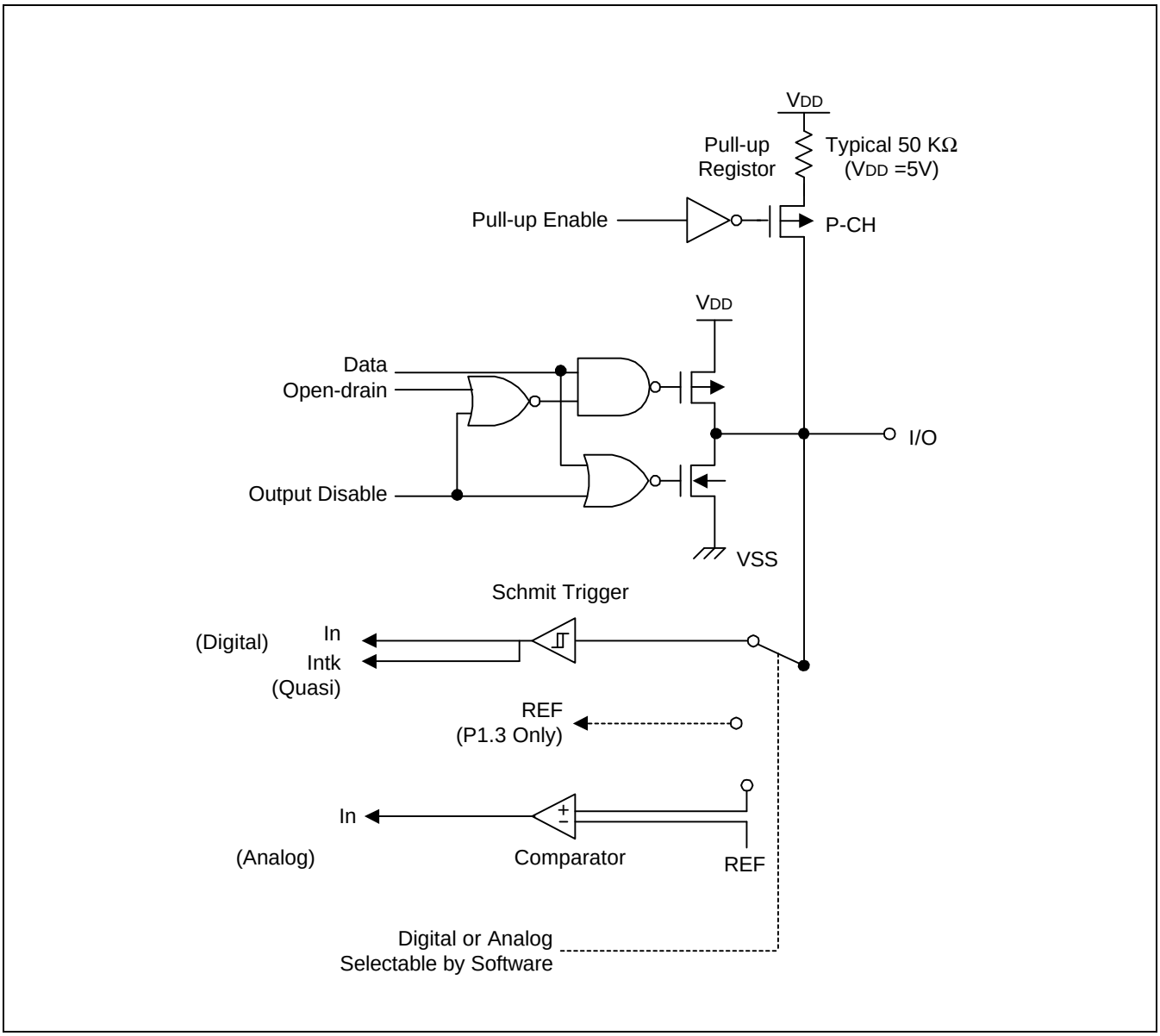


Figure 1-6. Pin Circuit Type 4

14 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C7031/7032 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Oscillators characteristics
— I/O capacitance
— Comparator electrical characteristics
— A.C. electrical characteristics
— Operating voltage range

Oscillation Characteristics

— System clock oscillator frequencies and stabilization time

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Miscellaneous Timing Waveforms

— Clock timing measurement at X_{IN}

— TIO timing

— Input timing for RESET

— Input timing for external interrupts and quasi-interrupts

— Serial data transfer timing

Characteristic Curves

— I_{DD} vs Frequency

— I_{DD} vs V_{DD}

— I_{OL} vs V_{OL} (P0.0)

— I_{OL} vs V_{OL} (P1.1)

— I_{OL} vs V_{OL} (P2.0)

— I_{OH} vs V_{OH} (P0.0)

— I_{OH} vs V_{OH} (P1.1)

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	- 0.3 to + 7.0	V
Input Voltage	V_I	All I/O ports	- 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	- 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	- 5	mA
		All I/O ports active	- 15	
Output Current Low	I_{OL}	One I/O port active	25	mA
		All I/O port, total	100	
Operating Temperature	T_A	–	- 40 to + 85	°C
Storage Temperature	T_{stg}	–	- 65 to + 150	°C

Table 14-2. D.C. Electrical Characteristics

(T_A = - 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	$V_{IH}1$	Ports 0, 1, 2, 3, RESET	0.7 V_{DD}	–	V_{DD}	V
	$V_{IH}2$	X_{IN}, X_{OUT}	V_{DD} - 0.5	–	V_{DD}	
Input Low Voltage	$V_{IL}1$	Ports 0, 1, 2, 3, RESET	–	–	0.3 V_{DD}	V
	$V_{IL}2$	X_{IN}, X_{OUT}			0.4	
Output High Voltage	$V_{OH}1$	V_{DD} = 4.5 V to 6.0 V I_{OH} = - 3 mA Ports 0, 1, 2, 3 except P0.0	V_{DD} - 1.0	V_{DD} - 0.4	–	V
		V_{DD} = 4.5 V to 6.0 V I_{OH} = - 6 mA Ports 0, 1, 2, 3 except P0.0	V_{DD} - 2.0	V_{DD} - 0.9	–	
	$V_{OH}2$	V_{DD} = 4.5 V to 6.0 V I_{OH} = - 10 mA P0.0	V_{DD} - 2.0	–	–	
Output Low Voltage	$V_{OL}1$	V_{DD} = 4.5 V to 6.0 V I_{OL} = 25 mA Ports 0, 1, 2, 3 except P0.0	–	1.4	2.0	V
	$V_{OL}2$	V_{DD} = 4.5 V to 6.0 V I_{OL} = 50 mA P0.0	–	1.6	2.0	V

Table 14-2. D.C. Electrical Characteristics (Continued)

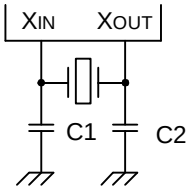
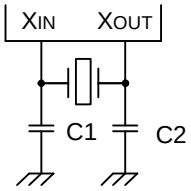
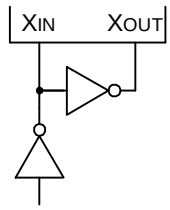
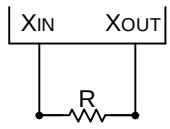
(T_A = - 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	$I_{LIH}1$	$V_{IN} = V_{DD}$ All input pins except $I_{LIH}2$	–	–	3	µA
	$I_{LIH}2$	$V_{IN} = V_{DD}$ X_{IN}, X_{OUT}		15	20	
Input Low Leakage Current	$I_{LIL}1$	V_{IN} = 0 V All input pins except $I_{LIL}2$	–	–	- 3	µA
	$I_{LIL}2$	V_{IN} = 0 V X_{IN}, X_{OUT}		-15	- 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	- 3	µA
Pull- Up Resistor	R_L	V_{IN} = 0 V; V_{DD} = 5 V - 10 % Ports 0, 1, 2, 3	15	50	80	KΩ
		V_{IN} = 0 V; V_{DD} = 3 V - 10 % Ports 0, 1, 2, 3	30	100	200	
Supply Current (2)	$I_{DD}1$	V_{DD} = 5 V ± 10 % (2) 4.19 MHz crystal oscillator C1 = C2 = 22 pF	–	1.7	8.0	mA
		V_{DD} = 3 V ± 10 % (3) 4.19 MHz crystal oscillator C1 = C2 = 22 pF		0.6	1.2	
	$I_{DD}2$	Idle mode; V_{DD} = 5 V ± 10 % 4.19 MHz crystal oscillator C1 = C2 = 22 pF	–	0.5	1.8	mA
		Idle mode; V_{DD} = 3 V ± 10 % 4.19 MHz crystal oscillator C1 = C2 = 22 pF		0.2	1.0	
	$I_{DD}3$	Stop mode V_{DD} = 5 V - 10 %		0.2	5	µA
		Stop mode V_{DD} = 3 V - 10 %		0.1	3	

NOTES:
1. D.C. electrical values for Supply Current ($I_{DD}1$ to $I_{DD}3$) do not include current drawn through internal pull-up resistors.
2. For high-speed controller operation, set the PCON register to 0011B.
3. For low-speed controller operation, set the PCON register to 0000B.

Table 14-3. Oscillators Characteristics

(T_A = - 40 °C to + 85 °C, V_{DD} = 5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency(1)	–	0.4	–	4.5	MHz
		Stabilization time (2)	After V_{DD} reaches the minimum level of its variable range	–	–	4	ms
Crystal Oscillator		Oscillation frequency(1)	–	0.4	4.19	4.5	MHz
		Stabilization time (2)	V_{DD} = 2.7 V to 4.5 V	–	–	30	ms
			V_{DD} = 4.5 V to 6.0 V	–	–	10	
External Clock		X_{IN} input frequency (1)	–	0.4	–	4.5	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	111	–	1250	ns
RC Oscillator		Frequency	V_{DD} = 5 V	0.6	1	2.3	MHz
			V_{DD} = 3 V	0.4	0.8	1.5	

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 14-5. Comparator Electrical Characteristics

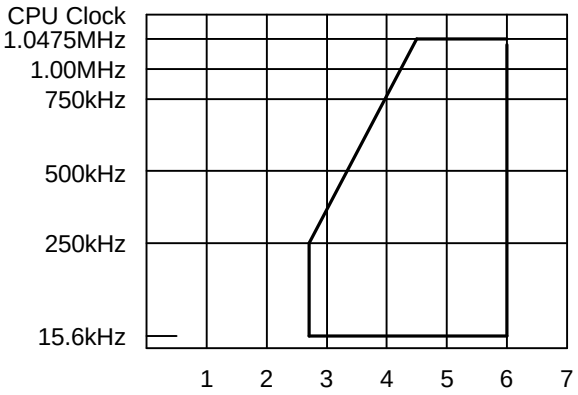
(T_A = - 40 °C to + 85 °C, V_{DD} = 4.0 V to 6.0 V)

Parameter		Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range		–	–	0	–	V_{DD}	V
Reference Voltage Range		V_{REF}	–	0	–	V_{DD}	V
Input Voltage Accuracy	Internal Reference	$V_{CIN}1$	–	–	–	- 150	mV
	External Reference	$V_{CIN}2$	–	–	–	- 50	
Input Leakage Current		I_{CIN}, I_{REF}	–	- 3	–	3	µA

Table 14-6. A.C. Electrical Characteristics

(T_A = - 40 °C to + 85 °C, V_{DD} = 2.7 V to 6.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 4.5 V to 6.0 V	0.95	–	64	µs
		V_{DD} = 2.7 V to 4.5 V	3.8			
TIO Input Frequency	f_{TI}	V_{DD} = 4.5 V to 6.0 V	0	–	1	MHz
		V_{DD} = 2.7 V to 4.5 V			275	kHz
TIO Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 V to 6.0 V	0.48	–	–	µs
		V_{DD} = 2.7 V to 4.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 4.5 V to 6.0 V; Input	800	–	–	ns
		V_{DD} = 4.5 V to 6.0 V; Output	950			
		V_{DD} = 2.7 V to 4.5 V; Input	3200			
		V_{DD} = 2.7 V to 4.5 V; Output	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 4.5 V to 6.0 V; Input	400	–	–	ns
		V_{DD} = 4.5 V to 6.0 V; Output	t_{KCY}/2-50			
		V_{DD} = 2.7 V to 4.5 V; Input	1600			
		V_{DD} = 2.7 V to 4.5 V; Output	t_{KCY}/2-50			
SI Setup Time to SCK High	t_{SIK}	Input	100	–	–	ns
		Output	150			
SI Hold Time to SCK High	t_{KSI}	Input	400	–	–	ns
		Output	400			
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 4.5 V to 6.0 V; Input	–	–	300	ns
		V_{DD} = 4.5 V to 6.0 V; Output			250	
		V_{DD} = 2.7 V to 4.5 V; Input			1000	
		V_{DD} = 2.7 V to 4.5 V; Output			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT1, KS0-KS3	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs



CPU Clock = 1/n x oscillator frequency (n =4, 8 or 64)

Figure 14-1. Standard Operating Voltage Range

Table 14-7. RAM Data Retention Supply Voltage in Stop Mode

(T_A = - 40 °C to + 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Data Retention Supply voltage	V_{DDDR}	–	2.0	—	6.0	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 2.0 V	–	0.1	10	µA
Release Signal Set Time	t_{SREL}	–	0	—	–	µs
Oscillation Stabilization Wait Time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

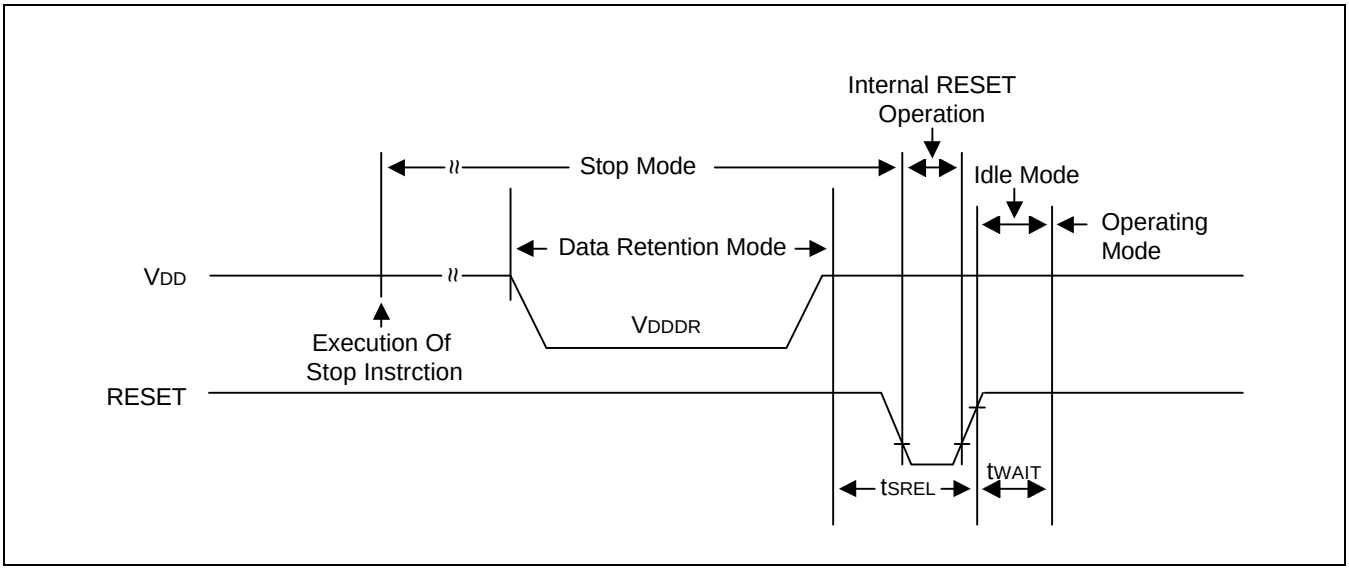


Figure 14-2.Stop Mode Release Timing When Initiated By RESET

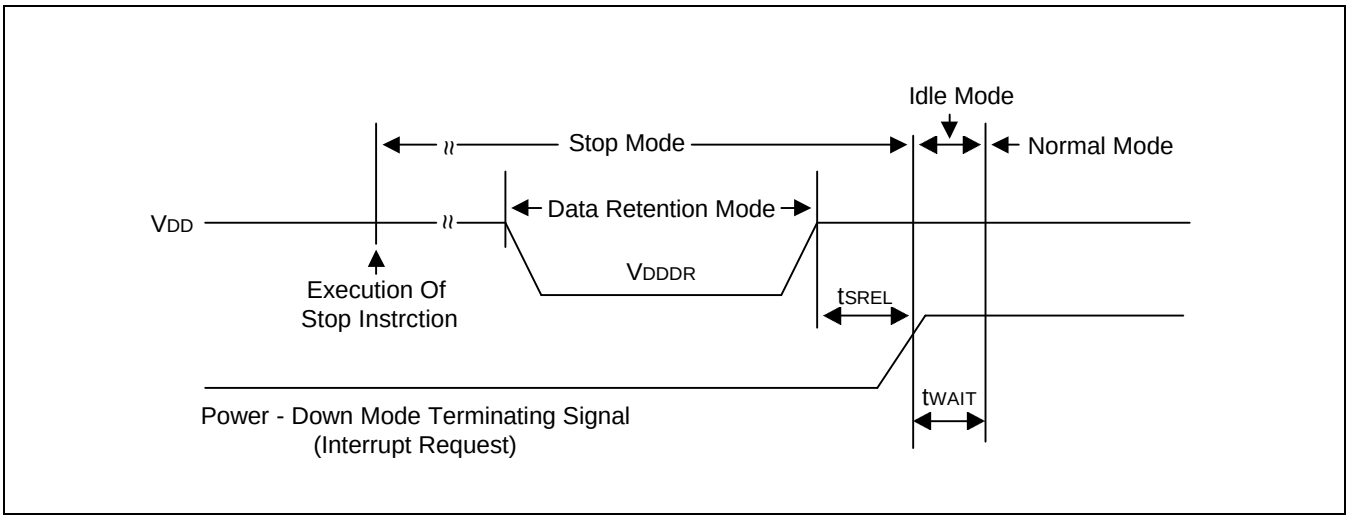


Figure 14-3. Stop Mode Release Timing When Initiated By Interrupt Request

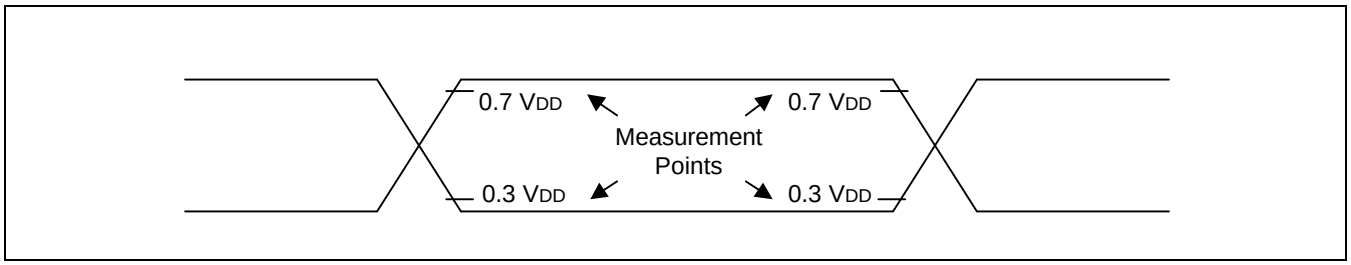


Figure 14-4. A.C. Timing Measure Points (Except for X_{IN})

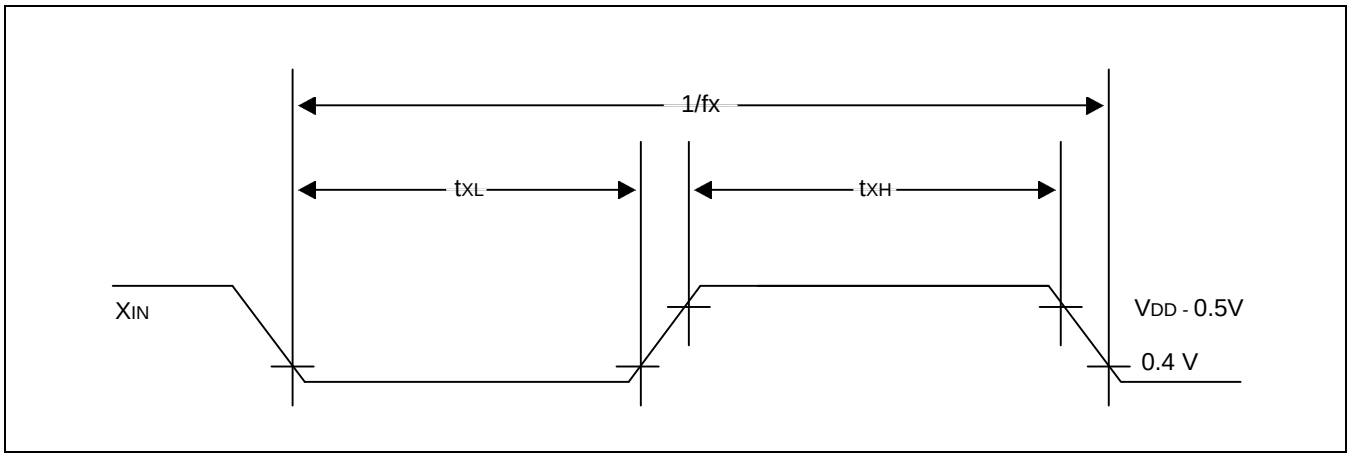


Figure 14-5. Clock Timing Measurement at X_{IN}

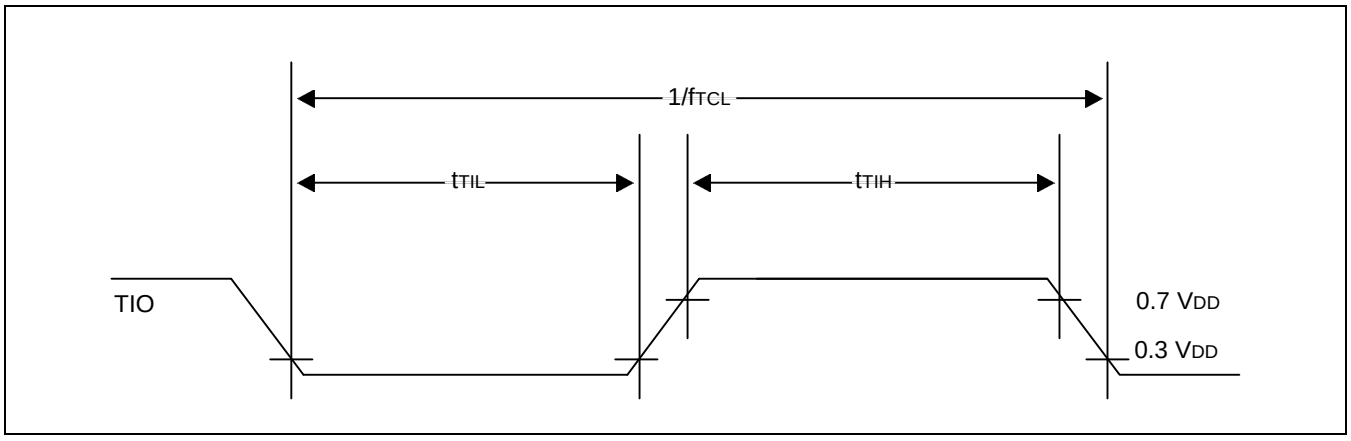


Figure 14-6. TIO Timing

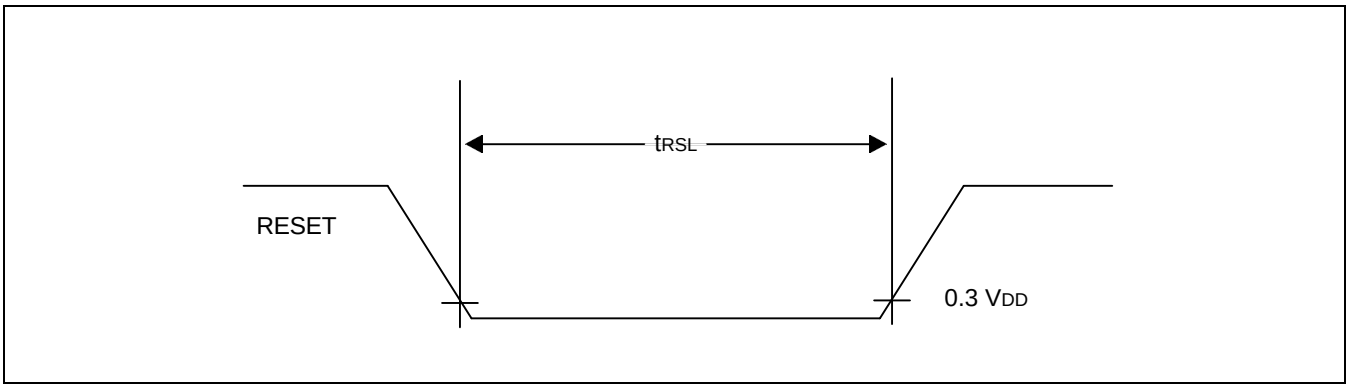


Figure 14-7. Input Timing for RESET Signal

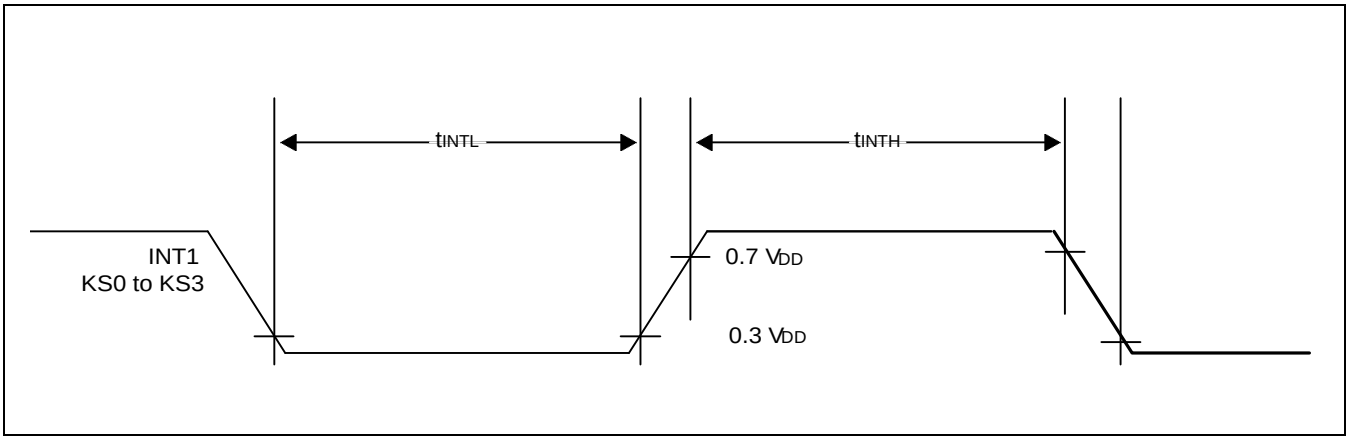


Figure 14-8. Input Timing for External Interrupts

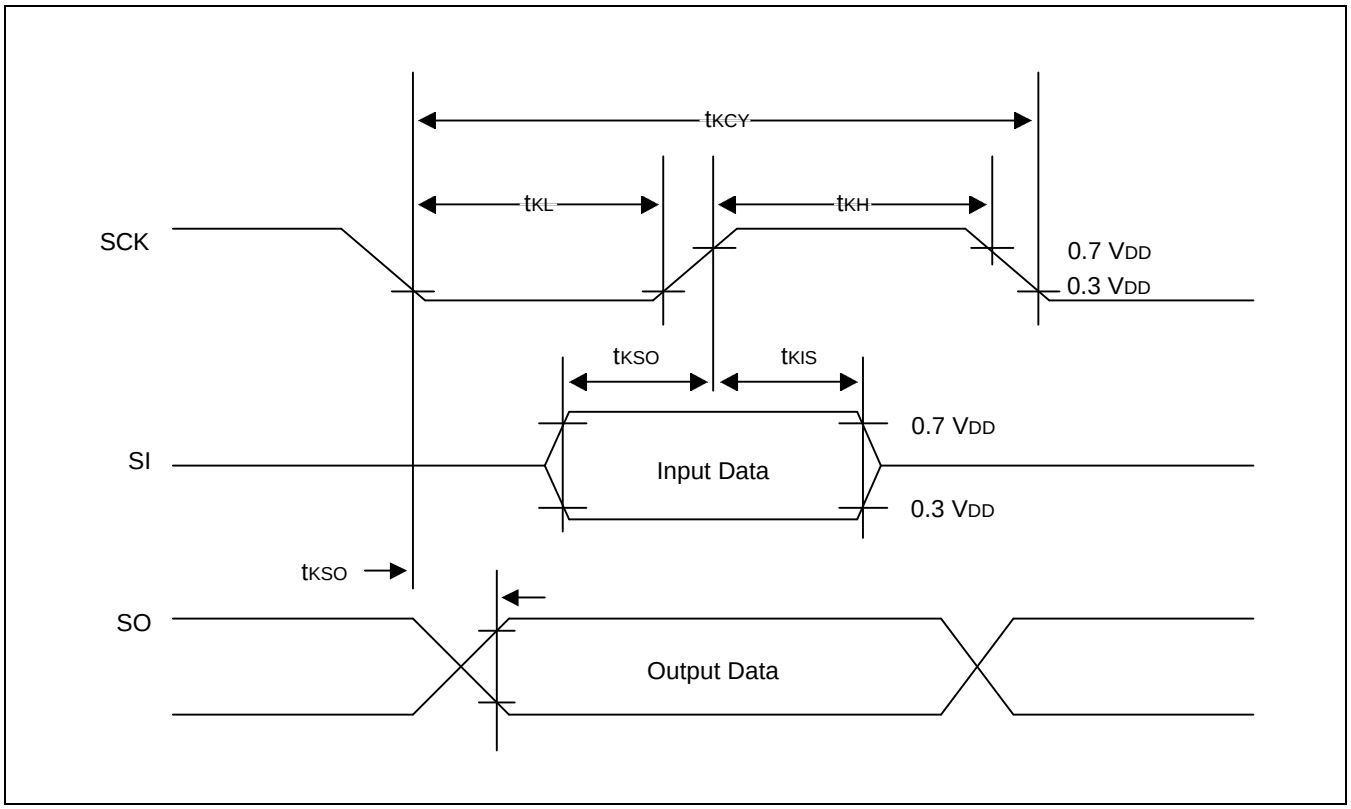


Figure 14-9. Serial Data Transfer Timing

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

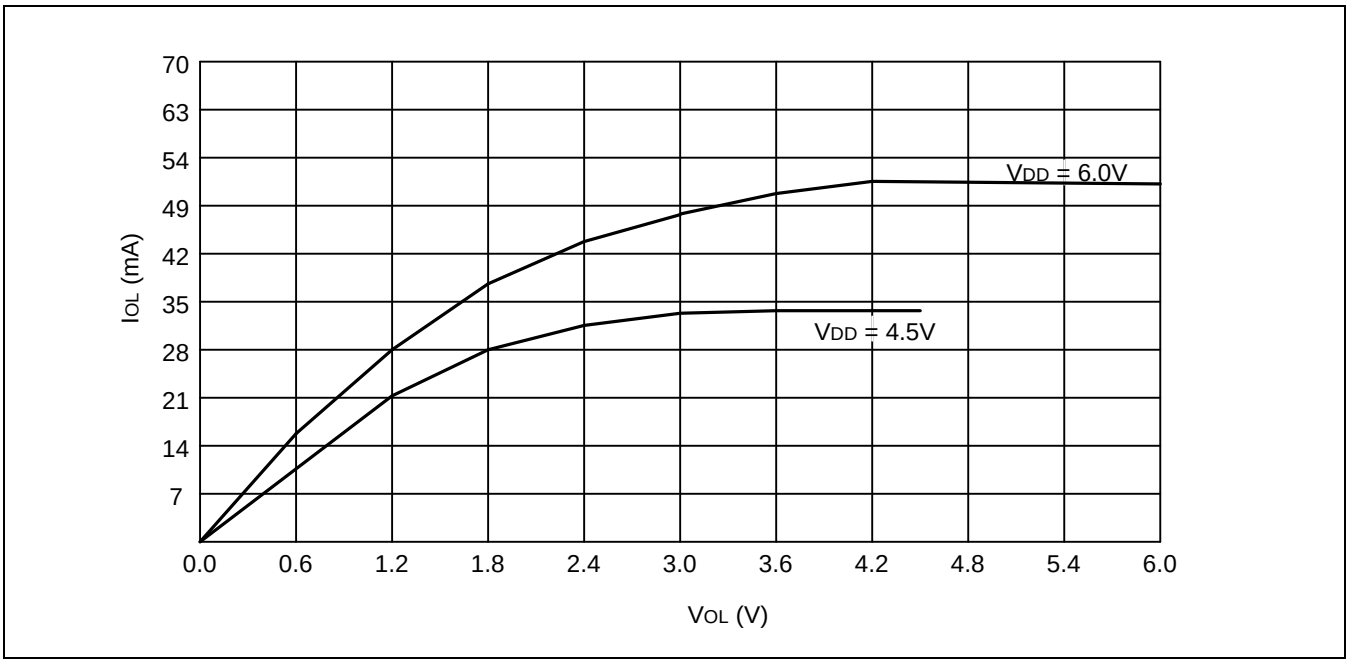


Figure 14-10. I_{OL} vs. V_{OL} (Port 0,1,2,3)

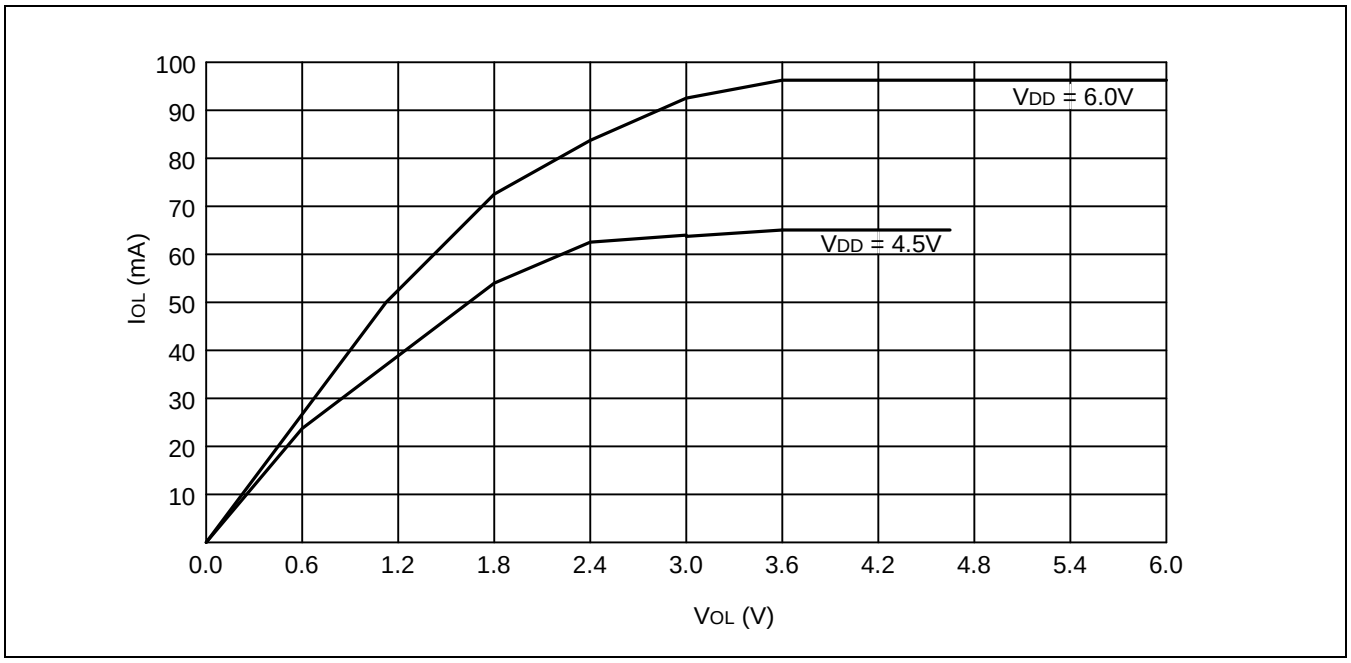


Figure 14-11. I_{OL} vs. V_{OL} (Port 0.0)

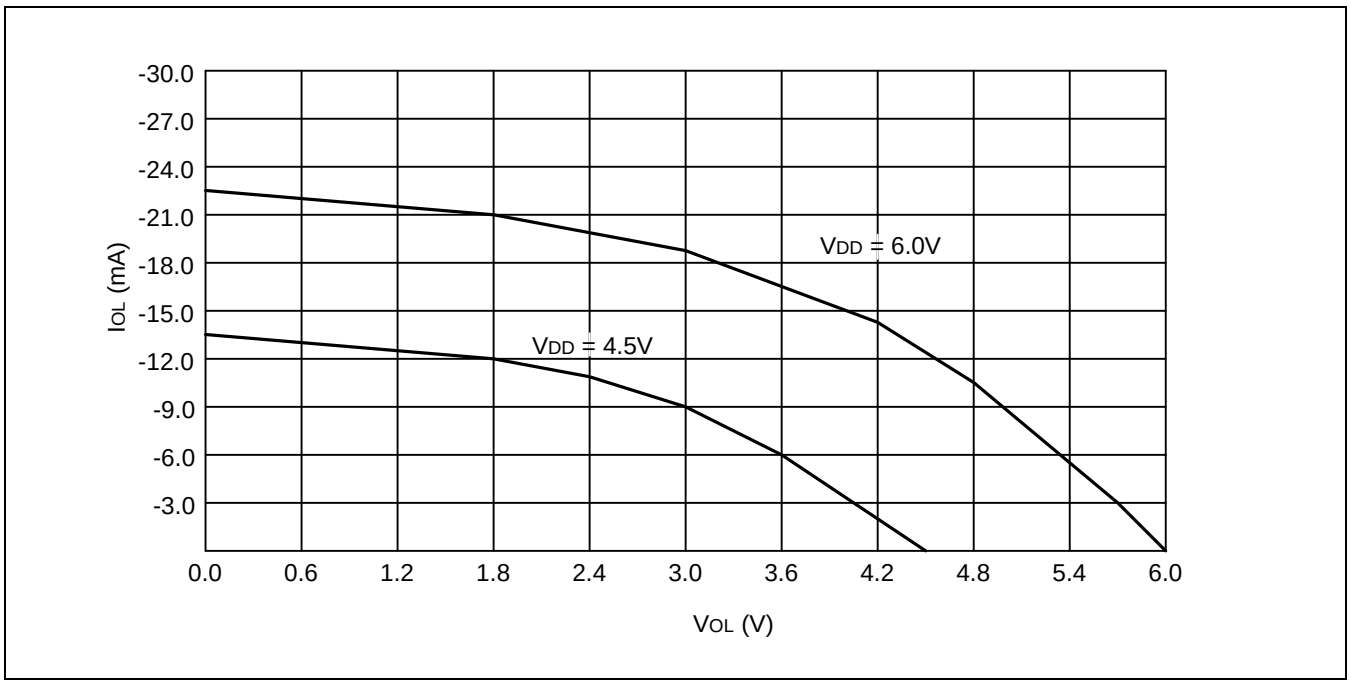


Figure 14-12. I_{OH} vs. V_{OH} (Port 0,1,2,3except P0.0)

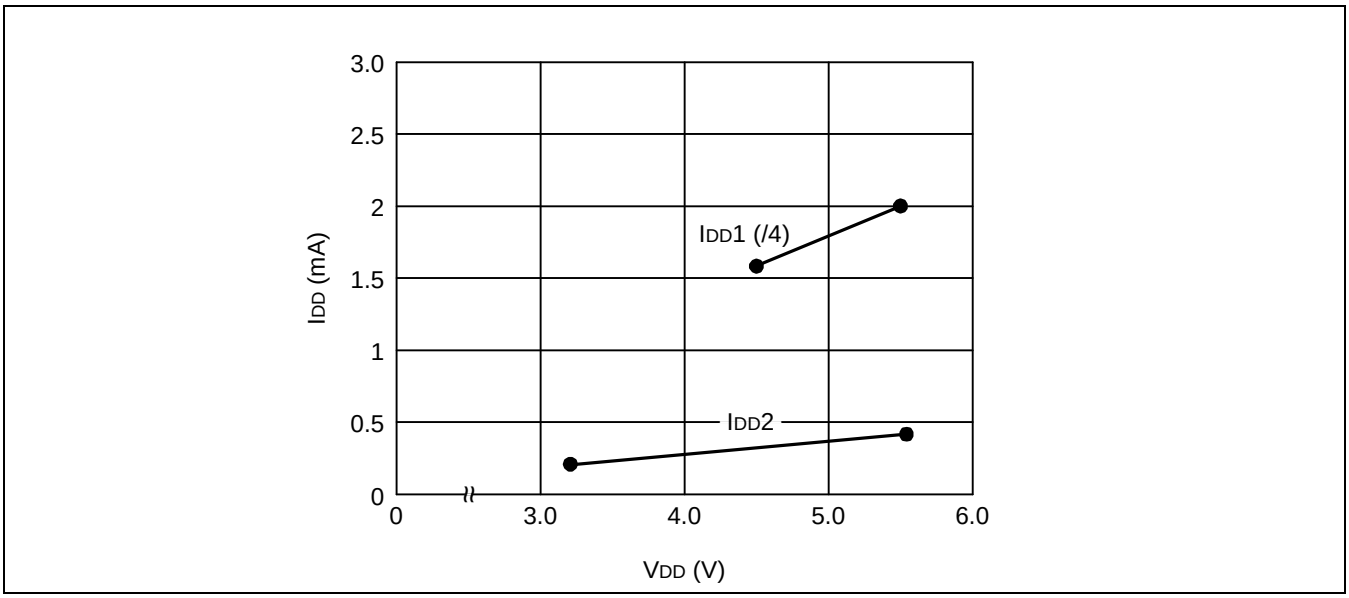


Figure 14-13. I_{DD} vs. V_{DD}

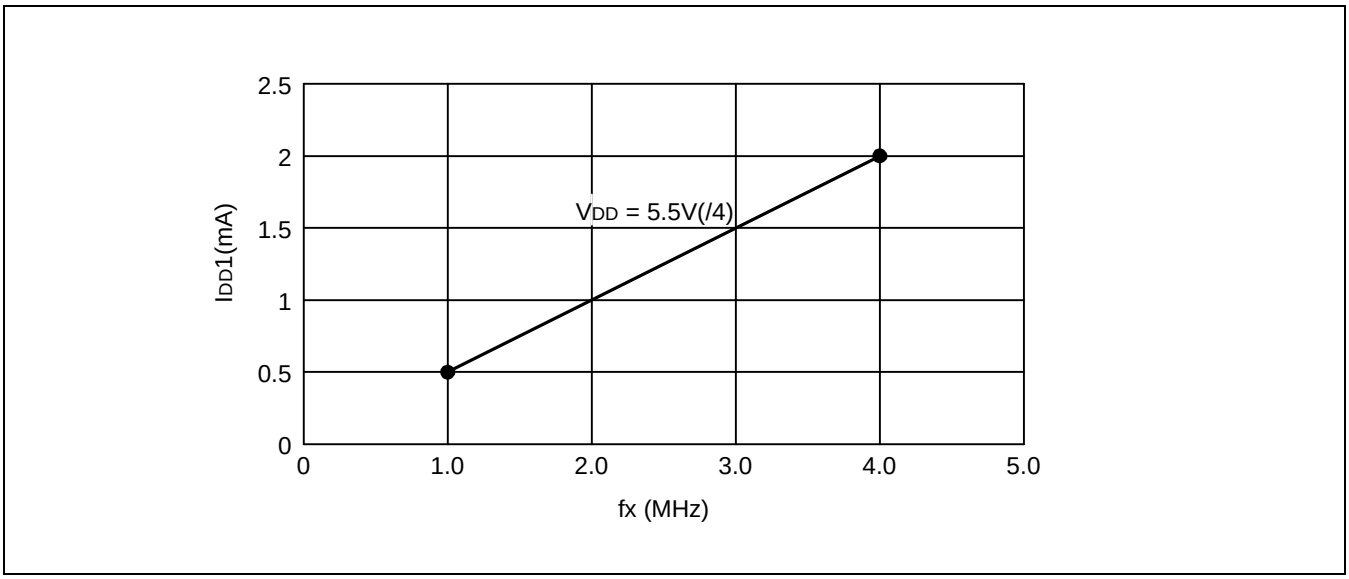


Figure 14-14. I_{DD} vs. Frequency

15 MECHANICAL DATA

This section contains the following information about the device package:

— A 20-pin DIP package is available for S3C7031/7032.

— A 20-pin SOP package is available for S3C7031/7032.

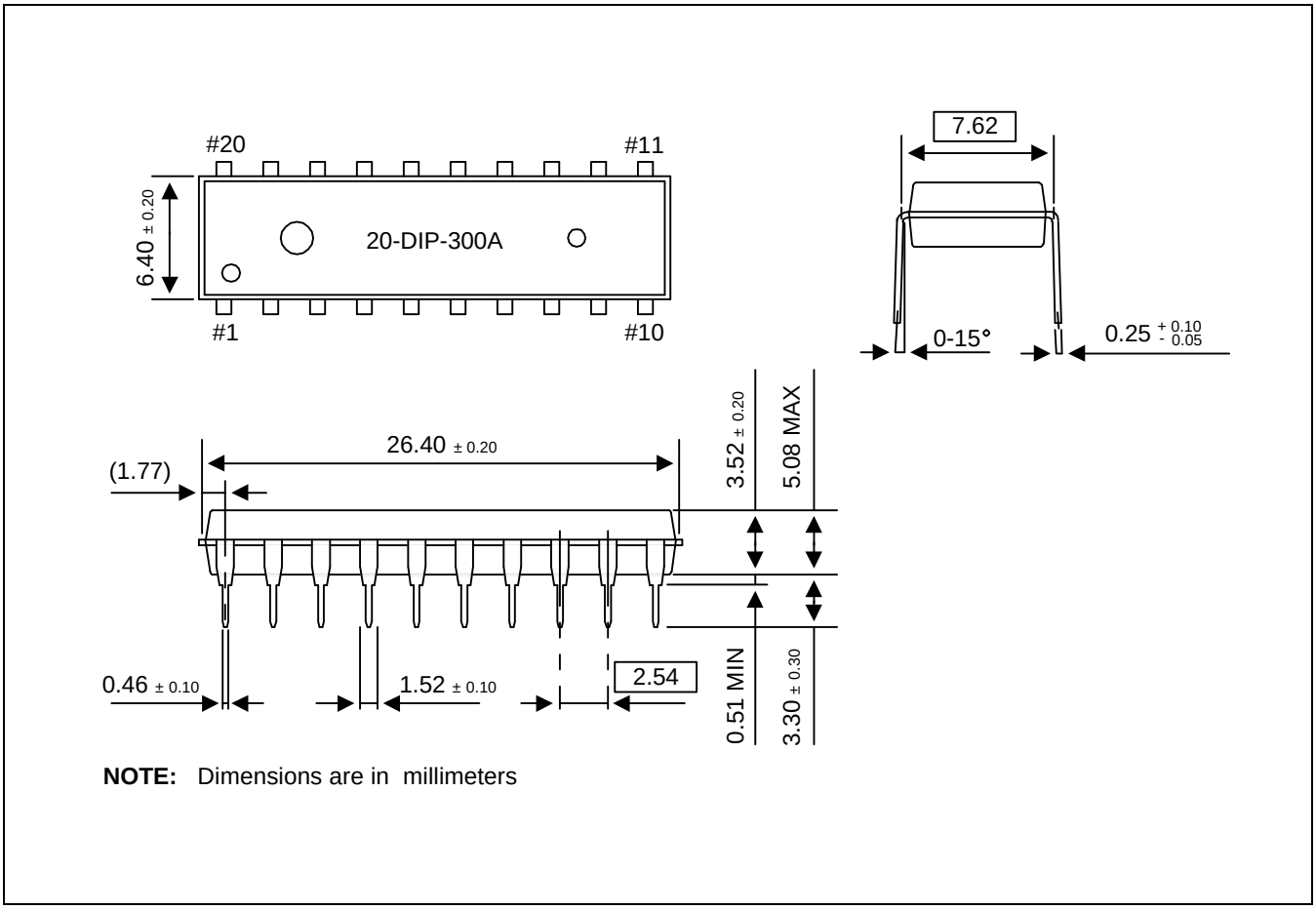


Figure 15-1. 20-pin DIP-300A Package Dimensions

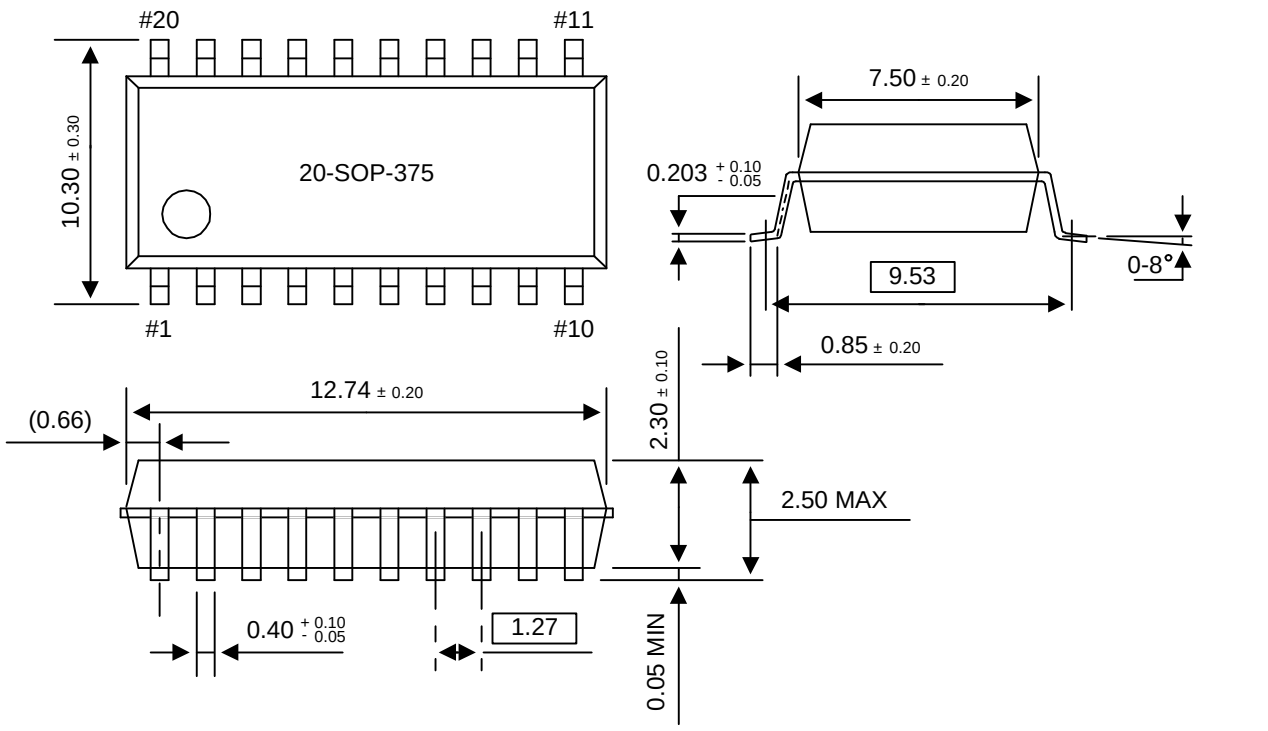


Figure 15-2. 20-pin SOP-375 Package Dimensions