Preliminary Data Sheet

VSC838

3.2Gb/s
36x37 Crosspoint Switch

Features

- 36 Input by 37 Output Crosspoint Switch
- 3.2Gb/s NRZ Data Bandwidth
- Non-Blocking Architecture Broadcast and Multicast Capabilities
- LVTTL/2.5V CMOS Control I/O (3.3V tolerant)
- Input Signal Activity Monitoring Function
- Integrated Signal Equalization (ISE) for Deterministic Jitter Reduction
- 66MHz Dual Programming Port
- Parallel and Serial programming modes
- Programmable On-Chip I/O Termination
- Differential CML Output Drivers
- Single 2.5V Supply
- 6W Typical—Low Drive Mode
  7W Typical—High Drive Mode
- High Performance 37.5mm, 480 TBGA Package

General Description

The VSC838 is a monolithic 36x36 asynchronous crosspoint switch, designed to carry broadband data streams. The VSC838 also has an internal 37th output channel which is used in conjunction with the Activity Monitor to allow in system diagnostics.

A high degree of signal integrity is maintained throughout the chip via fully differential signal paths.

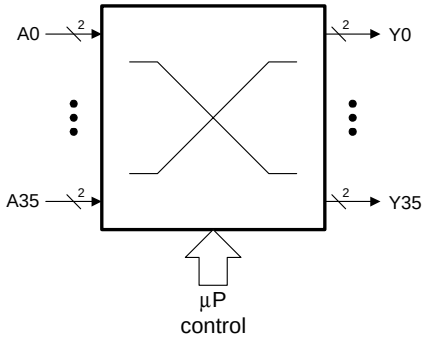
The crosspoint function is based on a multiplexer array architecture. Each data output is driven by a 36:1 multiplexer that can be programmed to one and only one of its 36 inputs. The signal path is unregistered and fully asynchronous, so there are not any restrictions on the phase, frequency, or signal pattern at each input.

Each high-speed output is a fully differential, switched current driver with switchable on-die terminations for maximum signal integrity. Data inputs are terminated on-die through 100Ω impedance between true and complement inputs (see *Input Termination* section for further details).

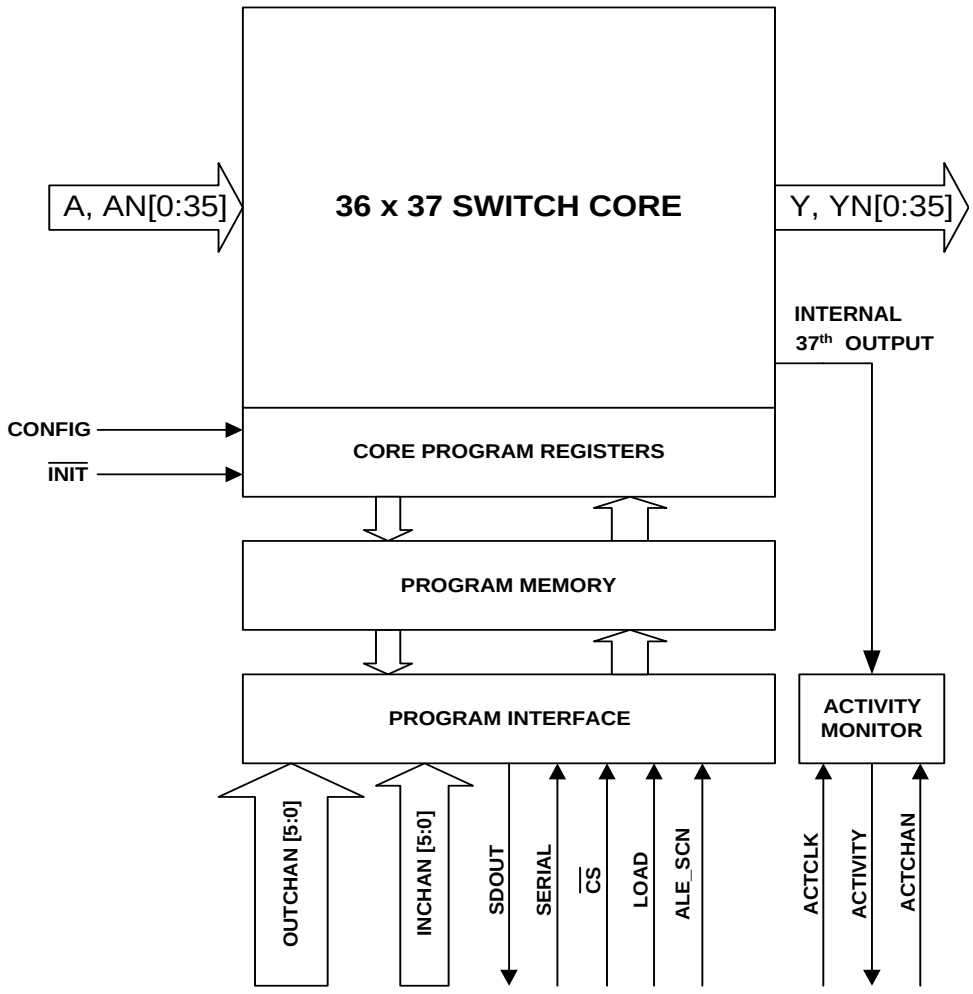
A dual mode programming interface is provided that allows programming commands to be sent as serial data or parallel data. Core programming can be random for each port address, or multiple program assignments can be queued and issued simultaneously. The programming may be initialized to a “straight-through” configuration (A0 to Y0, A1 to Y1, etc.) using the $\overline{\text{INIT}}$ pin.

Unused channels may be powered down to allow efficient use of the switch in applications that require only a subset of the channels. Power-down can be accomplished in hardware, via dedicated power pins for pairs of input and output channels, or in software by programming individual unused outputs with a disable code.

VSC838 Block Diagram



Functional Block Diagram



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Functional Description

Input / Output Characteristics

All input data must be differential and should be nominally biased to +2.0V or AC-coupled. Other levels are allowed as described under the *Input Termination* section. On-chip terminations are provided, with a nominal impedance of 100Ω differential. All input termination resistors float with an internal bias provided for AC-coupling.

For direct interconnection of multiple VSC838 devices, a CML termination mode is provided by tying the ITC pin to V_{CC}, which ties the center point of the 100Ω termination to V_{CC}, causing the terminations to act as loads for an open-drain or open-collector differential output.

Data outputs are provided through differential current switches with on-chip back-termination. The output circuit is capable of driving external 50Ω far-end termination (recommended). The output back-terminations are electronically switchable to enable a power savings of 1W (max) by reducing the output driver current.

Programming Interface

Parallel Mode

In parallel mode (SERIAL=0), the binary word on INCHAN[5:0] is the numerical identifier of the input that will be routed to the specified output. OUTCHAN[5:0] is the numerical identifier of the output being programmed. A rising edge on the LOAD signal will transfer the programming data to the shadow register in the program memory. Raising CONFIG (asynchronously) will transfer the programming data to the main latches in the program memory and cause the internal select signals in the core to re-configure the multiplexer. Lowering CONFIG will latch the main latches. CONFIG may be tied HIGH to enable programming to take effect instantaneously.

This interface may be used with multiplexed address/data buses by using only INCHAN[5:0] without OUTCHAN[5:0] and dropping ALE when the address of the output to be programmed is present on INCHAN[5:0]. After the address is latched, the input address may be presented on INCHAN[5:0] and programming proceeds as above.

No read-back capability is provided in parallel mode. Read-back for diagnostic purposes is provided in serial mode via the scan function.

Serial Mode

In serial mode (SERIAL=1), the INCHAN[0] pin becomes the serial data input SDIN and the INCHAN[1] pin becomes the serial clock SCLK (rising edge triggered). A serial word of the form [Output][Input] is shifted into the internal shift register, and the LOAD pin is asserted (HIGH) coincident with the last bit of the data word to signal that the word is to be applied. This transfers the input identifier to the shadow register of the addressed output. CONFIG is then applied (asynchronously) to transfer one or more program commands to the main latches of the program memories.

The SDOUT pin follows the data on the INCHAN[0](SDIN) pin 14 clock cycles later. This enables the user to chain the serial ports of several crosspoints, shift program data for all switches through such a chain, and assert LOAD on all switches simultaneously to program all of the connections simultaneously.

The output field is 7 bits long, representing the binary numerical identifier of the output to be programmed. The input field is 7 bits long, representing the numerical identifier of the input that will be routed to the specified output.

Serial Read-Back

Read-back of the program memory contents is accomplished in serial mode by setting the ALE_SCN pin HIGH. This will serially shift out the contents of the main latches in the program memories, slice 36 first and slice 0 last, and MSB-first, LSB-last for each 7-bit word (see Figure 3). One rising edge of INCHAN[1](SCLK) with ALE_SCN=0 and SERIAL=1 must occur to load the entire 483-bit shift register prior to shifting out data. At a clock rate of 66MHz, this operation takes 7.26µs.

Activity Monitoring

The activity monitor observes the output of the internal 37^{th} output from the core. By programming the 37^{th} output to observe various inputs, the input signals can be scanned for activity or lack thereof. Each rising edge of ACTCLK causes the monitor to read out the activity state from the previous ACTCLK period and clears the internal activity state until a data transition triggers it again. There must be a minimum of one rising and one falling edge on the observed input data pin during the ACTCLK period for activity to be detected. After power-on the output of ACTIVITY after the first ACTCLK rising edge is unknown.

To access the 37^{th} output, ACTCHAN and INCHAN[5] must both be HIGH.

Selective Power-Down

Unused input and output channels can be made to consume little or no power via one of two methods of selective power-down.

Software Power-Down

Using this feature, unused outputs may be disabled, saving approximately 170 mW per channel for maximum dissipation conditions. This is accomplished by programming each unused output to look at input 127 (7F Hex), which represents a non-existent input channel. The channel may be subsequently activated by programming a valid input address. It is recommended, however, that any changes in power programming only be executed as part of an initialization sequence to guard against the effects of any switching transients that might result from changing the power supply current suddenly. Software mode does not affect the functioning or power of unused input channels.

Hardware Power-Down

Using this feature, the power associated with given pairs of inputs may be shut off by tying the corresponding V_{EE} pin to V_{CC} (see Table 10). Approximately 160 mW per input pair is saved under the maximum dissipation conditions. The power associated with given pairs of outputs, including their contribution to the core power, can be shut off by tying the corresponding V_{EE} pin to V_{CC} (see Table 10). Approximately 360 mW per output pair is saved under the maximum dissipation conditions.

Certain V_{EE} pins must always be active. In other words, tied to the most negative supply, so the corresponding inputs and outputs will always be on and consuming power. See Figure 7 and Table 10 for the location of these pins.

AC Characteristics

Table 1: Data Path

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
f_{RATE}	Maximum data rate	-	-	3.2	Gb/s
T_{SKW}	Channel-to-channel delay skew	-	300	-	ps
T_{PDAY}	Propagation Delay from an A input to a Y output	-	750	-	ps
t_R, t_F	High-speed input rise/fall times, 20% to 80%	-	-	150	ps
t_R, t_F	High-speed output rise/fall times, 20% to 80%	-	-	150	ps
t_{jR}	Output added delay jitter, rms(1, 2)	-		10	ps
t_{jP}	Output added delay jitter, peak-to-peak(1, 2)	-		40	ps

NOTES: (1) Tested on a sample basis only. (2) Broadband (unfiltered) deterministic jitter added to a jitter-free input, 2^{23}-1 PRBS data pattern.

Table 2: Program Interface Timing

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{s\overline{WR}}$	Setup time from INCHAN[5:0] or OUTCHAN5:0] to rising edge of $\overline{WR}$.	3.35	—	—	ns
$T_{h\overline{WR}}$	Hold time from rising edge of WRB to INCHAN[5:0] or OUTCHAN[5:0].	1.45	—	—	ns
T_{PWLW}	Pulse width (HIGH or LOW) on LOAD	6.75	—	—	ns
$T_{s\overline{CS}}$	Setup time from $\overline{CS}$ to falling edge of LOAD or ALE_SCN in parallel or burst mode, or rising edge of LOAD in serial mode.	0	—	—	ns
T_{hCSB}	Hold time of $\overline{CS}$ rising edge after LOAD or ALE_SCN rising in parallel or burst mode, or falling edge of LOAD in serial mode, or falling edge of CONFIG in any mode.	0	—	—	ns
T_{PWCFG}	Pulse width (HIGH or LOW) on CONFIG.	6.75	—	—	ns
T_{sSDIN}	Setup time from INCHAN0(SDIN) to INCHAN1(SCLK) rising.	1.65	—	—	ns
T_{hSDIN}	Hold time of INCHAN0(SDIN) after INCHAN1(SCLK) rising.	1.0	—	—	ns
$T_{perSCLK}$	Minimum period of SCLK in serial mode.	15	—	—	ns
T_{sLOAD}	Setup time from LOAD to INCHAN1(SCLK) rising.	1.85	—	—	ns
T_{hLOAD}	Hold time of LOAD after INCHAN1(SCLK) rising.	0.95	—	—	ns
$T_{sSERIAL}$	Setup time from SERIAL rising to INCHAN1(SCLK) rising when entering serial mode or SERIAL falling to LOAD falling when entering parallel mode or SERIAL falling to LOAD rising when entering burst mode.	0.90	—	—	ns
$T_{hSERIAL}$	Hold time from INCHAN1(SCLK) rising to SERIAL falling when exiting serial mode.	0	—	—	ns
T_{dSDOUT}	Delay from INCHAN1(SCLK) rising to SDOUT, 20pF load.	—	—	6.20	ns
$T_{PW\overline{INIT}}$	Pulse width (HIGH or LOW) on $\overline{INIT}$.	6.75	—	—	ns
T_{sSCAN}	Setup time from ALE_SCN to INCHAN1(SCLK) rising when starting or completing a serial read-back sequence.	1.65	—	—	ns
T_{hSCAN}	Hold time of ALE_SCN after INCHAN1(SCLK) rising when starting or completing a serial read-back sequence.	1.0	—	—	ns

Figure 1: Parallel Mode -- Separate Address/Data (leave ALE_SCN pin HIGH)

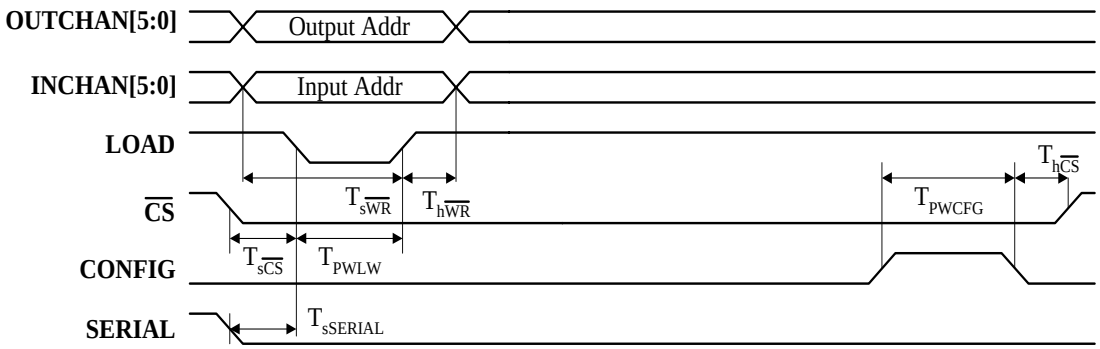


Figure 2: Parallel Mode -- Multiplexed Address/Data

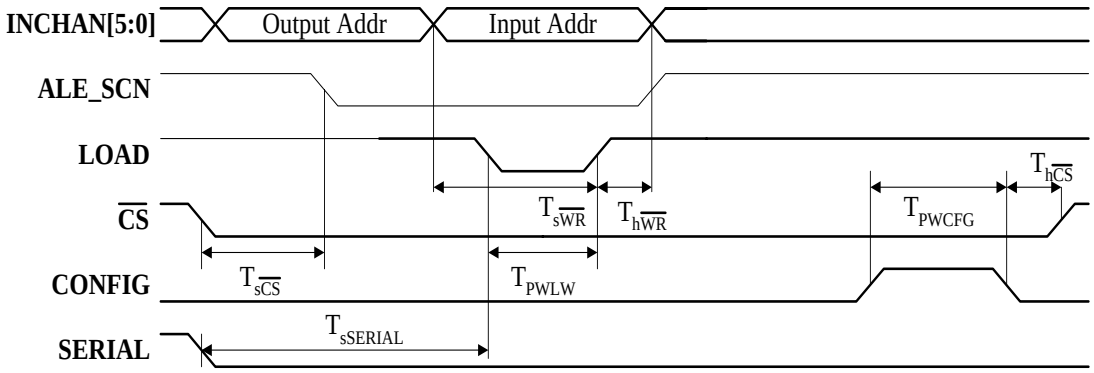


Figure 3: Serial Mode (leave ALE_SCN pin LOW during programming)

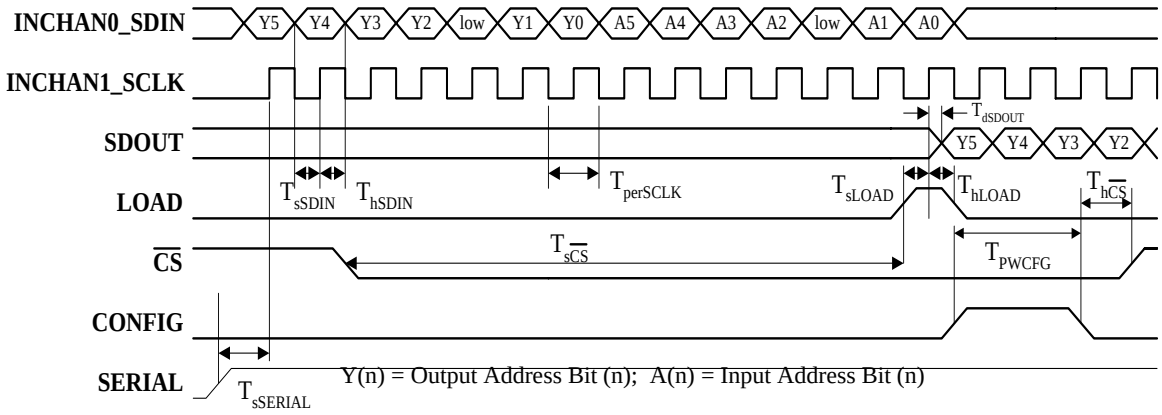
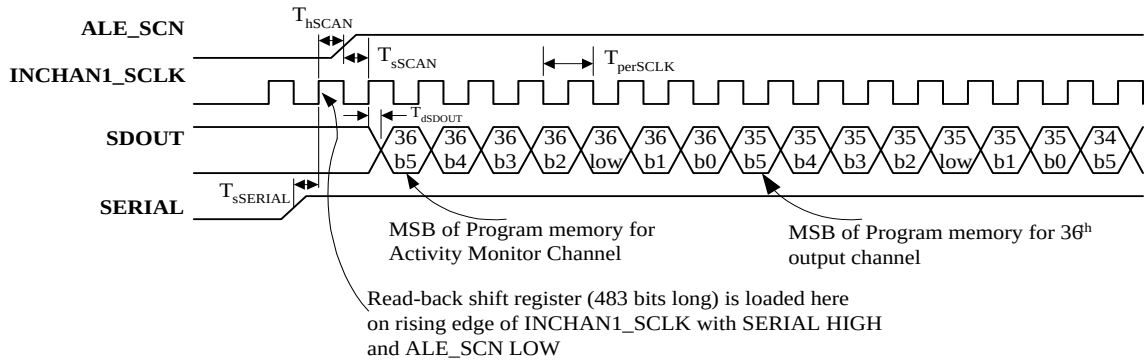


Figure 4: Serial Read-Back



NOTE: The word pattern during serial read back will be four valid words followed by four 'DON'T CARE' words.

DC Characteristics

All characteristics are over the specified operating conditions.

Table 3: Power Supply Requirements

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{CC}	V_{CC} supply current		2,286	3,428	mA	
P_T	Total chip power (with I_{TERM} = 0 and back-terminations ON, high drive)		6	9	W	MAX P_T is with +5% Supply, +85°C case temperature and high drive

Table 4: Control Port Input Levels (LVTTL/CMOS)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage	1.7		V_{CC}+1.0	V	
V_{IL}	Input LOW voltage	0		0.8	V	
I_{IH}	Input HIGH current			TBD	mA	
I_{IL}	Input LOW current			TBD	mA	
V_{OH}	Output HIGH voltage	V_{CC}-0.2		V_{CC}	V	DC Load < 500µA
V_{OL}	Output LOW voltage	0		0.2	V	DC Load < 2mA
V_{OHPU}	V_{OH} with external pull-up	2.4			V	250Ω to 3.3V(5%)
V_{OLPU}	V_{OL} with external pull-up			0.4	V	250Ω to 3.3V(5%)

Table 5: Signal Input Levels (high-speed signal path)

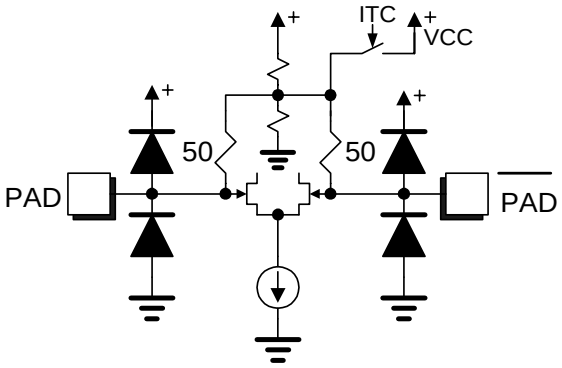
Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IN}	Input voltage amplitude	150		1100	mV	See Note 1
V_{ICM}	Input common-mode voltage	V_{CC}-0.7		V_{CC}-0.2	V	See Note 2

Table 6: Signal Output Levels (high-speed signal path), TERM_CTRL=ON, DRIVE_CTRL=HI

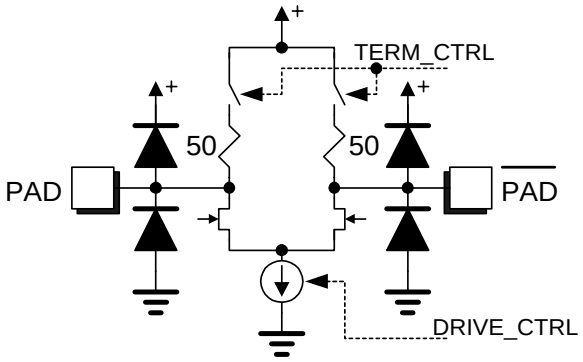
Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OUT}	Output differential voltage	400		600	mV	See Note 1, 3
V_{OCM}	Output common-mode voltage	V_{CC}-0.3		V_{CC}-0.2	V	See Note 2, 3

NOTES: (1) Mean peak-to-peak amplitude measurement of either true or complement of the differential signal.
(2) $V_{CC} = V_{CCP} = 2.5V$, $V_{EE} = 0V$.
(3) Terminated in 50Ω to V_{CC}. This termination is used for testing the part, but other terminations are allowed—see Table 9.

I/O Equivalent Circuits



H/S Input Equivalent Circuit



H/S Output Equivalent Circuit

Input Termination

The high-speed inputs of the VSC838 are internally terminated by a 100Ω impedance between true and complement inputs. Termination resistors are isolated from each other on-chip. The termination will self-bias to +2.0V (nominal) for AC-coupled applications. The ITC pin enables direct interconnection of multiple VSC838 devices. With ITC tied to V_{CC}, the center point of the 100Ω termination impedance is tied to V_{CC}, causing the terminations to act as loads for an open-drain or open-collector differential output.

Table 7: Allowed Input Termination Schemes

Type	*Description*	*Comments*
1	AC-coupled input	Tie ITC LOW, 100Ω differential input termination, input self-biased
2	DC-coupled from open-drain CML	Tie ITC HIGH, terminations acts as 50Ω load to V_{CC}
3	DC-coupled from back-terminated 2.5V CML	Tie ITC HIGH, terminations acts as 50Ω load to V_{CC}
4	DC-coupled from back-terminated 2.5V CML	Tie ITC LOW, 100Ω differential termination (preferred over Type 3)
5	DC-coupled from back-terminated 3.3V LV-PECL	Tie ITC LOW, 100Ω differential termination

Some allowed termination schemes result in additional I_{CC} current and power dissipation on-chip. See Table 8.

Table 8: Additional Current and Power

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
I_{CC-C}	Additional ICC current when receiving DC-Coupled CML (ITC = HIGH)			180	mA	
P_{CC-C}	Additional power dissipated on-chip for DC terminating CML at inputs			0.180	W	

Output Termination

The high-speed outputs of the VSC838 are internally back terminated by 50Ω to V_{CC} when the TERM_CTRL pin is HIGH. When this pin is LOW, the output driver functions as an open-drain CML driver. Setting DRIVE_CTRL LOW (GND) saves 1W under maximum power dissipation conditions. See Table 9 for allowable types of terminations and modes of operation.

Table 9: Allowed High-Speed Output Terminations and Modes of Operation

Type	*Description*	*DRIVE_ CTRL*	*TERM_ CTRL*	*V_{OD}(1) (mV) typ*	*V_{OCM}(1) (V) typ*
1	AC-coupled to 50Ω termination to any voltage	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0
2	AC-coupled to 100Ω differential termination	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0
3	DC-coupled, terminated in 50Ω to V_{CC} at far-end only	GND (LOW)	GND (OFF)	500	2.25
4	DC-coupled, terminated in 50Ω to V_{CC} at far-end only	V_{CC} (HIGH)	GND (OFF)	1000	2.0
5	DC-coupled, source and far-end terminated in 50Ω to V_{CC}	GND (LOW)	V_{CC} (ON)	250	2.375
6	DC-coupled, source and far-end terminated in 50Ω to V_{CC}	V_{CC} (HIGH)	V_{CC} (ON)	500	2.25
7	DC-coupled, 100Ω differential termination	GND (LOW)	V_{CC} (ON)	250	2.25
8	DC-coupled, 100Ω differential termination	V_{CC} (HIGH)	V_{CC} (ON)	500	2.0

NOTE: (1) Measured at output of VSC838, with V_{CC} = 2.5V.

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC}) Potential to GND ..... -0.5V to +4.0V
LVTTL Input Voltage Applied ..... -0.5V to V_{CC}+1.0V
ECL Input Voltage Applied ..... -0.5V to V_{CC} +0.5V
Output Current (I_{OUT}) 50mA
Case Temperature Under Bias (T_C) ..... -55°C to + 125°C
Storage Temperature (T_{STG}) ..... -65°C to + 150°C

NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Operating Conditions

Supply Voltage (V_{EE}) 0V
Supply Voltage (V_{CC}) ..... +2.5V ±5%
Supply Voltage (V_{CCP}) ..... +2.5V ±5%
Case Temperature Operating Range (T) ..... 0°C to 85°CPackage Pin Descriptions

Figure 5: Pinout Diagram -- Bottom View

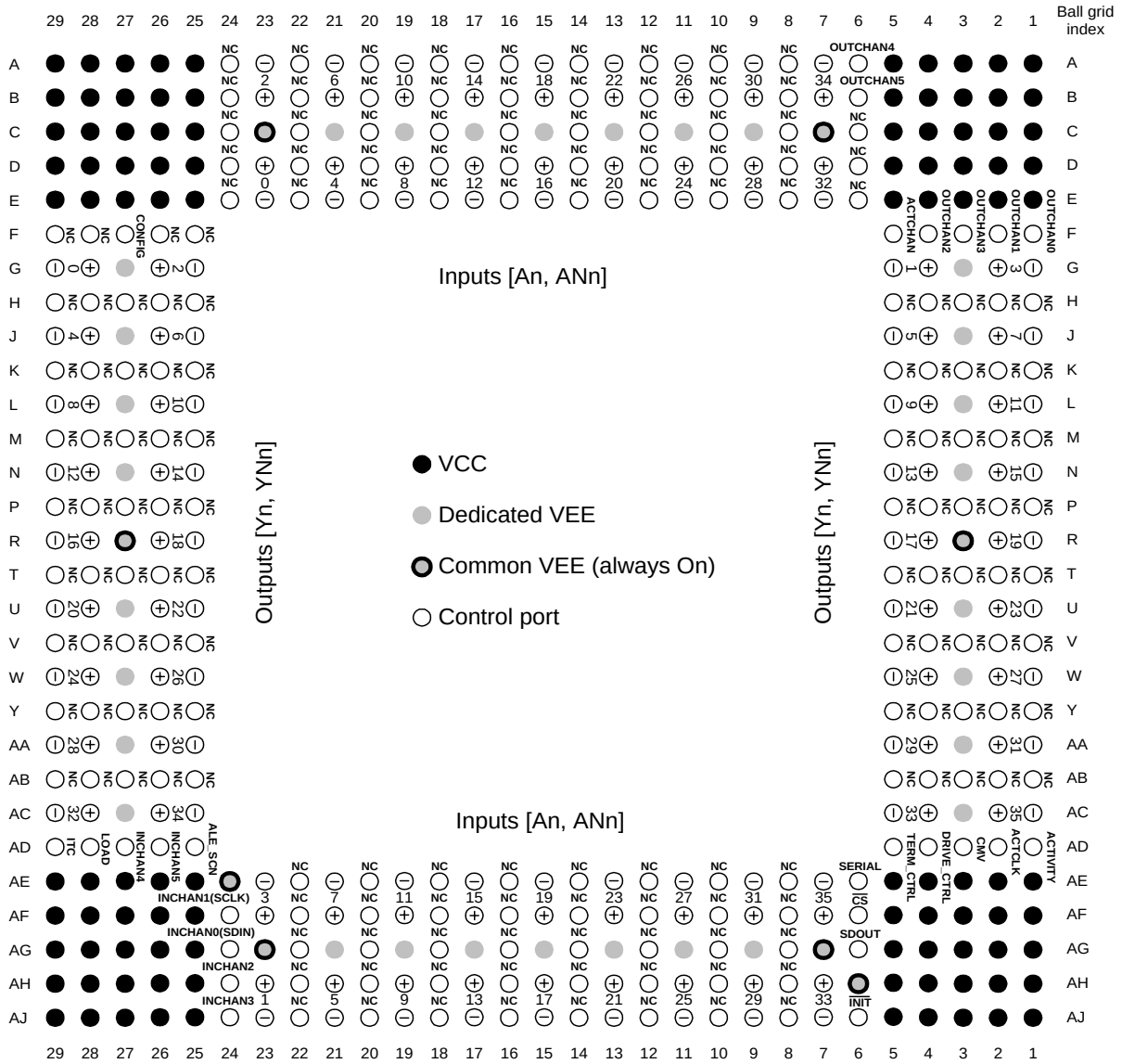


Table 10: Package Pin Indentifications

Signal Name	*Ball*	*Description*	*Level*
High-Speed Data Inputs			
A0, AN0	D23, E23	High-Speed Data Input Channel 0; True, Complement	PECL
A1, AN1	AH23, AJ23	High-Speed Data Input Channel 1; True, Complement	PECL
A2, AN2	B23, A23	High-Speed Data Input Channel 2; True, Complement	PECL
A3, AN3	AF23, AE23	High-Speed Data Input Channel 3; True, Complement	PECL
A4, AN4	D21, E21	High-Speed Data Input Channel 4; True, Complement	PECL
A5, AN5	AH21, AJ21	High-Speed Data Input Channel 5; True, Complement	PECL
A6, AN6	B21, A21	High-Speed Data Input Channel 6; True, Complement	PECL
A7, AN7	AF21, AE21	High-Speed Data Input Channel 7; True, Complement	PECL
A8, AN8	D19, E19	High-Speed Data Input Channel 8; True, Complement	PECL
A9, AN9	AH19, AJ19	High-Speed Data Input Channel 9; True, Complement	PECL
A10, AN10	B19, A19	High-Speed Data Input Channel 10; True, Complement	PECL
A11, AN11	AF19, AE19	High-Speed Data Input Channel 11; True, Complement	PECL
A12, AN12	D17, E17	High-Speed Data Input Channel 12; True, Complement	PECL
A13, AN13	AH17, AJ17	High-Speed Data Input Channel 13; True, Complement	PECL
A14, AN14	B17, A17	High-Speed Data Input Channel 14; True, Complement	PECL
A15, AN15	AF17, AE17	High-Speed Data Input Channel 15; True, Complement	PECL
A16, AN16	D15, E15	High-Speed Data Input Channel 16; True, Complement	PECL
A17, AN17	AH15, AJ15	High-Speed Data Input Channel 17; True, Complement	PECL
A18, AN18	B15, A15	High-Speed Data Input Channel 18; True, Complement	PECL
A19, AN19	AF15, AE15	High-Speed Data Input Channel 19; True, Complement	PECL
A20, AN20	D13, E13	High-Speed Data Input Channel 20; True, Complement	PECL
A21, AN21	AH13, AJ13	High-Speed Data Input Channel 21; True, Complement	PECL
A22, AN22	B13, A13	High-Speed Data Input Channel 22; True, Complement	PECL
A23, AN23	AF13, AE13	High-Speed Data Input Channel 23; True, Complement	PECL
A24, AN24	D11, E11	High-Speed Data Input Channel 24; True, Complement	PECL
A25, AN25	AH11, AJ11	High-Speed Data Input Channel 25; True, Complement	PECL
A26, AN26	B11, A11	High-Speed Data Input Channel 26; True, Complement	PECL
A27, AN27	AF11, AE11	High-Speed Data Input Channel 27; True, Complement	PECL
A28, AN28	D9, E9	High-Speed Data Input Channel 28; True, Complement	PECL
A29, AN29	AH9, AJ9	High-Speed Data Input Channel 29; True, Complement	PECL
A30, AN30	B9, A9	High-Speed Data Input Channel 30; True, Complement	PECL
A31, AN31	AF9, AE9	High-Speed Data Input Channel 31; True, Complement	PECL
A32, AN32	D7, E7	High-Speed Data Input Channel 32; True, Complement	PECL
A33, AN33	AH7, AJ7	High-Speed Data Input Channel 33; True, Complement	PECL
A34, AN34	B7, A7	High-Speed Data Input Channel 34; True, Complement	PECL
A35, AN35	AF7, AE7	High-Speed Data Input Channel 35; True, Complement	PECL

Signal Name	*Ball*	*Description*	*Level*
High-Speed Data Outputs			
Y0, YN0	G28, G29	High-Speed Data Output Channel 0; True, Complement	CML
Y1, YN1	G4, G5	High-Speed Data Output Channel 1; True, Complement	CML
Y2, YN2	G26, G25	High-Speed Data Output Channel 2; True, Complement	CML
Y3, YN3	G2, G1	High-Speed Data Output Channel 3; True, Complement	CML
Y4, YN4	J28, J29	High-Speed Data Output Channel 4; True, Complement	CML
Y5, YN5	J4, J5	High-Speed Data Output Channel 5; True, Complement	CML
Y6, YN6	J26, J25	High-Speed Data Output Channel 6; True, Complement	CML
Y7, YN7	J2, J1	High-Speed Data Output Channel 7; True, Complement	CML
Y8, YN8	L28, L29	High-Speed Data Output Channel 8; True, Complement	CML
Y9, YN9	L4, L5	High-Speed Data Output Channel 9; True, Complement	CML
Y10, YN10	L26, L25	High-Speed Data Output Channel 10; True, Complement	CML
Y11, YN11	L2, L1	High-Speed Data Output Channel 11; True, Complement	CML
Y12, YN12	N28, N29	High-Speed Data Output Channel 12; True, Complement	CML
Y13, YN13	N4, N5	High-Speed Data Output Channel 13; True, Complement	CML
Y14, YN14	N26, N25	High-Speed Data Output Channel 14; True, Complement	CML
Y15, YN15	N2, N1	High-Speed Data Output Channel 15; True, Complement	CML
Y16, YN16	R28, R29	High-Speed Data Output Channel 16; True, Complement	CML
Y17, YN17	R4, R5	High-Speed Data Output Channel 17; True, Complement	CML
Y18, YN18	R26, R25	High-Speed Data Output Channel 18; True, Complement	CML
Y19, YN19	R2, R1	High-Speed Data Output Channel 19; True, Complement	CML
Y20, YN20	U28, U29	High-Speed Data Output Channel 20; True, Complement	CML
Y21, YN21	U4, U5	High-Speed Data Output Channel 21; True, Complement	CML
Y22, YN22	U26, U25	High-Speed Data Output Channel 22; True, Complement	CML
Y23, YN23	U2, U1	High-Speed Data Output Channel 23; True, Complement	CML
Y24, YN24	W28, W29	High-Speed Data Output Channel 24; True, Complement	CML
Y25, YN25	W4, W5	High-Speed Data Output Channel 25; True, Complement	CML
Y26, YN26	W26, W25	High-Speed Data Output Channel 26; True, Complement	CML
Y27, YN27	W2, W1	High-Speed Data Output Channel 27; True, Complement	CML
Y28, YN28	AA28, AA29	High-Speed Data Output Channel 28; True, Complement	CML
Y29, YN29	AA4 , AA5	High-Speed Data Output Channel 29; True, Complement	CML
Y30, YN30	AA26, AA25	High-Speed Data Output Channel 30; True, Complement	CML
Y31, YN31	AA2, AA1	High-Speed Data Output Channel 31; True, Complement	CML
Y32, YN32	AC28, AC29	High-Speed Data Output Channel 32; True, Complement	CML
Y33, YN33	AC4, AC5	High-Speed Data Output Channel 33; True, Complement	CML
Y34, YN34	AC26, AC25	High-Speed Data Output Channel 34; True, Complement	CML
Y35, YN35	AC2, AC1	High-Speed Data Output Channel 35; True, Complement	CML

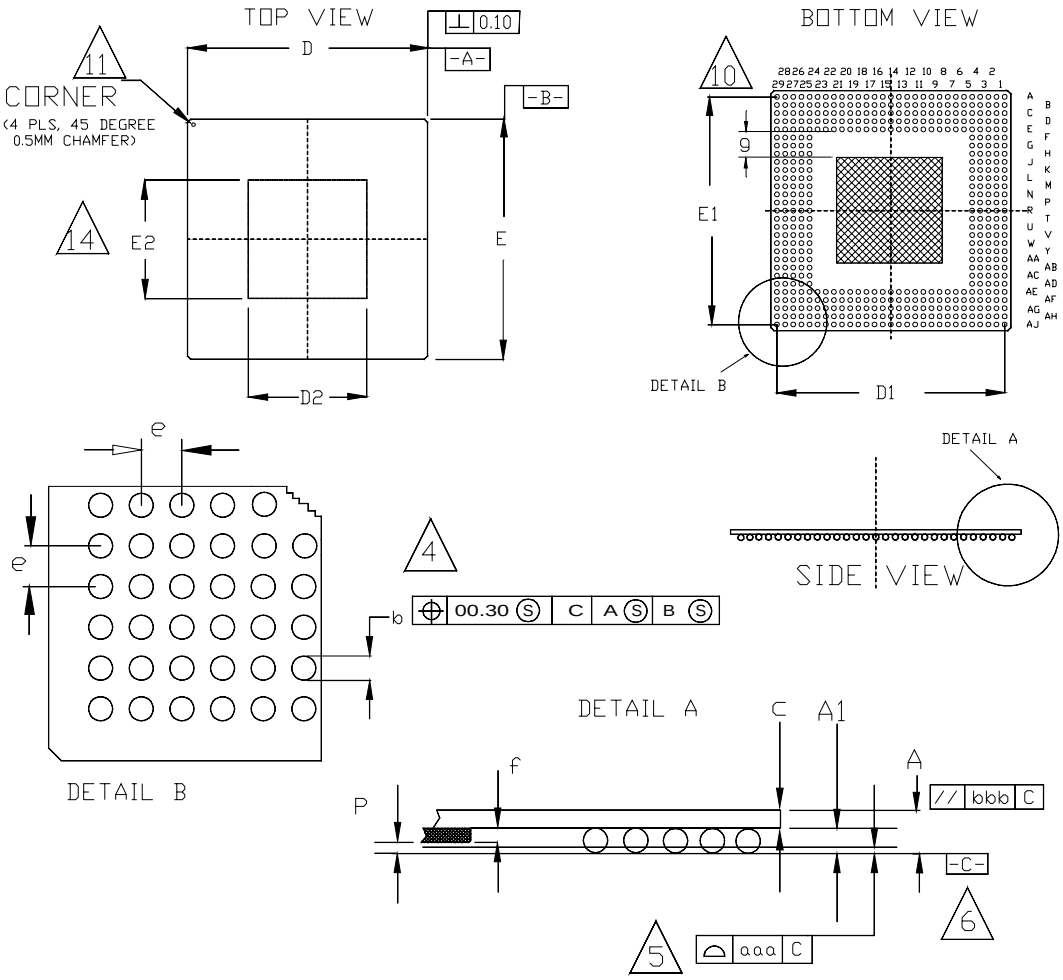
Signal Name	Ball	Description	Level
Control Pins			
ACTCLK	AD2	Clock for Activity Monitor (<10MHz)	LVTTL
ACTIVITY	AD1	ActivityResult from Previous ACTCLK Period	LVTTL
ALE_SCN	AD25	Address Latch Enable for Multiplexed Parallel Mode; Scan Enable for Serial Mode. See Figures 2 through 6 for proper use.	LVTTL
CMV	AD3	Output Drive Current Control (leave floating)	ANALOG
CONFIG	F27	Logic HIGH Transfers Programming to Main Program Memory	LVTTL
$\overline{CS}$	AF6	Chip Select (active LOW)	LVTTL
DRIVE_CTRL	AD4	Output Drive Current Switch (LOW = 10mA, HIGH = 20mA)	LVTTL
INCHAN0 (SDIN)	AG24	Input Channel, Bit 0 and Serial Data in Serial Mode	LVTTL
INCHAN1 (SCLK)	AF24	Input Channel, Bit 1 and Serial Clock in Serial Mode	LVTTL
INCHAN2	AH24	Input Channel, Bit 2	LVTTL
INCHAN3	AJ24	Input Channel, Bit 3	LVTTL
INCHAN4	AD27	Input Channel, Bit 4	LVTTL
INCHAN5	AD26	Input Channel, Bit 5	LVTTL
$\overline{INIT}$	AJ6	$\overline{INIT}$ = 0 Forces “Straight-Through” Program	LVTTL
ITC	AD29	Input Termination Control (GND = floating input termination, V_{CC} = CML mode. See Table 7).	ANALOG
LOAD	AD28	Rising Edge Writes Data in Parallel and Burst Modes, See Figure 5 for Serial Mode	LVTTL
OUTCHAN0	F1	Output Channel, Bit 0	LVTTL
OUTCHAN1	F2	Output Channel, Bit 1	LVTTL
ACTCHAN	F5	Activity Channel Enable bit; HIGH = Enable	LVTTL
OUTCHAN2	F4	Output Channel, Bit 2	LVTTL
OUTCHAN3	F3	Output Channel, Bit 3	LVTTL
OUTCHAN4	A6	Output Channel, Bit 4	LVTTL
OUTCHAN5	B6	Output Channel, Bit 5	LVTTL
SDOUT	AG6	Serial Data Out for Serial Mode and Scan	LVTTL
SERIAL	AE6	SERIAL = 1 (Sets Serial Mode)	LVTTL
TERM_CTRL	AD5	Output Back-Termination Control (LOW = no back term; HIGH = 50Ω back-termination to V_{CC}. See Table 9).	LVTTL

Signal Name	*Ball*	*Description*	*Level*
Power Supplies			
NC	D22, AH22, B22, AF22 D20, AH20, B20, AF20 D18, AH18, B18, AF18 D16, AH16, B16, AF16 D14, AH14, B14, AF14 D12, AH12, B12, AF12 D10, AH10, B10, AF10 D8, AH8, B8, AF8 E22, AJ22, A22, AE22 E20, AJ20, A20, AE20 E18, AJ18, A18, AE18 E16, AJ16, A16, AE16 E14, AJ14, A14, AE14 E12, AJ12, A12, AE12 E10, AJ10, A10, AE10 E8, AJ8, A8, AE8	No Connect	
NC	H28, H4, H26, H2 K28, K4, K26, K2 M28, M4, M26, M2 P28, P4, P26, P2 T28, T4, T26, T2 V28, V4, V26, V2 Y28, Y4, Y26, Y2 AB28, AB4, AB26, AB2 H29, H5, H25, H1 K29, K5, K25, K1 M29, M5, M25, M1 P29, P5, P25, P1 T29, T5, T25, T1 V29, V5, V25, V1 Y29, Y5, Y25, Y1 AB29, AB5, AB25, AB1	No Connect	
NC	E6, D6, C6 A24, B24, D24, E24, C24 F29, F28, F25, F26	No Connect	
VEE	C23, C7, R3, AG7 AG23, R27, AH6, AE24P	Common Negative Power Supply	GND

Signal Name	*Ball*	*Description*	*Level*
VCC	A1, A2, A3, A4, A5 B1, B2, B3, B4, B5 C1, C2, C3, C4, C5 D1, D2, D3, D4, D5 E1, E2, E3, E4, E5 A25, A26, A27, A28, A29 B25, B26, B27, B28, B29 C25, C26, C27, C28, C29 D25, D26, D27, D28, D29 E25, E26, E27, E28, E29 AE1, AE2, AE3, AE4, AE5 AF1, AF2, AF3, AF4, AF5 AG1, AG2, AG3, AG4, AG5 AH1, AH2, AH3, AH4, AH5 AJ1, AJ2, AJ3, AJ4, AJ5 AE25,AE26,AE27,AE28,AE29 AF25,AF26,AF27,AF28,AF29 AG25,AG26,AG27,AG28, AG29 AH25,AH26,AH27,AH28, AH29 AJ25,AJ26,AJ27,AJ28,AJ29	Positive Power Supply	2.5V
NC	C22, C20, C18, C16, C14, C12, C10, C8, AG22, AG20, AG18, AG16, AG14, AG12, AG10, AG8, H3, K3, M3, P3, T3, V3, Y3, AB3, H27, K27, M27, P27, T27, V27, Y27, AB27,	No Connect	
VEEP_T1	C21	Negative Power Supply for Inputs A4/AN4 + A6/AN6	GND
VEEP_T2	C19	Negative Power Supply for Inputs A8/AN8 + A10/AN10	GND
VEEP_T3	C17	Negative Power Supply for Inputs A12/AN12 + A14/AN14	GND
VEEP_T4	C15	Negative Power Supply for Inputs A16/AN16+A18/AN18	GND
VEEP_T5	C13	Negative Power Supply for Inputs A20/AN20+A22/AN22	GND
VEEP_T6	C11	Negative Power Supply for Inputs A24/AN24+A26/AN26	GND
VEEP_T7	C9	Negative Power Supply for Inputs A28/AN28+A30/AN30	GND
VEEP_B1	AG21	Negative Power Supply for Inputs A5/AN5+A7/AN7	GND
VEEP_B2	AG19	Negative Power Supply for Inputs A9/AN9+A11/AN11	GND
VEEP_B3	AG17	Negative Power Supply for Inputs A13/AN13+A15/AN15	GND
VEEP_B4	AG15	Negative Power Supply for Inputs A17/AN17+A19/AN19	GND
VEEP_B5	AG13	Negative Power Supply for Inputs A21/AN21+A23/AN23	GND

Signal Name	*Ball*	*Description*	*Level*
VEEP_B6	AG11	Negative Power Supply for Inputs A25/AN25+A27/AN27	GND
VEEP_B7	AG9	Negative Power Supply for Inputs A29/AN29+A31/AN31	GND
VEEP_L0	G3	Negative Power Supply for Outputs Y1/YN1+Y3/YN3	GND
VEEP_L1	J3	Negative Power Supply for Outputs Y5/YN5+Y7/YN7	GND
VEEP_L2	L3	Negative Power Supply for Outputs Y9/YN9+Y11/YN11	GND
VEEP_L3	N3	Negative Power Supply for Outputs Y13/YN13+Y15/YN15	GND
VEEP_L4	U3	Negative Power Supply for Outputs Y21/YN21+Y23/YN23	GND
VEEP_L5	W3	Negative Power Supply for Outputs Y25/YN25+Y27/YN27	GND
VEEP_L6	AA3	Negative Power Supply for Outputs Y29/YN29+Y31/YN31	GND
VEEP_L7	AC3	Negative Power Supply for Outputs Y33/YN33+Y35/YN35	GND
VEEP_R0	G27	Negative Power Supply for Outputs Y0/YN0+Y2/YN2	GND
VEEP_R1	J27	Negative Power Supply for Outputs Y4/YN4+Y6/YN6	GND
VEEP_R2	L27	Negative Power Supply for Outputs Y8/YN8+Y10/YN10	GND
VEEP_R3	N27	Negative Power Supply for Outputs Y12/YN12+Y14/YN14	GND
VEEP_R4	U27	Negative Power Supply for Outputs Y20/YN20+Y22/YN22	GND
VEEP_R5	W27	Negative Power Supply for Outputs Y24/YN24+Y26/YN26	GND
VEEP_R6	AA27	Negative Power Supply for Outputs Y28/YN28+Y30/YN30	GND
VEEP_R7	AC27	Negative Power Supply for Outputs Y32/YN32+Y34/YN34	GND

Package Information - 37.5mm 480 BGA



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.45	1.55	1.65
A1	0.60	0.65	0.70
D	37.30	37.50	37.70
D1	35.56 (BSC.)		
E	37.30	37.50	37.70
E1	35.56 (BSC.)		
b	0.65	0.75	0.85
c	0.85	0.90	0.95
f	0.30	0.35	0.40
M	29		
N	480		
aaa			0.15
bbb			0.15
e	1.27 TYP.		
P	0.15		
g	0.40		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C-
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C-
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE BLACK OXIDE.
8. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
9. SUBSTRATE MATERIAL BASE IS COPPER.
10. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF PACKAGE BODY
11. 45 DEG. 0.5 mm CHAMFER CORNER AND WHITE DOT FOR PIN1 IDENTIFICATION.

Ordering Information

The order number for this product is formed by a combination of the device type and package type.

VSC838 **XX**

Device Type
OC-48 36x37 Crosspoint Switch

Package Style
UG: 480 TBGA, 37.5mm Body

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