T-46-07-09

GigaBit Logic

10G024
10G024K

Quad D Flip Flop with XOR Inputs
1.9 GHz Clock Rate
10G PicoLogic™ Family

2

FEATURES

- 850 ps typical clock to output delay
- Individual or common clock inputs
- Differential outputs with common output enable control
- Common asynchronous clear control
- ECL and PicoLogic™ compatible I/O
- Extended Temp. Range: -40°C to +100°C (10G024K)
- Temperature and voltage compensated design
- ≤ 50 ps clock to output delay skew
- Ouput Wire-OR capability
- Available in 40 pin C-Leaded and Leadless chip carriers or die form

APPLICATIONS

- Cyclic Redundancy Check Code Generation
- Bit Extender for 10G061 Synchronous Counter
- Toggle (T) flip-flop with SEL as the toggle control
- Complementing Register for Subtraction
- Pseudo-random Word Generator
- Synchronous set-reset (S-R) flip-flop with $\overline{DA}$ as reset input and DB as the set input.

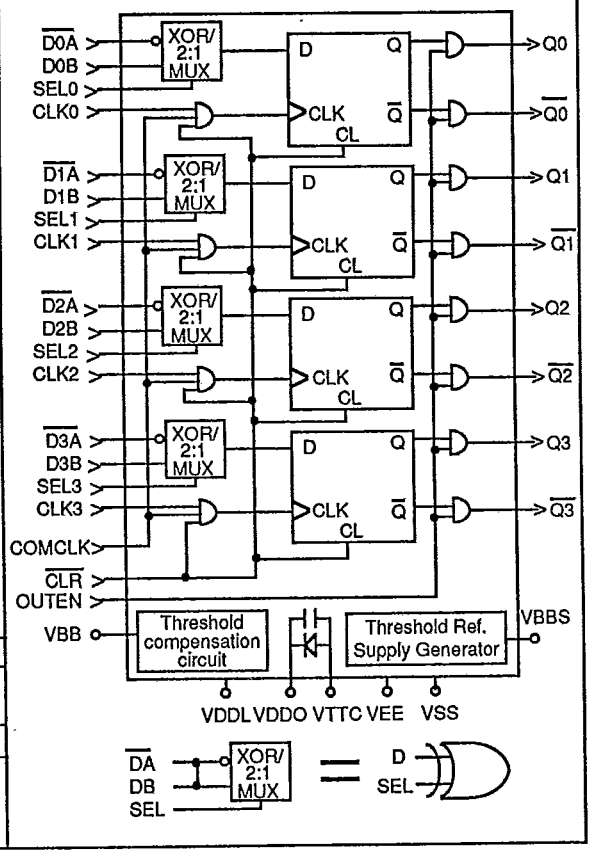
FUNCTIONAL DESCRIPTION

The 10G024 is a Gallium Arsenide quad D-type flip flop with XOR gate or 2:1 MUX data inputs (D0A-D3A, D0B-D3B). When the $\overline{DA}$ and DB inputs are connected together, data to each of the four stages is the XOR of this input and the SEL input, and is latched into the flip flop by the rising edge of either the individual clock inputs (CLK0-CLK3) or the common clock input (COMCLK). An active low common clear ($\overline{CLR}$) input is provided for resetting each flip flop asynchronously to a low level. All device outputs can be disabled (brought low), without interfering with the current state of the flip flop, via the output enable (OUTEN) control. This permits wired-OR bus connection.

The 10G024 can be clocked at 2.1 GHz typically. Clock to output delay at room temp. is 850 ps and the skew in output delay time is tightly matched to 30 ps which results in a highly symmetric output eye pattern.

The 10G024 is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G024 ORDERING INFORMATION

Package Type	Min. Speed 0°C to 85°C		Min. Speed -40°C to 100°C
	1.9 GHz	1.6 GHz	1.0 GHz
C-Leaded CC	10G024-2C	10G024-3C	10G024-2C
Leadless CC	10G024-2L	10G024-3L	10G024-2L
Dice		10G024-3X	10G024-2X

GigaBit Logic

10G024
10G024K

10G024 OPERATION (Truth Table with XOR Gate Inputs Configured)							
Function	$\overline{CLR}$	OE	CLKn	COMCLK	$\overline{DnA}$ = DnB	SEL	Output Qn (t+1)
Clear *	L	H	X	X	X	X	L
Output Disabled	H	L	L or H	L or H	X	X	L
Output Enabled	H	H	L or H	L or H	X	X	Qn(t)
XOR	H	H	⊓⊔	H	0	0	0
XOR	H	H	⊓⊔	H	0	1	1
XOR	H	H	H	⊓⊔	1	0	1
XOR	H	H	H	⊓⊔	1	1	0
Clock Disabled	H	H	L	⊓⊔	X	X	Qn(t)
Clock Disabled	H	H	⊓⊔	L	X	X	Qn(t)

10G024 OPERATION (Truth Table with 2:1 MUX Inputs Configured)								
Function	SELn	$\overline{CLR}$	OE	CLKn	COMCLK	$\overline{DnA}$	DnB	Qn (t+1)
Clear *	X	L	H	X	X	X	X	L
Output Disabled	X	H	L	L or H	L or H	X	X	L
Output Enabled	X	H	H	L or H	L or H	X	X	Qn(t)
Select A	H	H	H	⊓⊔	H	$\overline{DnA(t)}$	X	$\overline{DnA(t)}$
Select B	L	H	H	⊓⊔	H	X	DnB(t)	$\overline{DnB(t)}$
Select A	H	H	H	H	⊓⊔	$\overline{DnA(t)}$	X	$\overline{DnA(t)}$
Select B	L	H	H	H	⊓⊔	X	DnB(t)	DnB(t)
Clock Disabled	X	H	H	L	⊓⊔	X	X	Qn(t)
Clock Disabled	X	H	H	⊓⊔	L	X	X	Qn(t)

The operation of the 10G024 is described in the truth tables above. The device is configured for XOR gate inputs by connecting together the DA and DB inputs and using this as one XOR input, the other being the SEL input. With the inputs configured for 2:1 Muxing, when SEL is high, A data are selected. When SEL is low, B data are selected. All flip flop stages are reset to low by bringing CLR low at any time. All outputs can be turned off for bus connection, without altering the current state of the flip flops, by bringing OUTEN low.

Data are clocked into the flip flop assuming the appropriate setup and hold time requirements are met. At any time, the clock input can be disabled by setting the unused clock input(s) low. The current state of each flip flop is maintained in this case.

* When both clock signals are in the high state, application of $\overline{CLR}$ will cause data at the inputs to be clocked into the flip-flops at the rising edge of the $\overline{CLR}$ pulse. Hence, avoid reseting $\overline{CLR}$ (returning to the high state) when both CLKn and COMCLK are high.

PIN DESCRIPTIONS

$\overline{D0A}$ - $\overline{D3A}$	A data inputs
D0B - D3B	B data inputs
SEL0-SEL3	MUX select or XOR gate inputs
CLK0 - CLK3	Individual flip flop clock inputs
COMCLK	Common clock input to all four flip flops
$\overline{CLR}$	Active low asynchronous clear control
OUTEN	Active high output enable control
Q0 - Q3	True data outputs
$\overline{Q0}$ - $\overline{Q3}$	Complement data outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	AC return lead for the package internal VDDO decoupling capacitor. Typically connect to VTT.
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult App. Note 4 for detail.
VBB	Reference input to the 10G024's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving the 10G024 from ECL. Connect to the VBBS pin when the 10G024 is driven from PicoLogic™. This pin may not be left unconnected.
VBBS	PicoLogic™ threshold reference output voltage. Connect to VBB when driving from PicoLogic™.

GigaBit Logic

10G024
10G024K

CRC ERROR DETECTION SCHEMES

DEFINITION:

Cyclical redundancy check (CRC) is an efficient method to detect errors in digital transmission systems. CRC codes are the remainder (R(x)) of the division between the data to be transmitted (M(x)) and a standard check polynomial P(x).

$$M(x) = Q(x) \cdot P(x) + R(x)$$

The code R(x) is appended to the serial data M(x). Therefore, the data transmitted becomes T(x) = M(x) + R(x).

CRC error detection uses modulo - 2 arithmetic. Since modulo - 2 has no carries or borrows, addition and substraction yield the same result. Hence,

$$T(x) = M(x) + R(x) = M(x) - R(x) = Q(x) \cdot P(x)$$

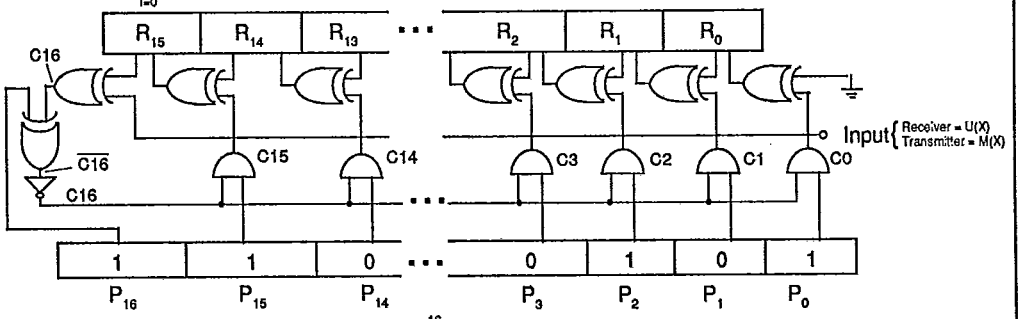
To check the validity of the data, the receiver simply divides the received data U(x) by the same standard polynomial P(x). If there are no errors, U(x) is equal to the transmitted polynomial T(x), and the division results in a remainder of zero.

$$\frac{U(x)}{P(x)} = \frac{T(x)}{P(x)} = \frac{Q(x) \cdot P(x)}{P(x)} = Q(x) + 0$$

CRC 16 CODE IMPLEMENTATION

a) Conceptual Diagram

Transmitter: $R(X) = \sum_{i=0}^{15} R_i X^i$ [Remainder of M(X)/P(X)]; Receiver: R(X)=0 if no errors [Remainder of U(X)/P(X)]

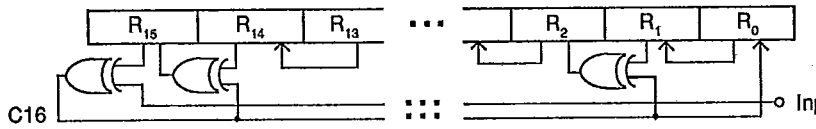


$$P(X) = \sum_{i=0}^{16} P_i X^i = X^{16} + X^{15} + X^2 + 1$$

b) Simplified Diagram [M(X)/P(X) or U(X)/P(X)]

$P_i=0 \rightarrow Ci=0 \rightarrow R_{i-1} \oplus Ci = R_{i-1} \oplus 0 = R_{i-1};\ 0 \le i \le 15$

$P_i=1 \rightarrow Ci=C16 = \overline{(R_{15} \oplus Input) \oplus 1} = \overline{\overline{R_{15} \oplus Input}} = R_{15} \oplus Input;\quad P_{16} = 1;\ 0 \le i \le 15$



NOTE: CRC recommended references: C. Deierling, "Exclusive-OR inputs give you many uses for GaAs flip-flop" Article Reprint AR-19 (See Section 8); Krishna Rallapa, "CRC error detection schemes ensures data accuracy." EDN, (September 5, 1978), pg. 119.

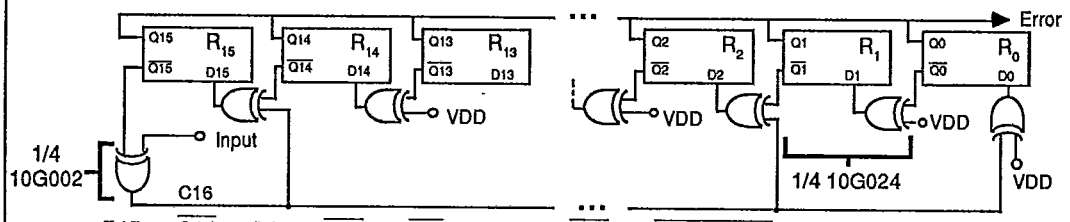
GigaBit Logic

10G024
10G024K

CRC 16 IMPLEMENTATION USING FOUR 10G024's AND ONE 10G002

CRC 16 CHECKER:

In order to check if the remainder is 0 (no error), we suggest to wire-OR the Q outputs of all flip-flops. Therefore, only $\overline{Q}$ is available to perform the division.



$D15 = \overline{Q14} \oplus C16 = \overline{Q14} \oplus (\overline{Q15} \oplus Input) = \overline{Q14} \oplus (\overline{Q15 \oplus Input}) = Q14 \oplus (Q15 \oplus Input)$

NOTE: R_4 to R_{11} (two 10G024's) can be replaced by one 10G022

CRC 16 GENERATOR: Same circuit as above except:

1). A disable should be added to force C16 to VDD and allow the 10G024's to function as shift registers only, Q15 being the output.

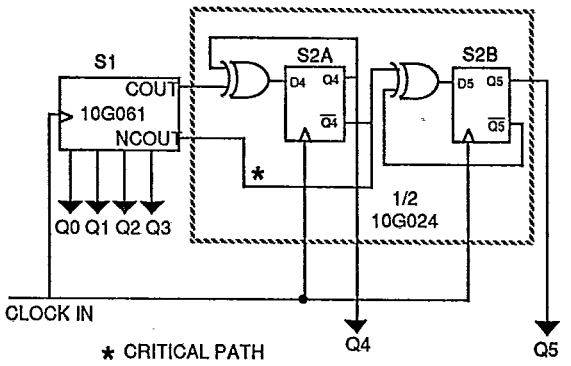
2). Q15 should be muxed with the input in order for the transmitted data to be alternatively the input [M(X)] or Q15 [remainder R(X) appended to M(X)].

TWO BIT SYNCHRONOUS EXTENSION OF THE 10G061 USING THE 10G024

TRUTH TABLE AT COUNT 1110 OF Q1

10G061 Count	Cout	Q4	D4	Q4•Cout	Q5	D5	
1110	0	0	0	0	0	0	
1111	1	0	1	0	0	0	
0000	0	1	1	0	0	0	16 Counts*
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
1110	0	1	1	0	0	0	
1111	1	1	0	1	0	1	
0000	0	0	0	0	1	1	16 Counts*
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
1110	0	0	0	0	1	1	
1111	1	0	1	0	1	1	
0000	0	1	1	0	1	1	16 Counts*
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
1110	0	1	1	0	1	1	
1111	1	1	0	1	1	0	
0000	0	0	0	0	0	0	

• If N 10G061 are cascaded, then counts = 16^N



$D5 = \overline{(\overline{Q4} + \overline{Cout})} \oplus \overline{Q5}$
$= (Q4 \cdot Cout) \oplus Q5$
$= (Q4 \cdot Cout) \oplus Q5$
$D4 = Q4 \oplus Cout$

S1 is a 10G061 counter in free counting mode (please refer to the 10G061 datasheet, pg. 3, for more details). When the 10G061 reaches 15 (1111, i.e. terminal count), COUT pulses high for one clock period. This causes S2A to toggle since $D4=\overline{Q4}=Q4 \oplus 1$. This circuit could be expanded to multiple 10G061 counters with S1 being the most significant counter.

GigaBit Logic

10G024
10G024K

DC CHARACTERISTICS

Tc = -40°C to 100°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I in 1	Input Current; Data, Sel, CLKn	-500	200	500	µA	VIN = -1.0 V to -1.6 V
I in 2	Input Current; COMCLK, CLR, OUTEN	-1000	500	1000	µA	
ISS	Power Supply Current (10G024)		260	340	mA	
ISS	Power Supply Current (10G024K)		260	375	mA	
IEE	Power Supply Current (10G024)		35	65	mA	
IEE	Power Supply Current (10G024K)		35	70	mA	
VIH	Input High Voltage (10G024K)	-0.8			V	
VIL	Input Low Voltage (10G024K)			-1.8	V	
PD	Power Dissipation (10G024)		1.0	1.5	W	
PD	Power Dissipation (10G024K)		1.0	1.7	W	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Notes 1, 2)

VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

		10G024-2							10G024-3							
		Tc= 0° C		Tc= 25° C			Tc= 85° C		Tc= 0° C		Tc= 25° C			Tc= 85° C		
SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNITS
1/Tc1	Individual clock freq.	1.9		1.9	2.1		1.9		1.6		1.6	1.8		1.6		GHz
1/Tc2	Common clock freq.	1.6		1.6	1.8		1.6		1.3		1.3	1.5		1.3		GHz
Tsd	Data setup time	-50		-50			-50		-40		-40			-40		ps
Tss	SEL setup time	-50		-50			-50		-40		-40			-40		ps
Thd	Data hold time	250		250			250		275		275			275		ps
Ths	SEL hold time	150		150			150		165		165			165		ps
Tdod	Output disable delay	375	650	350	500	550	350	650	400	700	350	550	600	400	700	ps
Tdoe	Output enable delay	350	600	350	450	500	350	600	350	650	350	500	550	350	650	ps
Twc	Clear pulse width	500					500		550					550		ps
Tdc	Output clear delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdhl	Clock to output H-L delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
Tdlh	Clock to output L-H delay	600	950	600	850	900	600	950	600	1050	600	975	1000	600	1050	ps
	Clock to output skew		50		30	50		50		50		30	50		50	ps
Tr	Output rise time		175		175			200		200		175			225	ps
Tf	Output fall time		150		125			150		175		125			175	ps

NOTES:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

GigaBit Logic

10G024
10G024K

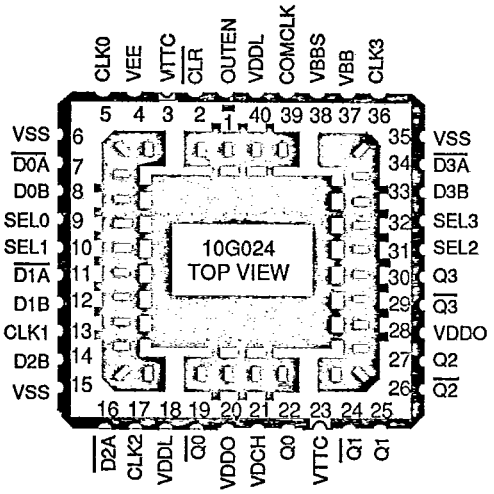
AC CHARACTERISTICS (Notes 1, 2)

VSS= -3.5V to -3.3V, VEE= -5.5V to -5.1V, VDDL=VDDO=Gnd., unless otherwise indicated

SYMBOL	PARAMETER	10G024K-2							UNITS
		Tc= -40° C		Tc= 25° C			Tc= 100° C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
1/Tc1	Individual clock freq.	1.0		1.9	2.1		1.0		GHz
1/Tc2	Common clock freq.	0.8		1.6	1.8		0.8		GHz
Tsd	Data setup time	-40		-50			-40		ps
Tss	SEL setup time	-40		-50			-40		ps
Thd	Data hold time	275		250			275		ps
Ths	SEL hold time	165		150			165		ps
Tdod	Output disable delay	400	700	350	500	550	400	700	ps
Tdoe	Output enable delay	350	650	350	450	500	350	650	ps
Twc	Clear pulse width	550					550		ps
Tdc	Output clear delay	600	1050	600	850	900	600	1050	ps
Tdhl	Clock to output H-L delay	600	1050	600	850	900	600	1050	ps
Tdlh	Clock to output L-H delay	600	1050	600	850	900	600	1050	ps
	Clock to output skew		50		30	50		50	ps
Tr	Output rise time		200		175			225	ps
Tf	Output fall time		175		125			175	ps

NOTES:
1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

PIN FUNCTIONS - PACKAGE TYPES "L" AND "C"



NOTE: Pin 1 is marked for orientation.

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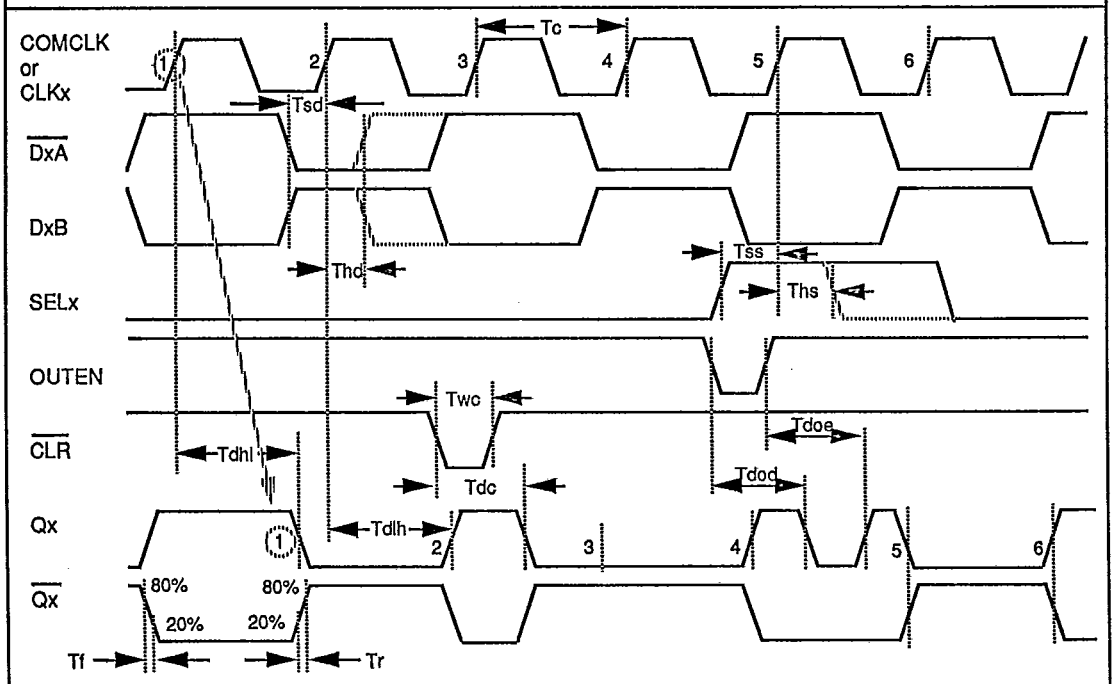
10G024
10G024K

SWITCHING WAVEFORMS



NOTES

T-90-20

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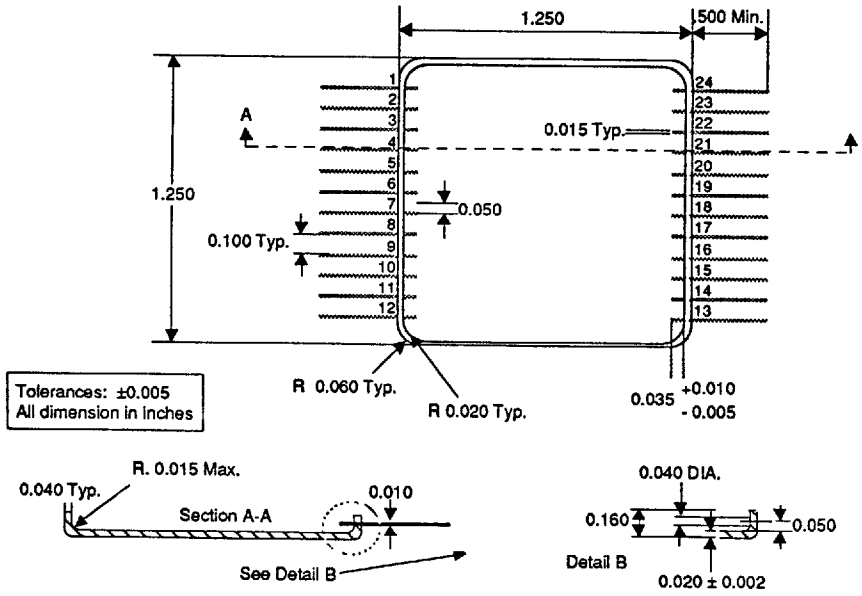
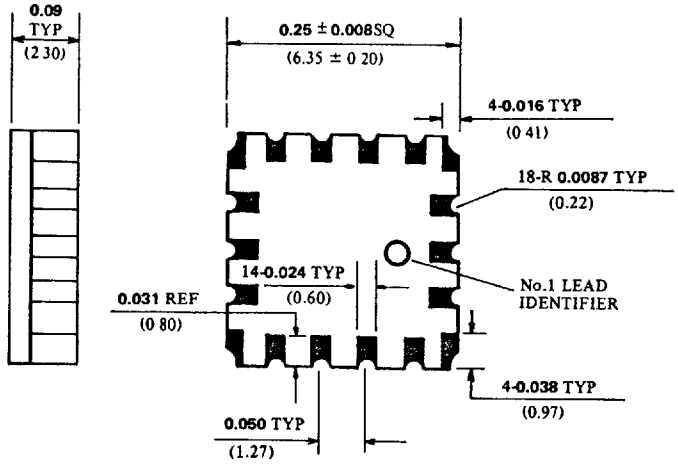
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

11

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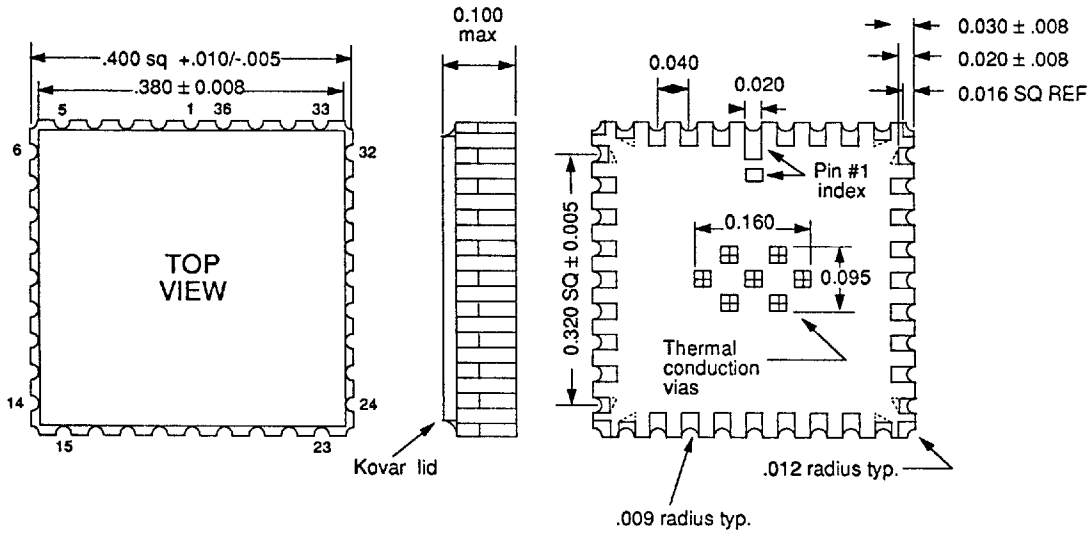
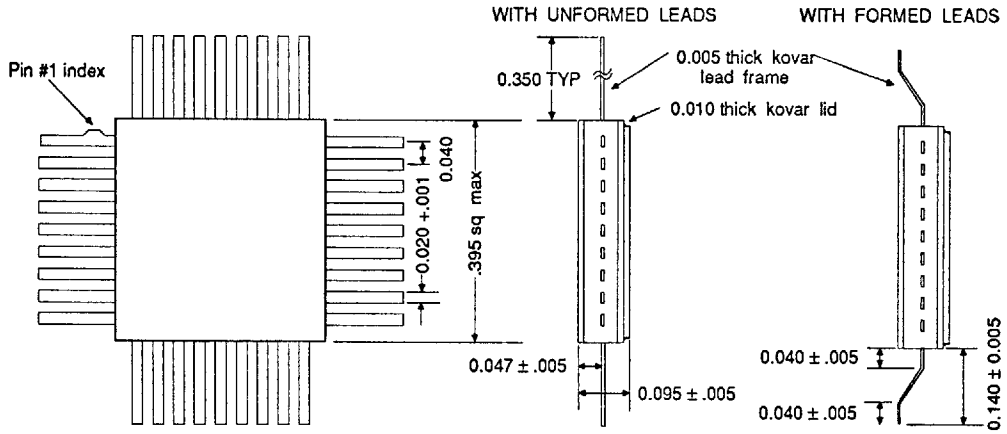
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



T-90-20

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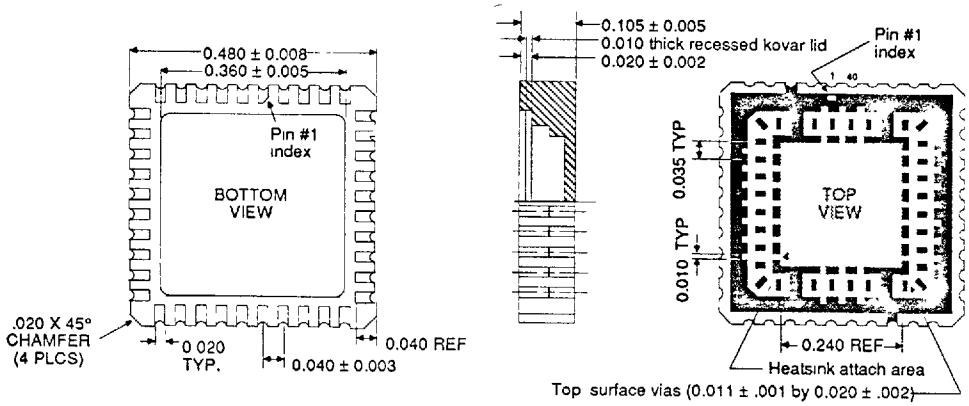
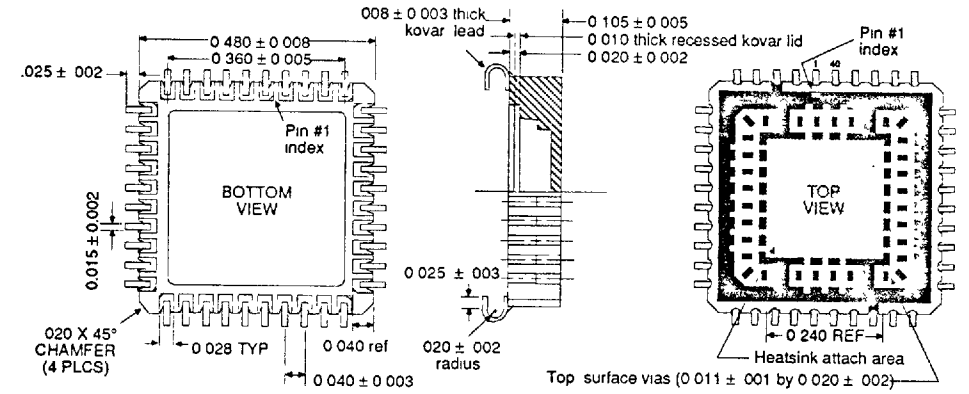
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

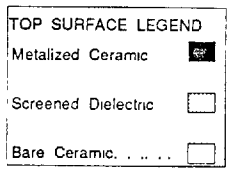


40 PIN LEADED CHIP CARRIER
TYPE C

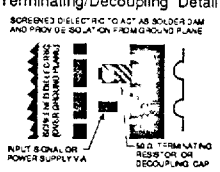


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



T-90-20

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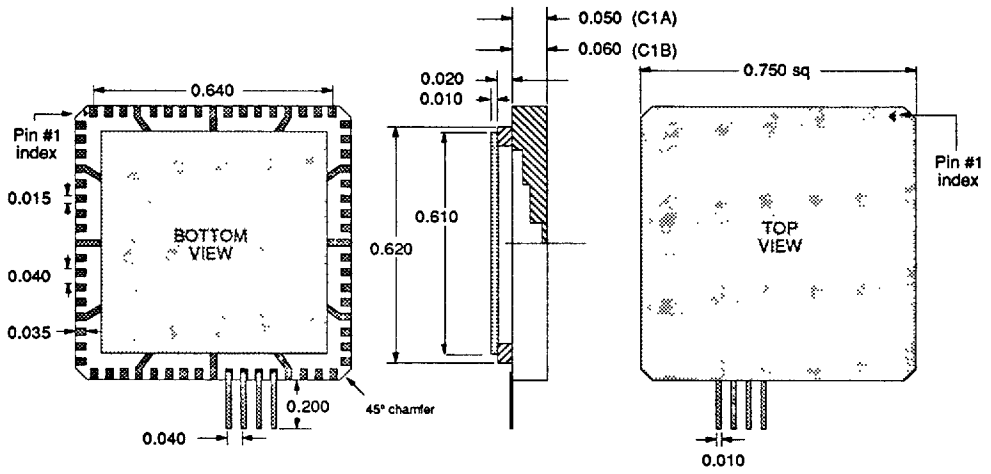
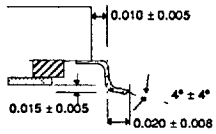
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3