

# 4 Pin µP Voltage Supervisor with Manual Reset

# **General Description**

The ASM811/ASM812 are cost effective low power supervisors designed to monitor voltage levels of 3.0V, 3.3V and 5.0V power supplies in low-power microprocessor ( $\mu$ P), microcontroller ( $\mu$ C) and digital systems. They provide excellent reliability by eliminating external components and adjustments.

A reset signal is issued if the power supply voltage drops below a preset reset threshold and is asserted for at least 140ms after the supply has risen above the reset threshold. The ASM811 has an active-low output  $\overline{RESET}$  that is guaranteed to be in the correct state for  $V_{CC}$  down to 1.1V. The ASM812 has an active-high RESET output. The reset comparator is designed to ignore fast transients on  $V_{CC}.$  A debounced manual reset input allows the user to manually reset the systems to bring them out of locked state.

Low power consumption makes the ASM811/ASM812 ideal for use in portable and battery operated equipment. The ASM811/ ASM812 are available in a compact 4-pin SOT-143 package and thus use minimal board space.

**Applications** 

- · Computers and Controllers
- Embedded controllers
- Portable/Battery operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment
- · Automotive systems
- · Safety Systems

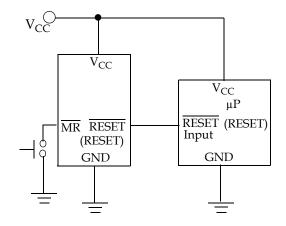
Six voltage thresholds are available to support 3V to 5V systems:

RESET THRESHOLD				
Suffix	Voltage			
L	4.63			
M	4.38			
J	4.00			
Т	3.08			
S	2.93			
R	2.63			

### **Features**

- · New 4.0V threshold option
- 9µA supply current
- Monitor 5V, 3.3V and 3V supplies
- · Manual reset input
- 140ms min. reset pulse width
- Guaranteed over temperature
- Active-low reset valid with 1.1V supply (ASM811)
- Small 4-pin SOT-143 package
- · No external components
- Power-supply transient-immune design

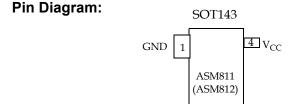
### **Typical Operating Circuit**



# October 2003



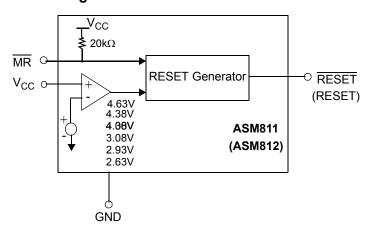
### rev 1.0



(RESET) RESET 2

3 MR

# **Block Diagram**



# **Pin Description**

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Pi	n #	Pin	Eurotion
ASM811	ASM812	Name	Function
1	1	GND	Ground.
2	-	RESET	$\overline{\text{RESET}}$ is asserted LOW if $V_{CC}$ falls below $V_{TH}$ and remains LOW for $T_{RST}$ after $V_{CC}$ exceeds the Threshold. In addition, $\overline{\text{RESET}}$ is active LOW as long as the manual reset is low.
-	2	RESET	RESET is asserted HIGH if $V_{CC}$ falls below $V_{TH}$ and remains HIGH for $T_{RST}$ after $V_{CC}$ exceeds the threshold. In addition, RESET is active HIGH as long as the manual reset is low.
3	3	MR	Manual Reset Input. A logic LOW on $\overline{\text{MR}}$ asserts reset. Reset remains active as long as $\overline{\text{MR}}$ is LOW and for T <sub>MRST</sub> after $\overline{\text{MR}}$ returns HIGH. The active low input has an internal 20k $\Omega$ pull-up resistor. The input should be left open if not used. It can be driven by TTL or CMOS logic or shorted to ground by a switch.
4	4	V <sub>CC</sub>	Power supply input voltage (3.0V, 3.3V, 5.0V)

# **Detailed Description**

A proper reset input enables a microprocessor / microcontroller to start in a known state. ASM811/812 assert reset to prevent code execution errors during power-up, power-down and brown-out conditions.

### **Reset Timing**

The reset signal is asserted- LOW for the ASM811 and HIGH for the ASM812- when the  $V_{CC}$  supply voltage falls below the threshold trip voltage and remains asserted for 140ms minimum after the  $V_{CC}$  has risen above the threshold.

# Manual Reset (MR) Input

A logic low on  $\overline{MR}$  assserts  $\overline{RESET}$  LOW on the ASM811 and RESET HIGH on the ASM812.  $\overline{MR}$  is internally pulled high through a  $20k\Omega$  resistor and can be driven by TTL/CMOS gates or with open collector/drain outputs.  $\overline{MR}$  can be left open if not used.  $\overline{MR}$  may be connected to ground through a normally-open momentary switch without an external debounce circuit.

A  $0.1\mu F$  capacitor from  $\overline{MR}$  to ground can be added for additional noise immunity.



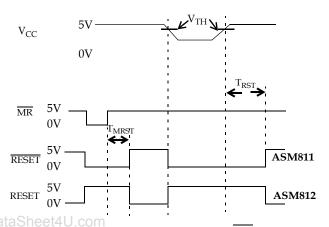


Figure 1: Reset Timing and Manual Reset (MR)

# Power Supply $\overline{MR}$ $\overline{RESET}$ $\overline{MR}$ $\overline{RESET}$

Figures 2 & 3: RESET valid with V<sub>CC</sub> under 1.1V

# **Reset Output Operation**

In  $\mu P$  /  $\mu C$  systems it is important to have the processor and the system begin operation from a known state. A reset output to a processor is provided to prevent improper operation during power supply sequencing or low voltage brown-out conditions.

The ASM811/812 are designed to monitor the system power supply voltages and issue a reset signal when the levels are out of range. RESET outputs are guaranteed to be active for  $V_{CC}$  above 1.1V. When  $V_{CC}$  exceeds the reset threshold, an internal timer keeps RESET active for the reset timeout period, after which RESET becomes inactive (HIGH for the ASM811 and LOW for the ASM812). If  $V_{CC}$  drops below the reset threshold, RESET automatically becomes active. Alternatively, external circuitry or an operator can initiate this condition using the Manual Reset ( $\overline{\rm MR}$ ) pin.  $\overline{\rm MR}$  can be left open if it is not used.  $\overline{\rm MR}$  can be driven by TTL/CMOS logic or even an external switch.

# Valid Reset with V<sub>CC</sub> under 1.1V

To ensure logic inputs connected to the ASM811  $\overline{\text{RESET}}$  pin are in a known state when  $V_{CC}$  is under 1.1V, a  $100 \text{k}\Omega$  pull-down resistor at  $\overline{\text{RESET}}$  is needed. The value is not critical. A  $100 \text{k}\Omega$  pull-up resistor to  $V_{CC}$  is needed with the ASM812.

# **Application Information**

### **Negative VCC Transients**

Typically short duration transients of 100mV amplitude and 20 $\mu$ s duration do not cause a false RESET. A 0.1 $\mu$ F capacitor at V<sub>CC</sub> increses transient immunity.

### **Bidirectional Reset Pin Interfacing**

The ASM811/812 can interface with  $\mu P$  /  $\mu C$  bi-directional reset pins by connecting a 4.7k $\Omega$  resistor in series with the ASM811/812 reset output and the  $\mu P/\mu C$  bi-directional reset input pin.

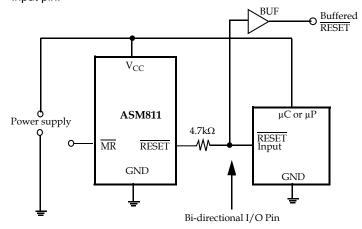


Figure 4: Bi-directional Reset Pin Interface



# **Absolute Maximum Ratings, Table 1:**

1				
	Parameter	Min	Max	Units
	Pin Terminal Voltage With Respect To Groun			
	V <sub>cc</sub>	-0.3	6.0	V
	RESET, RESET and MR	-0.3	V <sub>CC</sub> + 0.3	V
www.Doto	Input current at V <sub>CC</sub> and MR		20	mA
www.Data	Output current: RESET, RESET		20	mA
	Rate of Rise at V <sub>CC</sub>		100	V/µs

Note: These are stress ratings only and the functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.

# **Absolute Maximum Ratings, Table 2:**

Parameter	Min	Max	Units
Power Dissipation (T <sub>A</sub> = 70°C) Derate SOT-143 4mW/°C above 70°C		320	uW
Operating temperature range	-40	105	°C
Storage temperature range	-65	160	°C
Lead temperature (Soldering, 10 sec)		300	°C

Note: These are stress ratings only and the functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.



# **Electrical Characteristics:**

Unless otherwise noted,  $V_{CC}$  is over the full voltage range,  $T_A$  = -40°C to 105°C.

Typical values at  $T_A = 25^{\circ}C$ ,  $V_{CC} = 5V$  for L/M/J devices,  $V_{CC} = 3.3V$  for T/S devices and  $V_{CC} = 3V$  for R devices.

	Symbol	Parameter	Cond	itions	Min	Тур	Max	Unit
	V <sub>CC</sub>	Input Voltage Range	$T_{A} = 0^{\circ}C$ $T_{A} = -40^{\circ}C$		1.1 1.2		5.5 5.5	V V
Data	I <sub>cc</sub> Sheet4U.	Supply Current (Unloaded)	$T_A$ = -40°C to 85°C $T_A$ = -40°C to 85°C $T_A$ = 85°C to 105°C $T_A$ = 85°C to 105°C	$V_{CC}$ < 5.5V, L/M/J $V_{CC}$ < 3.6V, R/S/T $V_{CC}$ < 5.5V, L/M/J $V_{CC}$ < 3.6V, R/S/T		9 6.8	15 10 25 20	μА
			L devices	$T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } 85^{\circ}C$ $T_A = 85^{\circ}C \text{ to } 105^{\circ}C$	4.56 4.50 4.40	4.63	4.70 4.75 4.86	
			M devices	$T_A = 25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } 85^{\circ}C$ $T_A = 85^{\circ}C \text{ to } 105^{\circ}C$	4.31 4.25 4.16	4.38	4.45 4.50 4.56	V
	V <sub>TH</sub> Reset Threshold		J devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ $T_A = 85^{\circ}\text{C to }105^{\circ}\text{C}$	3.93 3.89 3.80	4.00	4.06 4.10 4.20	
		Reset Inresnola	T devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ $T_A = 85^{\circ}\text{C to }105^{\circ}\text{C}$	3.04 3.00 2.92	3.08	3.11 3.15 3.23	
			S devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ $T_A = 85^{\circ}\text{C to }105^{\circ}\text{C}$	2.89 2.85 2.78	2.93	2.96 3.00 3.08	
			R devices	$T_A = 25^{\circ}\text{C}$ $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ $T_A = 85^{\circ}\text{C to }105^{\circ}\text{C}$	2.59 2.55 2.50	2.63	2.66 2.70 2.76	
	TC <sub>VTH</sub>	Reset Threshold Temp. Coefficient				30		ppm/°C
		V <sub>CC</sub> to Reset Delay	V <sub>CC</sub> = V <sub>TH</sub> to (	V <sub>TH</sub> - 125mV),		60		μs
			T <sub>A</sub> = 0°C to 70°C		140		560	
		Reset Active Timeout Period	T <sub>A</sub> = -40°C	T <sub>A</sub> = -40°C to 105°C		240	840	ms
	t <sub>MR</sub>	MR Minimum Pulse Width			10			μs

### Notes

- $1. \underline{Production} \ testing \ done \ at \ TA = 25^{\circ}C. \ Over-temperature \ specifications \ guaranteed \ by \ design \ only \ using \ six \ sigma \ design \ limits.$
- 2. RESET output is active LOW for the ASM811 and RESET output is active HIGH for the ASM812.
- 3. Glitches of 100ns or less typically will not generate a reset pulse.



Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
	MR Glitch Immunity	Note 3		100		ns	
t <sub>MD</sub>	MR to RESET Propogation Delay	Note 2		0.5		μs	
V <sub>IH</sub>	MR Input Threshold	V <sub>CC</sub> > V <sub>TH</sub> (MAX),	2.3				
V <sub>IL</sub>	MR Input Threshold	ASM811/812L/M/J			0.8	V	
V <sub>IH</sub>	MD law it Three held	V <sub>CC</sub> > V <sub>TH</sub> (MAX),	0.77V <sub>CC</sub>			V	
V <sub>IL</sub>	MR Input Threshold	ASM811/812R/S/T			0.25V <sub>CC</sub>	V	
	MR Pullup Resistance		10	20	30	kΩ	
aSheet4U.	com	V <sub>CC</sub> = V <sub>TH</sub> min., I <sub>SINK</sub> = 1.2mA, ASM811R/S/T			0.3		
$V_{OL}$	Low RESET Output Voltage (ASM811)	$V_{CC} = V_{TH} \text{ min., } I_{SINK} = 3.2\text{mA},$ ASM811L/M/J			0.4	V	
		$V_{CC} > 1.1V$ , $I_{SINK} = 50\mu A$			0.3		
V	High RESET Output Voltage	V <sub>CC</sub> > V <sub>TH</sub> max., I <sub>SOURCE</sub> = 500μA, ASM811R/S/T	0.8V <sub>CC</sub>			V	
V <sub>OH</sub>	(ASM811)	V <sub>CC</sub> > V <sub>TH</sub> max., I <sub>SOURCE</sub> = 800μA, ASM811L/M/J	V <sub>CC</sub> - 1.5			V	
V <sub>OL</sub>	Low RESET Output Voltage (ASM812)	V <sub>CC</sub> = V <sub>TH</sub> max., I <sub>SINK</sub> = 1.2mA, ASM812R/S/T			0.3	V	
		V <sub>CC</sub> = V <sub>TH</sub> max., I <sub>SINK</sub> = 3.2mA, ASM812L/M/J			0.4		
V <sub>OH</sub>	High RESET Output Voltage (ASM812)	1.8V < V <sub>CC</sub> < V <sub>TH</sub> min., I <sub>SOURCE</sub> = 150μA	0.8V <sub>CC</sub>			V	
T <sub>RST</sub>	Active Reset Timeout Period	V <sub>CC</sub> > V <sub>TH</sub>	140	240		msec	
T <sub>MRST</sub>	Manual Active Reset Time- out Period	MR returns HIGH		180		msec	

### Notes:

 $<sup>1. \</sup>underline{Production\ testing\ done\ at\ TA} = 25^{\circ}C.\ Over-temperature\ specifications\ guaranteed\ by\ design\ only\ using\ six\ sigma\ design\ limits.$ 

<sup>2.</sup> RESET output is active LOW for the ASM811 and RESET output is active HIGH for the ASM812.

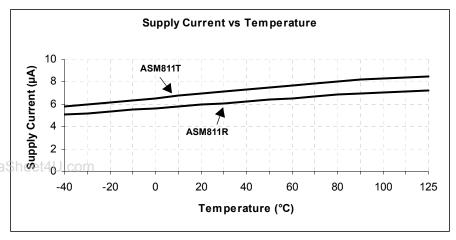
<sup>3.</sup> Glitches of 100ns or less typically will not generate a reset pulse.

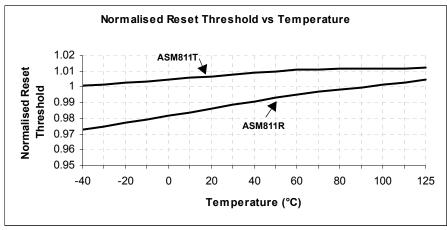


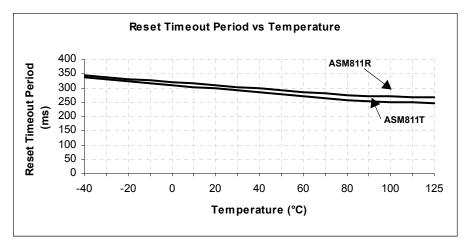
# **Typical Operating Characteristics**

Unless otherwise noted,  $V_{CC}$  is over the full voltage range,  $T_A = -40^{\circ}C$  to  $105^{\circ}C$ . Typical values at  $T_A = 25^{\circ}C$ ,

 $V_{CC}$  = 5V for L/M/J devices,  $V_{CC}$  = 3.3V for T/S devices and  $V_{CC}$  = 3V for R devices.







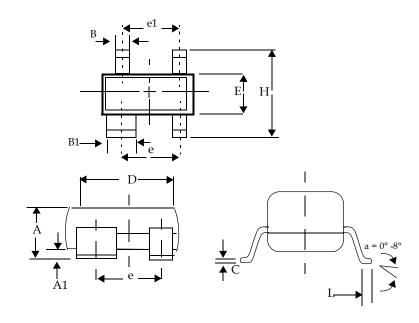


rev 1.0

# **Package Dimensions:**

# Plastic SOT-143 (4-Pin)

		Inches		Millimeters	
		Min	Max	Min	Max
	Α	0.031	0.047	0.787	1.194
	A1	0.001	0.005	0.025	0.127
www.Data	Sheet-	0.014	0.022	0.356	0.559
	B1	0.030	0.038	0.762	0.965
	C	0.0034	0.006	0.086	0.152
	D	0.105	0.120	2.667	3.048
	Е	0.047	0.055	1.194	1.397
	е	0.070	0.080	1.778	2.032
	e1	0.071	0.079	1.803	2.007
	Н	0.082	0.098	2.083	2.489
	L	0.004	0.012	0.102	0.305





# **Ordering Information:**

	Part Number <sup>1</sup>	Reset Threshold (V)	Temperature Range	Pin-Package	Package Marking (XX Lot Code)			
	ASM811 ACTIVE LOW RESET							
	ASM811LEUS-T	4.63	-40°C to +105°C	4-SOT143	SMXX			
	ASM811MEUS-T	4.38	-40°C to +105°C	4-SOT143	SNXX			
	ASM811JEUS-T	4.00	-40°C to +105°C	4-SOT143	SOXX			
	ASM811TEUS-T	3.08	-40°C to +105°C	4-SOT143	SPXX			
W	ASM811SEUS-T	2.93	-40°C to +105°C	4-SOT143	SQXX			
	ASM811REUS-T	2.63	-40°C to +105°C	4-SOT143	SRXX			
	ASM812 ACTIVE HIGH RESET							
	ASM812LEUS-T	4.63	-40°C to +105°C	4-SOT143	SSXX			
	ASM812MEUS-T	4.38	-40°C to +105°C	4-SOT143	STXX			
	ASM812JEUS-T	4.00	-40°C to +105°C	4-SOT143	SUXX			
	ASM812TEUS-T	3.08	-40°C to +105°C	4-SOT143	SVXX			
	ASM812SEUS-T	2.93	-40°C to +105°C	4-SOT143	SWXX			
	ASM812REUS-T	2.63	-40°C to +105°C	4-SOT143	SXXX			

### Notes:

# **Related Products:**

	ASM809	ASM810	ASM811	ASM812
Max Supply Current	15μΑ	15μΑ	15μΑ	15μΑ
Package Pins	3	3	4	4
Manual RESET input				
Package Type	SOT - 23	SOT - 23	SOT - 143	SOT - 143
Active-HIGH RESET Output				
Active-LOW RESET Output				

<sup>1.</sup> Tape and Reel packaging is indicated by the -T designation.



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