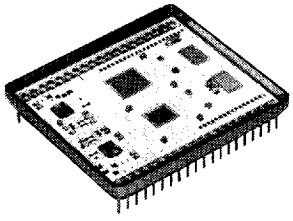
MIL-STD-1553 ADVANCED INTEGRATED MUX (AIM) HYBRID



SEE ALSO USER'S GUIDE

DESCRIPTION

DDC's BUS-61553 Advanced Integrated Mux (AIM) Hybrid is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT) device. Packaged in a single 78 pin DIP package, the BUS-61553 contains dual low-power transceivers, complete BC/RTU/MT protocol logic, a MIL-STD-1553-to-host interface unit and an 8K x 16 RAM.

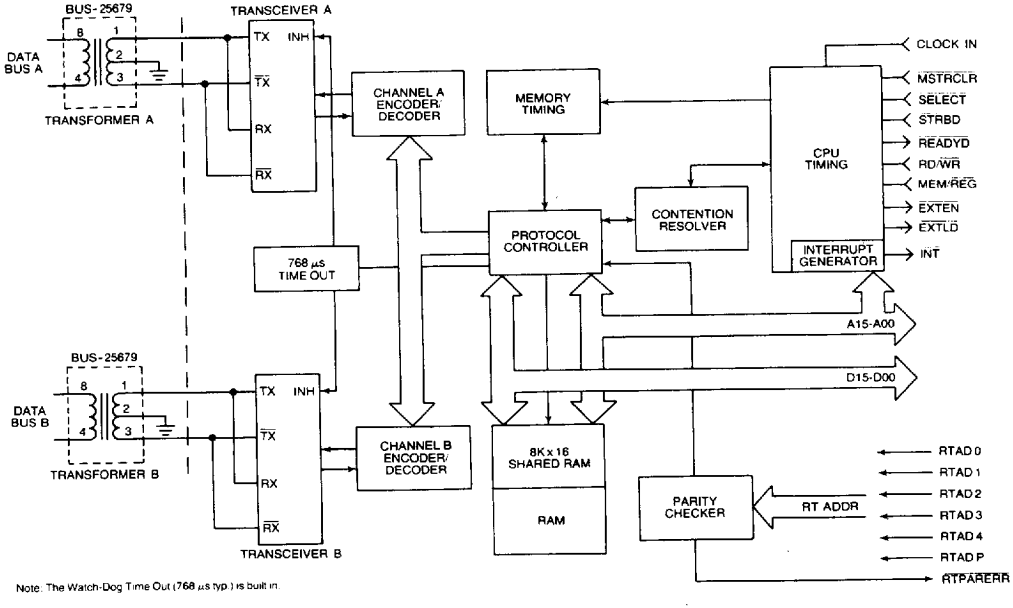
Using an industry standard dual transceiver and standard status and control signals, the BUS-61553 simplifies system integration at both the MIL-STD-1553 and host processor interface levels.

All 1553 operations are controlled through the CPU access to the shared 8K x 16 RAM. To ensure maximum design flexibility, memory control lines are provided for attaching external RAM to the BUS-61553 Address and Data Buses and for disabling internal memory; the total combined memory space can be expanded to 64K x 16. All 1553 transfers are entirely memory-mapped; thus the CPU interface requires minimal hardware and/or software support.

The BUS-61553 operates over the full military −55°C to +125°C temperature range. Available screened to MIL-STD-883, the BUS-61553 is ideal for demanding military and industrial microprocessor to 1553 interface applications.

FEATURES

- ***Fully Intergrated Terminal Including:***
  - ***Dual Transceiver***
  - ***BC/RT/MT Protocol***
  - ***Memory Management Unit***
  - ***Processor Interface Logic***
  - ***8K x 16 RAM***
- ***SOS And Bipolar Technologies***
- ***Options For Radiation Hardness***
- ***Space Qualified***
- ***High Reliability***
- ***Available With Screening To Class "S" of MIL-STD-883***



Note: The Watch-Dog Time Out (768 µs typ.) is built in.

FIGURE 1. BUS-61553 BLOCK DIAGRAM

TABLE 6. BUS-61553 PIN FUNCTIONS (78 PIN DIP)

PIN	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (μA)	I_{OL} (mA)	FUNCTION
1	D00	(5)	−0.4	−400	3.6	Data Bus Bit 0 (LSB).
2	D02	(5)	−0.4	−400	3.6	Data Bus Bit 2.
3	D04	(5)	−0.4	−400	3.6	Data Bus Bit 4.
4	D06	(5)	−0.4	−400	3.6	Data Bus Bit 6.
5	D08	(5)	−0.4	−400	3.6	Data Bus Bit 8.
6	D10	(5)	−0.4	−400	3.6	Data Bus Bit 10.
7	D12	(5)	−0.4	−400	3.6	Data Bus Bit 12.
8	D14	(5)	−0.4	−400	3.6	Data Bus Bit 14.
9	RTAD1	(5)	−0.4	•	•	Remote Terminal Address Bit 1.
10	RTAD0	(5)	−0.4	•	•	Remote Terminal Address Bit 0 (LSB).
11	RTAD4	(5)	−0.4	•	•	Remote Terminal Address Bit 4 (MSB).
12	$\overline{\text{ILLCMD}}$	+10	±0.01	•	•	Legal Command. Defines the received command as illegal.
13	SA/MC-0	•	•	−400	2.0	Subaddress/Mode Command Bit 0. Multiplexed output bit-0 of subaddress/word count field of the current command word. SA/MC determined by the state of LMC.
14	LOGIC +5V	•	•	•	•	+5V supply input for digital logic section. B6 counter.
15	SA/MC-1	•	•	−400	2.0	Subaddress/Mode Command Bit 1. In MT mode, pulses every time 32 words have been stored. B7 counter.
16	$\overline{\text{BCSTRCV}}$	•	•	−400	2.0	Broadcast Received. Indicates current command is a 1553 Broadcast Command.
17	LMC	•	•	−400	2.0	Latched Mode Command. Logic 1 indicates current command word is a mode code and selects MC0-MC4. Logic 0 indicates non-mode command and selects SA0-SA4.
18	−15VB	•	•	•	•	−15V input power supply connection for the B channel transceiver.
19	GNDB	•	•	•	•	Ground B. Power supply return connection for the B channel transceiver.
20	TX/RX-B	•	•	•	•	Transmit/Receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 Bus.
21	LOGIC GND	•	•	•	•	Logic Ground. Power supply return for the digital logic section.
22	A01	(5)	−0.4	−400	3.6	Address Bit 1.
23	A03	(5)	−0.4	−400	3.6	Address Bit 3.
24	A05	(5)	−0.4	−400	3.6	Address Bit 5.
25	A07	(5)	−0.4	−400	3.6	Address Bit 7.
26	A09	(5)	−0.4	−400	3.6	Address Bit 9.
27	A11	(5)	−0.4	−400	3.6	Address Bit 11.
28	A13	(5)	−0.4	−400	3.6	Address Bit 13.
29	A15	(5)	−0.4	−400	3.6	Address Bit 15 (MSB).
30	$\overline{\text{MEMOE}}$			−400	4.0	Memory Output Enable. A Logic 0 used to enable data output from memory when the 1553 or CPU reads from memory.
31	$\overline{\text{MEMENA-OUT}}$	•	•	−400	4.0	Memory Enable Out. Low level output to enable external RAM. Used with $\overline{\text{MEMOE}}$ to read data or with $\overline{\text{MEMWR}}$ to write data into external RAM.
32	CLOCK IN	±20	±0.02	•	•	Clock Input. 16 MHz TTL clock.
33	MEM/$\overline{\text{REG}}$	(6)	−0.7	•	•	Memory/Register. Input from CPU to select memory or register data transfer.
34	$\overline{\text{STRBD}}$	(6)	−0.7	•	•	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from CPU.
35	$\overline{\text{EXTEN}}$	•	•	−400	4.0	External Enable. Used to load data into external devices.
36	RD/$\overline{\text{WR}}$	(6)	−0.7	•	•	Read/Write. Input from the CPU which defines the Data Bus transfer as a read or write operation.
37	$\overline{\text{EXTLD}}$	•	•	−400	4.0	External load. Used tc load data into external devices.
38	GNDA	•	•	•	•	Ground A. Power supply return connection for the A channel transceiver.
39	−15VA	•	•	•	•	−15V input power supply connection for the A channel transceiver.
40	TX/RX-A	•	•	•	•	Transmit/Receive transceiver-A. Input/output to the coupling transformer that connects to the A channel of the 1553 Bus.

TABLE 6. BUS-61553 PIN FUNCTIONS (78 PIN DIP) (Continued)

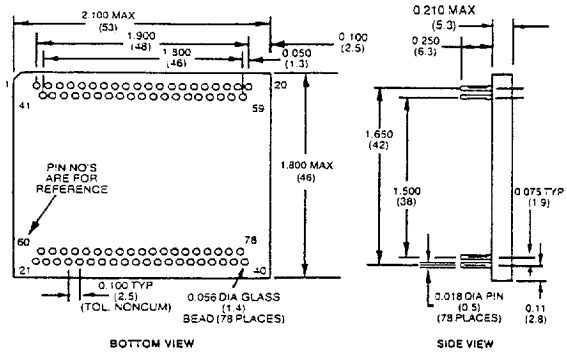
PIN	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (μA)	I_{OL} (mA)	FUNCTION
41	D01	(5)	−0.4	−400	3.6	I/O Data Bus Bit 1.
42	D03	(5)	−0.4	−400	3.6	Data Bus Bit 3.
43	D05	(5)	−0.4	−400	3.6	Data Bus Bit 5.
44	D07	(5)	−0.4	−400	3.6	Data Bus Bit 7.
45	D09	(5)	−0.4	−400	3.6	Data Bus Bit 9.
46	D11	(5)	−0.4	−400	3.6	Data Bus Bit 11.
47	D13	(5)	−0.4	−400	3.6	Data Bus Bit 13.
48	D15	(5)	−0.4	−400	3.6	Data Bus Bit 15 (MSB).
49	RTAD3	(5)	−0.4	•	•	Remote Terminal Address Bit 3.
50	RTAD2	(5)	−0.4	•	•	Remote Terminal Address Bit 2.
51	RTADP	(5)	−0.4	•	•	Remote Terminal Address Parity Input.
52	SA/MC-2	•	•	−400	2.0	Subaddress/Mode Command Bit 2. B8 (MSB) counter.
53	SA/MC-4	•	•	−400	2.0	Subaddress/Mode Command Bit 4.
54	SA/MC-3	•	•	−400	2.0	Subaddress/Mode Command Bit 3.
55	$\overline{\text{THIS-RT}}$	•	•	−400	2.0	Logic 0 pulse indicates receipt of a valid command word which contains the Remote Terminal address equivalent to the RTAD0-RTAD4 inputs.
56	$\overline{\text{RTPARERR}}$	•	•	−400	2.0	RTU (address) Parity Error. Logic 0 indicates RTU address parity (odd parity: RTAD0-RTAD4, RTADP) has been violated.
57	T/$\overline{\text{R}}$	•	•	−400	2.0	Transmit/Receive 1553 data. Latched T/R bit from current command word.
58	+5VB	•	•	•	•	+5V power supply connection for the B channel transceiver.
59	$\overline{\text{TX/RX-B}}$	•	•	•	•	Transmit/Receive transceiver-B. Inverted I/O to coupling transformer that connects to channel B of the 1553 Bus.
60	A00	(5)	−0.4	−400	3.6	Address Bit 0 (LSB).
61	A02	(5)	−0.4	−400	3.6	Address Bit 2.
62	A04	(5)	−0.4	−400	3.6	Address Bit 4.
63	A06	(5)	−0.4	−400	3.6	Address Bit 6.
64	A08	(5)	−0.4	−400	3.6	Address Bit 8.
65	A10	(5)	−0.4	−400	3.6	Address Bit 10.
66	A12	(5)	−0.4	−400	3.6	Address Bit 12.
67	A14	(5)	−0.4	−400	3.6	Address Bit 14.
68	$\overline{\text{MEMWR}}$	•	•	−400	4.0	Memory Write. Output pulse to write data into memory.
69	$\overline{\text{MEMENA-IN}}$	±20	±0.02	•	•	Memory Enable In. Enables internal RAM only; connect directly to $\overline{\text{MEMENA-OUT}}$.
70	$\overline{\text{INCMD}}$	•	•	−400	2.0	In Command. Indicates BC or RTU currently in message transfer sequence.
71	$\overline{\text{MSTRCLR}}$	(6)	−0.7	•	•	Master Clear. Power-on reset from CPU.
72	$\overline{\text{INT}}$	•	•	−400	4.0	Interrupt. Interrupt pulse line to CPU.
73	$\overline{\text{IOEN}}$	•	•	−400	4.0	Input/Output Enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
74	$\overline{\text{SELECT}}$	(6)	−0.7	•	•	Select. Input from the CPU. When active, selects BUS-61553 for operation.
75	$\overline{\text{READYD}}$	•	•	−400	4.0	Ready Data. When active indicates data has been received from, or is available to, the CPU.
76	$\overline{\text{TAGEN}}$	•	•	−400	4.0	Tag Enable. Enables an external time to counter for transferring the time tag word into memory.
77	+5VA	•	•	•	•	+5V input power supply connection for the channel A transceiver.
78	$\overline{\text{TX/RX-A}}$	•	•	•	•	Transmit/Receive transceiver-A. Inverted I/O to the coupling transformer that connects to Channel A of the 1553 Bus.

Notes:

1. I_{IH} is specified at: V_{cc} = 5.5V, V_{IH} = 2.7V.
2. I_{IL} is specified at: V_{cc} = 5.5V, V_{IL} = 0.4V.
3. I_{OH} is specified at: V_{cc} = 4.5V, V_{IH} = 2.4V.
4. I_{OL} is specified at: V_{cc} = 4.5V, V_{IH} = 0.4V.
5. Internal Pull-up Resistor = 30K Ohms, typ.
6. Internal Pull-up Resistor = 16K Ohms, typ.
7. PIN 13 = B6, PIN 15 = B7, and PIN 52 = B8(MSB). B6, B7, and B8 are the MSB lines of an 8 BIT Counter used in the BC and MT mode to count 32 WORD TRANSFERS to memory (16 words received off the bus) for a total of 128 DATA and Tag words (in MT mode). (See page 17 for discussion.)

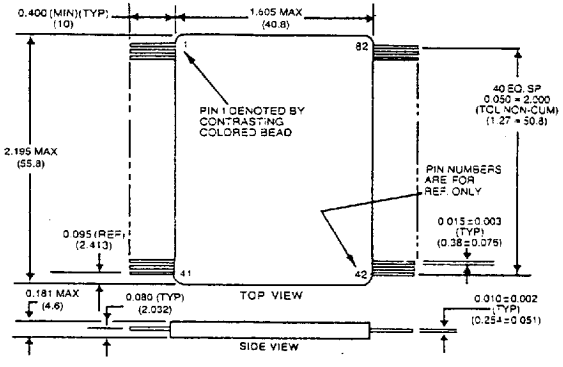
TABLE 7. BUS-61563 FLATPACK PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	NC	42	NC
2	D00	43	TX/RX-A
3	D01	44	$\overline{\text{TX/RX-A}}$
4	D02	45	−15VA
5	D03	46	+5V
6	D04	47	GNDA
7	D05	48	$\overline{\text{TAGEN}}$
8	D06	49	$\overline{\text{EXTLD}}$
9	D07	50	$\overline{\text{READYD}}$
10	D08	51	RD/$\overline{\text{WR}}$
11	D09	52	$\overline{\text{SELECT}}$
12	D10	53	$\overline{\text{EXTEN}}$
13	D11	54	$\overline{\text{IOEN}}$
14	D12	55	$\overline{\text{STRBD}}$
15	D13	56	$\overline{\text{INT}}$
16	D14	57	MEM/$\overline{\text{REG}}$
17	D15	58	$\overline{\text{MSTRCLR}}$
18	RTAD1	59	CLOCK IN
19	RTAD3	60	$\overline{\text{INCMD}}$
20	RTAD0	61	$\overline{\text{MEMENA-OUT}}$
21	RTAD2	62	$\overline{\text{MEMENA-IN}}$
22	RTAD4	63	$\overline{\text{MEMOE}}$
23	RTADP	64	$\overline{\text{MEMWR}}$
24	$\overline{\text{ILLCMD}}$	65	A15
25	SA/MC-2	66	A14
26	SA/MC-0	67	A13
27	SA/MC-4	68	A12
28	LOGIC +5V	69	A11
29	SA/MC-3	70	A10
30	SA/MC-1	71	A09
31	$\overline{\text{THIS-RT}}$	72	A08
32	$\overline{\text{BCSTRCV}}$	73	A07
33	$\overline{\text{RTPARERR}}$	74	A06
34	LMC	75	A05
35	T/$\overline{\text{R}}$	76	A04
36	−15VB	77	A03
37	+5VB	78	A02
38	$\overline{\text{GNDB}}$	79	A01
39	$\overline{\text{TX/RX-B}}$	80	A00
40	TX/RX-B	81	LOGIC GND
41	NC	82	NC



Note: Dimensions are in inches (millimeters).

FIGURE 34. MECHANICAL OUTLINE (CERAMIC DDIP)



Note: Dimensions are in inches (millimeters).

FIGURE 35. MECHANICAL OUTLINE (METAL FLATPACK)

ORDERING INFORMATION

BUS-61553-110

- **Test Criteria**
  - 0 = None
- **Screening**
  - 0 = Standard DDC Procedures
  - 1 = Full 883B Screening
  - 2 = 883B Screening without QCI testing
- **Temperature Range**
  - 1 = -55 to +125°C
  - 3 = 0 to +70°C
- **Power Supply**
  - 3 = -15 V Transceivers
  - 4 = -12 V Transceivers
  - 5 = +5 V Transceivers - Call Factory
  - 6 = Transceiverless - use with BUS-63102II - Call Factory
- **Packaging**
  - 5 = DDIP
  - 6 = Flat Pack

H-ABR