

FMP20N50ES

Super FAP-E^{3S} series

N-CHANNEL SILICON POWER MOSFET

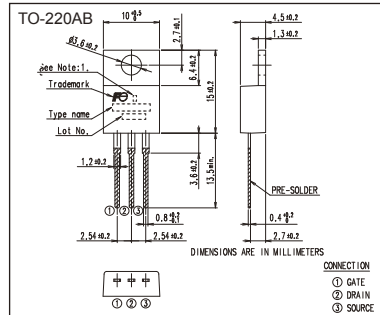
■ Features

- Maintains both low power loss and low noise
- Lower R_{DS(on)} characteristic
- More controllable switching dv/dt by gate resistance
- Smaller V_{GS} ringing waveform during switching
- Narrow band of the gate threshold voltage (4.2±0.5V)
- High avalanche durability

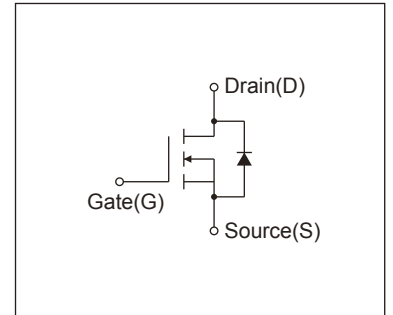
■ Applications

- Switching regulators
- UPS (Uninterruptible Power Supply)
- DC-DC converters

■ Outline Drawings [mm]



■ Equivalent circuit schematic



■ Maximum Ratings and Characteristics

● Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V _{DS}	500	V	
	V _{DSSX}	500	V	V _{GS} = -30V
Continuous Drain Current	I _D	±20	A	
Pulsed Drain Current	I _{DP}	±80	A	
Gate-Source Voltage	V _{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I _{AR}	20	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E _{AS}	582.5	mJ	Note*2
Repetitive Maximum Avalanche Energy	E _{AR}	27	mJ	Note*3
Peak Diode Recovery dv/dt	dv/dt	4.6	kV/μs	Note*4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note*5
Maximum Power Dissipation	P _D	2.02	W	T _a =25°C
		270		T _c =25°C
Operating and Storage Temperature range	T _{ch}	150	°C	
	T _{stg}	-55 to + 150	°C	

● Electrical Characteristics at T_c=25°C (unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	500	-	-	V
Gate Threshold Voltage	V _{GS} (th)	I _D =250μA, V _{DS} =V _{GS}	3.7	4.2	4.7	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =500V, V _{GS} =0V		-	25	μA
		V _{DS} =400V, V _{GS} =0V	T _{ch} =25°C	-	250	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V		10	100	nA
Drain-Source On-State Resistance	R _{DS} (on)	I _D =10A, V _{GS} =10V		0.27	0.31	Ω
Forward Transconductance	g _{fs}	I _D =10A, V _{DS} =25V	5	10	-	S
Input Capacitance	C _{iss}	V _{DS} =25V		2100	3150	pF
Output Capacitance	C _{oss}	V _{GS} =0V		250	375	
Reverse Transfer Capacitance	C _{rss}	f=1MHz		15	22.5	
Turn-On Time	td(on)	V _{cc} =300V		40	60	ns
	tr	V _{GS} =10V		38	57	
Turn-Off Time	td(off)	I _D =10A		85	127.5	
	tf	R _{GS} =15Ω		17	25.5	
Total Gate Charge	Q _G	V _{cc} =250V		57	85.5	nC
Gate-Source Charge	Q _{GS}	I _D =20A		21	31.5	
Gate-Drain Charge	Q _{GD}	V _{GS} =10V		21	31.5	
Gate-Drain Crossover Charge	Q _{SW}			10	15	
Avalanche Capability	I _{AV}	L=1.07mH, T _{ch} =25°C	20	-	-	A
Diode Forward On-Voltage	V _{SD}	I _F =20A, V _{GS} =0V, T _{ch} =25°C		0.90	1.35	V
Reverse Recovery Time	t _{rr}	I _F =20A, V _{GS} =0V		0.5	-	μs
Reverse Recovery Charge	Q _{rr}	-di/dt=100A/μs, T _{ch} =25°C		7.0	-	μC

● Thermal Characteristics

Description	Symbol	Test Conditions	min.	typ.	max.	Unit
Thermal resistance	R _{th} (ch-c)	Channel to Case			0.460	°C/W
	R _{th} (ch-a)	Channel to Ambient			62.0	°C/W

Note *1 : T_{ch}≤150°C.

Note *2 : Stating T_{ch}=25°C, I_{AS}=8A, L=16.7mH, V_{cc}=50V, R_G=50Ω.

E_{AS} limited by maximum channel temperature and avalanche current. See to 'Avalanche Energy' graph.

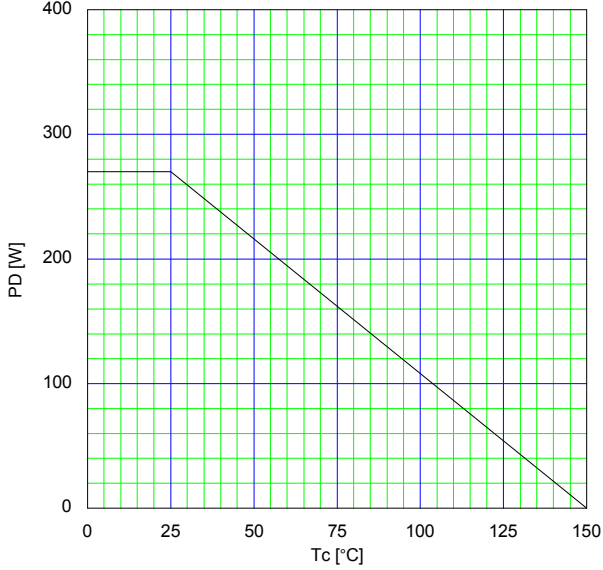
Note *3 : Repetitive rating : Pulse width limited by maximum channel temperature.

See to the 'Transient Thermal impedance' graph.

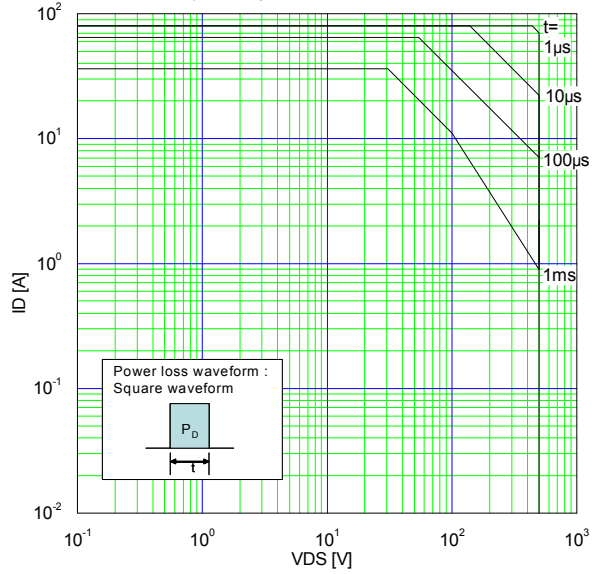
Note *4 : I_F≤I_D, -di/dt=100A/μs, V_{cc}≤BV_{DSS}, T_{ch}≤150°C.

Note *5 : I_F≤I_D, dv/dt=4.6kV/μs, V_{cc}≤BV_{DSS}, T_{ch}≤150°C.

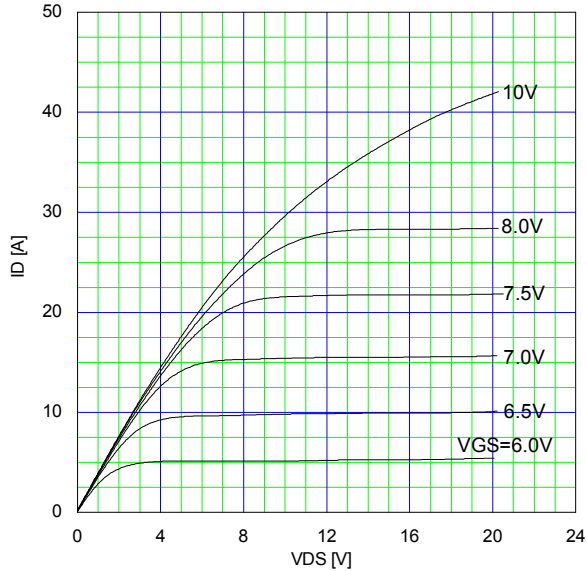
Allowable Power Dissipation
 $P_D = f(T_c)$



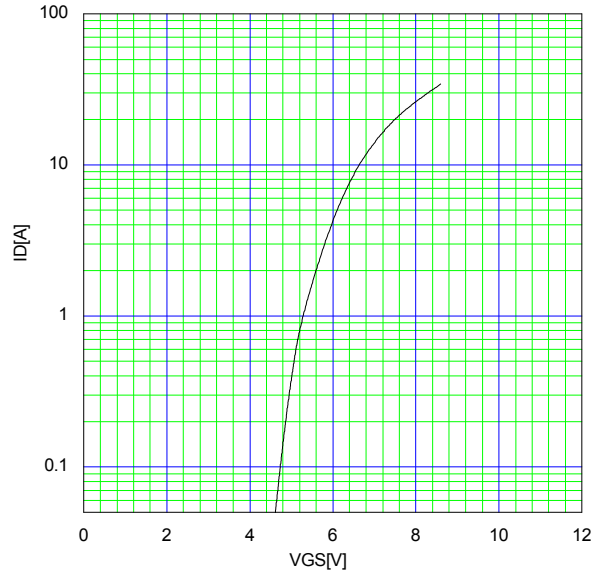
Safe Operating Area
 $I_D = f(V_{DS})$: Duty=0 (Single pulse), $T_c = 25^\circ\text{C}$



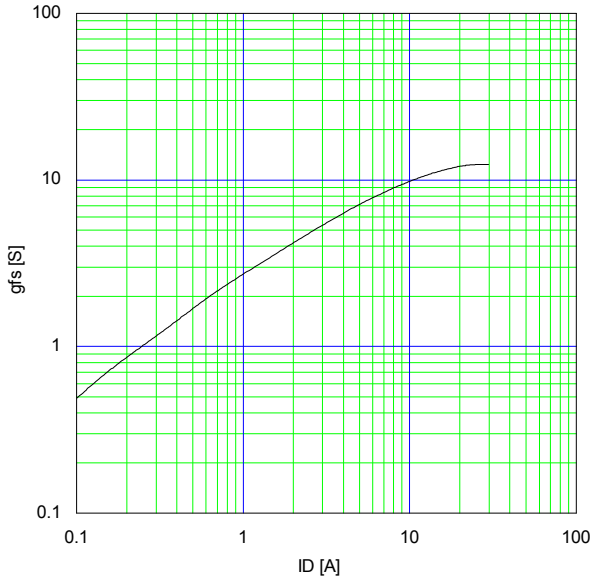
Typical Output Characteristics
 $I_D = f(V_{DS})$: 80 µs pulse test, $T_{ch} = 25^\circ\text{C}$



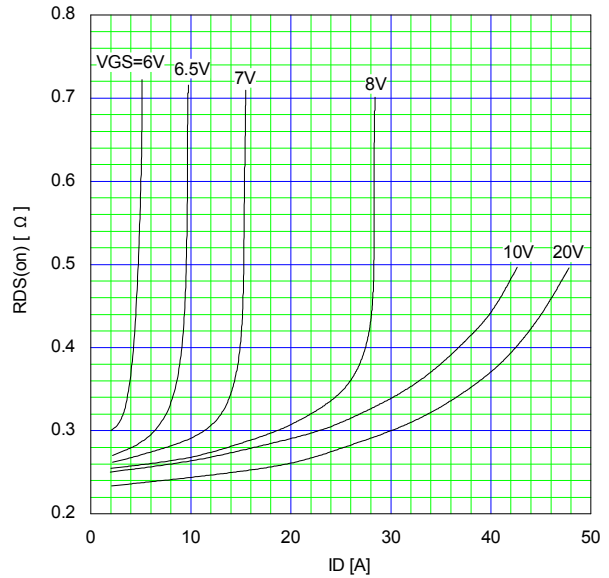
Typical Transfer Characteristic
 $I_D = f(V_{GS})$: 80 µs pulse test, $V_{DS} = 25\text{V}$, $T_{ch} = 25^\circ\text{C}$



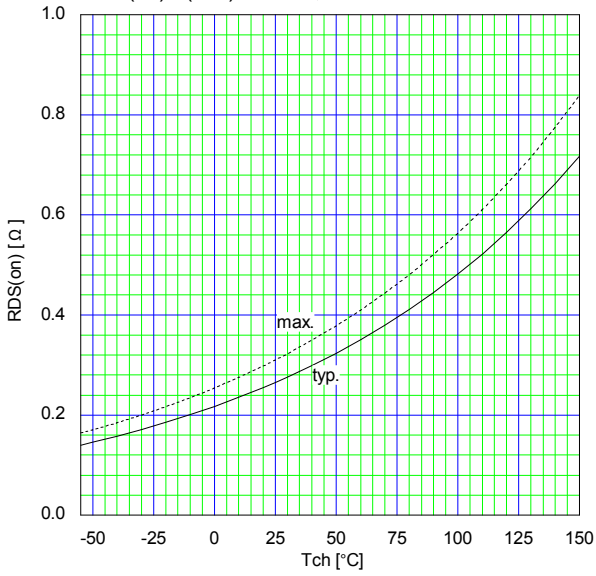
Typical Transconductance
 $g_{fs} = f(I_D)$: 80 µs pulse test, $V_{DS} = 25\text{V}$, $T_{ch} = 25^\circ\text{C}$



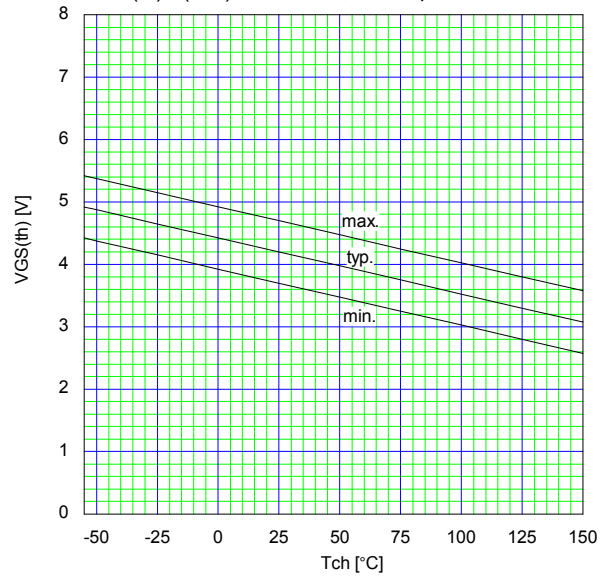
Typical Drain-Source on-state Resistance
 $R_{DS(on)} = f(I_D)$: 80 µs pulse test, $T_{ch} = 25^\circ\text{C}$



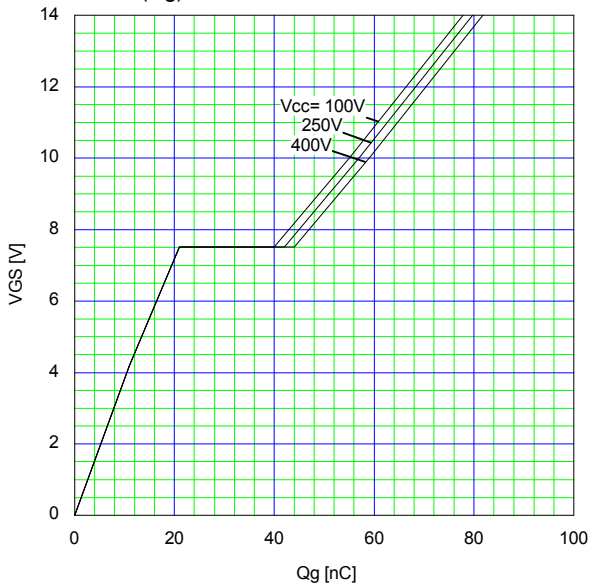
Drain-Source On-state Resistance
 $R_{DS(on)}=f(T_{ch}):I_D=10A, V_{GS}=10V$



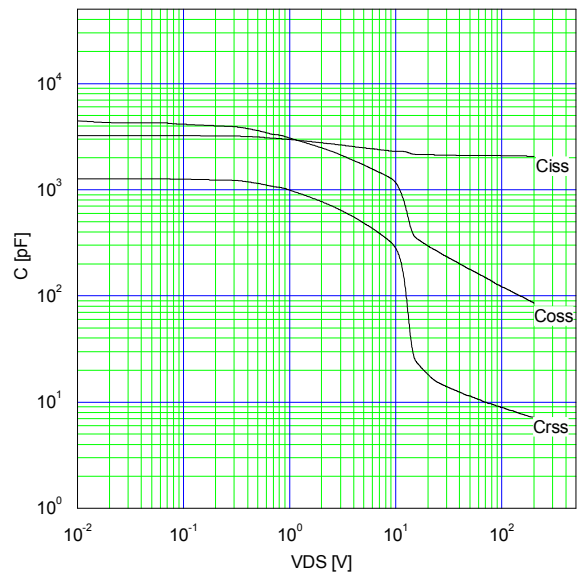
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)}=f(T_{ch}):V_{DS}=V_{GS}, I_D=250\mu A$



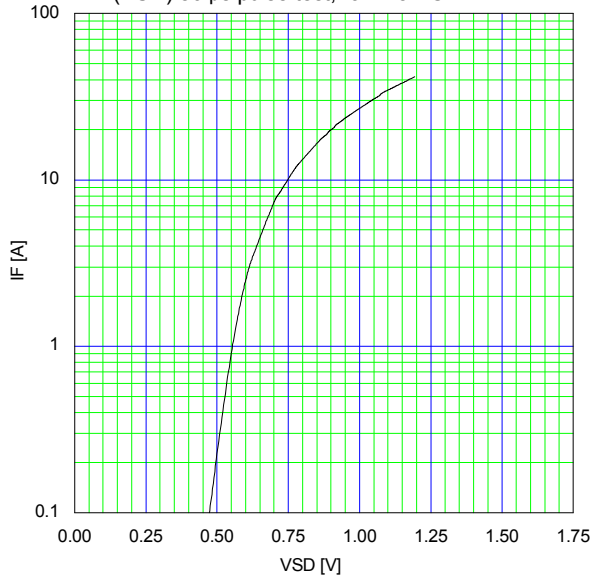
Typical Gate Charge Characteristics
 $V_{GS}=f(Q_g):I_D=20A, T_{ch}=25\text{ }^\circ\text{C}$



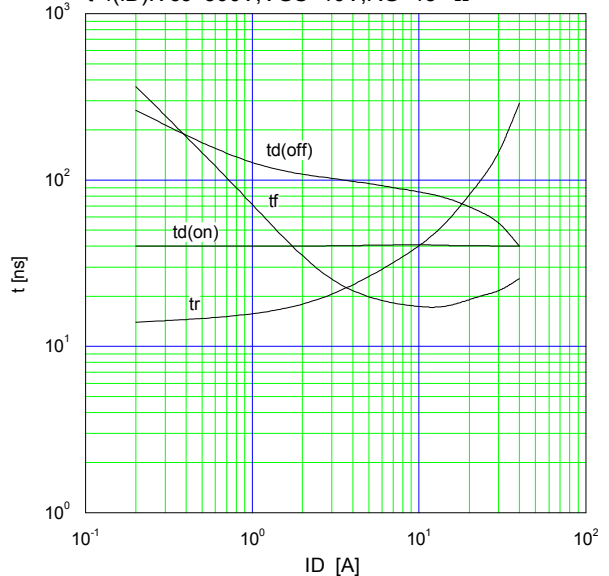
Typical Capacitance
 $C=f(V_{DS}):V_{GS}=0V, f=1\text{MHz}$

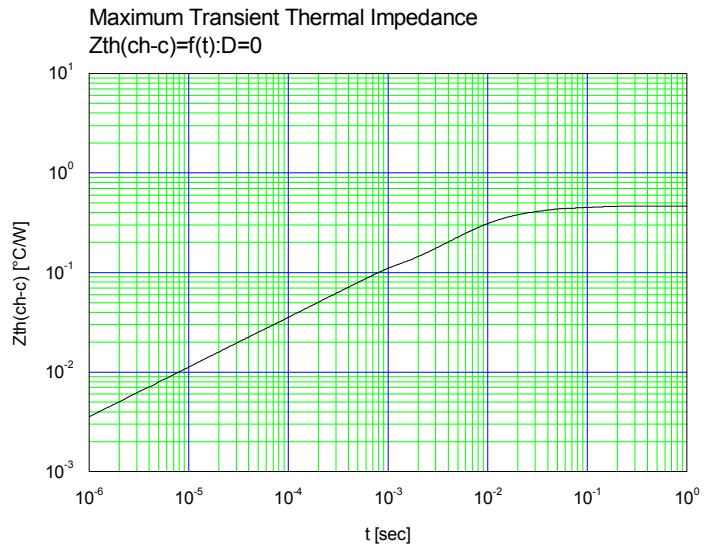
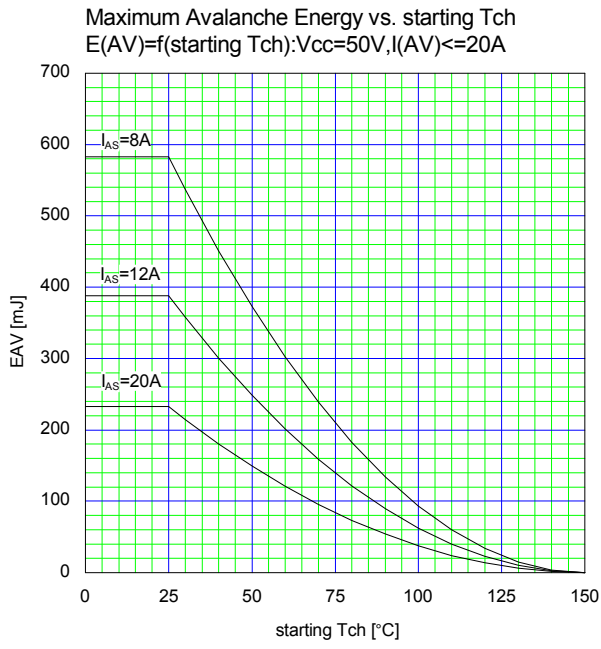


Typical Forward Characteristics of Reverse Diode
 $I_F=f(V_{SD}):80\text{ }\mu\text{s pulse test}, T_{ch}=25\text{ }^\circ\text{C}$



Typical Switching Characteristics vs. I_D
 $t=f(I_D):V_{cc}=300V, V_{GS}=10V, R_G=15\text{ }\Omega$





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