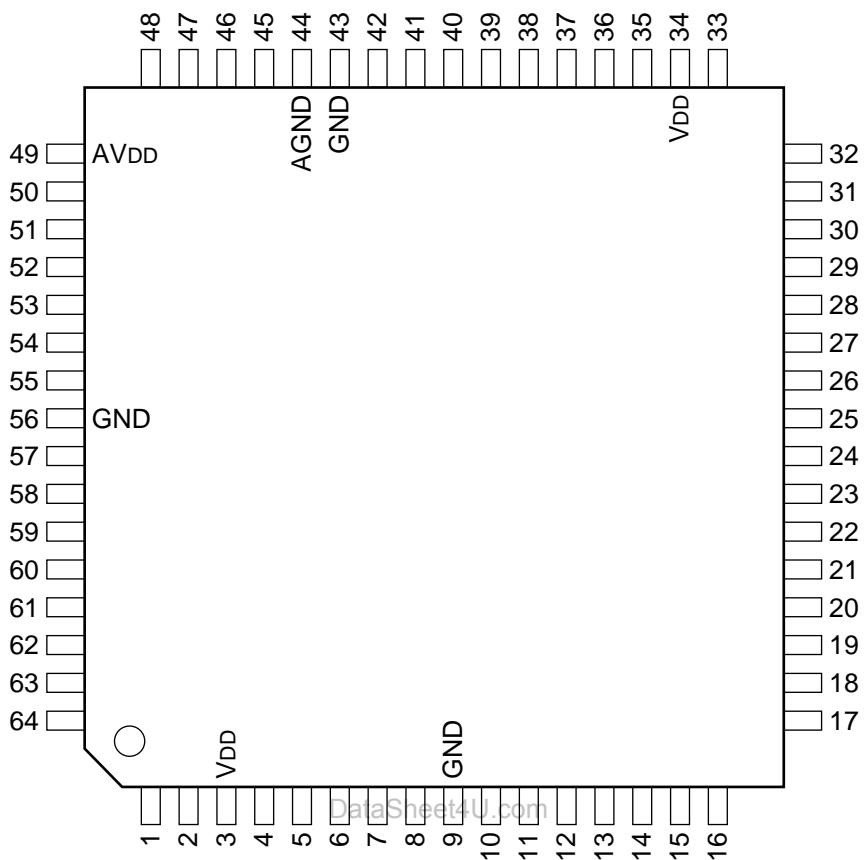


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IL00

### C-MOS MICRO COMPUTER

-TOP VIEW-



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MODE 1			MODE 2				
35	P50/TMC1	D0	10	45	P60/AN0	D0	10
36	P51/FT11	D1	11	46	P61/AN1	D1	11
37	P52/FT12/TMRI	D2	12	47	P62/AN2	D2	12
38	P53/TM0	D3	13	48	P63/AN3	D3	13
39	P54/FTOB1/FTCI1	D4	14			D4	14
40	P55/FTOB2/FTCI2	D5	15	50	P70/TXD2	D5	15
41	P56/FTOA1	D6	16	51	P71/RXD2	D6	16
42	P57/FIOA2/∅	D7	17	52	P72/SCK2	D7	17
				53	P73/TXD1		
		A0	18	54	P74/RXD1	P30/A0	18
45	P60/AN0	A1	19	55	P75/SCK1	P31/A1	19
46	P61/AN1	A2	20			P32/A2	20
47	P62/AN2	A3	21			P33/A3	21
48	P63/AN3	A4	22	59	P10/ $\overline{\text{WAIT}}$	P34/A4	22
		A5	23	60	P11/ $\overline{\text{IRQ0}}$	P35/A5	23
		A6	24	61	P12/ $\overline{\text{ADTRG/IRQ1}}$	P36/A6	24
50	P70/TXD2	A7	25	62	P13/ $\overline{\text{IRQ2}}$	P37/A7	25
51	P71/RXD2	A8	26	63	P14/ $\overline{\text{IRQ3}}$		
52	P72/SCK2	A9	27			P40/A8	26
53	P73/TXD1	A10	28	4	MD0	P41/A9	27
54	P74/RXD1	A11	29	5	MD1	P42/A10	28
55	P75/SCK1	A12	30	6	MD2	P43/A11	29
		A13	31			P44/A12/IRQ	30
		A14	32	7	RES	P45/A13/IRQ5	31
59	P10/ $\overline{\text{WAIT}}$	A15	33	8	NMI	P46/A14/IRQ6	32
60	P11/ $\overline{\text{IRQ0}}$					P47/A15/IRQ7	33
61	P12/ $\overline{\text{ADTRG/IRQ1}}$	RD	1				
62	P13/ $\overline{\text{IRQ2}}$	WR	2	57	EXTAL	P50/TMC1	35
63	P14/ $\overline{\text{IRQ3}}$			58	XTAL	P51/FT11	36
		AS	64			P52/FT12/TMRI	37
4	MD0					P53/TM0	38
5	MD1					P54/FTOB1/FTCI1	39
6	MD2					P55/FTOB2/FTCI2	40
7	RES					P56/FTOA1	41
8	NMI					P57/FIOA2/∅	42
57	EXTAL						
58	XTAL					RD	1
						WR	2
						AS	64

## MODE 3

35	P50/TMCI	D0	10
36	P51/FTI1	D1	11
37	P52/FTI2/TMRI	D2	12
38	P53/TM0	D3	13
39	P54/FTOB1/FTCI1	D4	14
40	P55/FTOB2/FTCI2	D5	15
41	P56/FTOA1	D6	16
42	P57/FIOA2/∅	D7	17
			18
		A0	18
45	P60/AN0	A1	19
46	P61/AN1	A2	20
47	P62/AN2	A3	21
48	P63/AN3	A4	22
		A5	23
		A6	24
50	P70/TXD2	A7	25
51	P71/RXD2	A8	26
52	A19	A9	27
53	P73/TXD1	A10	28
54	P74/RXD1	A11	29
55	P75/SCK1	A12	30
		A13	31
		A14	32
59	P10/WAIT	A15	33
60	P11/IRQ0		
		A16	63
4	MD0	A17	62
5	MD1	A18	61
6	MD2		
		WR	1
7	RES	RD	2
8	NMI	AS	64
57	EXTAL		
58	XTAL		

## MODE 4

35	P50/TMCI	D0	10
36	P51/FTI1	D1	11
37	P52/FTI2/TMRI	D2	12
38	P53/TM0	D3	13
39	P54/FTOB1/FTCI1	D4	14
40	P55/FTOB2/FTCI2	D5	15
41	P56/FTOA1	D6	16
42	P57/FIOA2/∅	D7	17
			18
		P30/A0	18
45	P60/AN0	P31/A1	19
46	P61/AN1	P32/A2	20
47	P62/AN2	P33/A3	21
48	P63/AN3	P34/A4	22
		P35/A5	23
		P36/A6	24
		P37/A7	25
4	MD0	P40/A8	26
5	MD1	P41/A9	27
6	MD2	P42/A10	28
		P43/A11	29
7	RES	P44/A12/IRQ4	30
		P45/A13/IRQ5	31
8	NMI	P46/A14/IRQ6	32
		P47/A15/IRQ7	33
57	EXTAL		
58	XTAL		
		P10/WAIT	59
		P11/IRQ0	60
		P12/A18/ADTRG/IRQ1	61
		P13/A17/IRQ2	62
		P14/A16/IRQ3	63
		P70/TXD2	50
		P71/RXD2	51
		P72/SCK2/A19	52
		P73/TXD1	53
		P74/RXD1	54
		P75/SCK1	55
		RD	1
		WR	2
		AS	64

## MODE 7

35	P50/TMCI	P10	59
36	P51/FT11	P11/ $\overline{\text{IRQ0}}$	60
37	P52/FT12/TMRI	P12/A18/ $\overline{\text{ADTRG}}/\overline{\text{IRQ1}}$	61
38	P53/TM0	P13/ $\overline{\text{IRQ2}}$	62
39	P54/FTOB1/FTCI1	P14/ $\overline{\text{IRQ3}}$	63
40	P55/FTOB2/FTCI2	P15	64
41	P56/FTOA1	P16	1
42	P57/FIOA2/ $\emptyset$	P17	2
			10
45	P60/AN0	P20	11
46	P61/AN1	P21	12
47	P62/AN2	P22	13
48	P63/AN3	P23	14
		P24	15
		P25	16
		P26	17
50	P70/TXD2	P27	18
51	P71/RXD2		19
52	P72/SCK2	P30	20
53	P73/TXD1	P31	21
54	P74/RXD1	P32	22
55	P75/SCK1	P33	23
		P34	24
		P35	25
4	MD0	P36	26
5	MD1	P37	27
6	MD2		28
		P40	29
8	NMI	P41	30
		P42	31
57	EXTAL	P43	32
58	XTAL	P44/ $\overline{\text{IRQ4}}$	33
		P45/ $\overline{\text{IRQ5}}$	
		P46/ $\overline{\text{IRQ6}}$	
		P47/ $\overline{\text{IRQ7}}$	
		RES	7

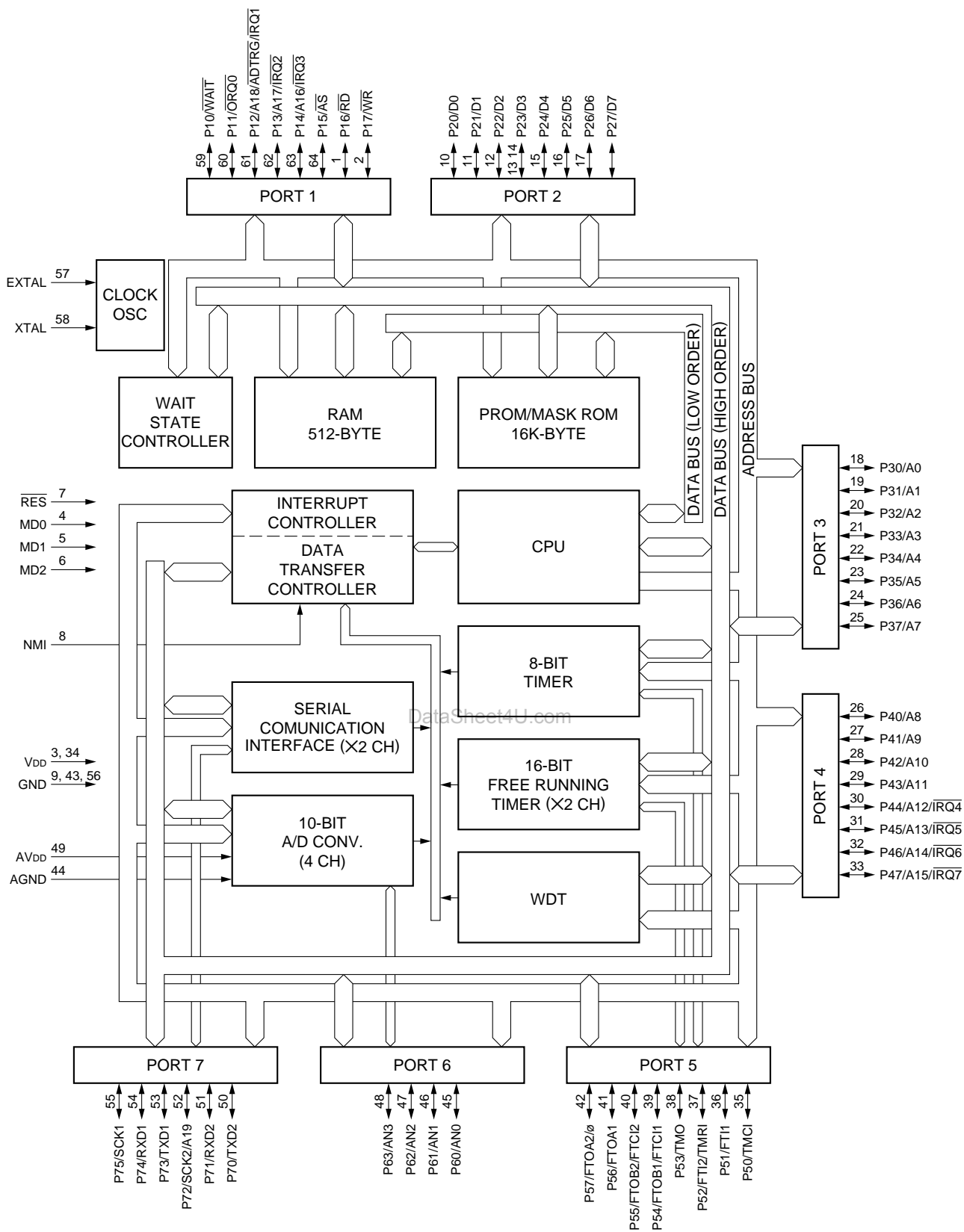
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INPUTS			OPERATION MODE	CONTENTS
MD2	MD1	MD0		
0	0	1	MODE 1	EXTENSION MINIMUM MODE (ROM INVALID)
0	1	0	MODE 2	EXTENSION MINIMUM MODE (ROM VALID)
0	1	1	MODE 3	EXTENSION MAXIMUM MODE (ROM INVALID)
1	0	0	MODE 4	EXTENSION MAXIMUM MODE (ROM VALID)
1	1	1	MODE 7	SINGLE CHIP MODE

0; LOW LEVEL

1; HIGH LEVEL



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