UNISONIC TECHNOLOGIES CO., LTD

LLV321

LINEAR INTEGRATED CIRCUIT

GENERAL PURPOSE, LOW VOLTAGE, RAIL-TO-RAIL **OUTPUT AMPLIFIERS**

DESCRIPTION

The LLV321 is a single, low cost and voltage feedback amplifier, that consumes only 80µA supply current, 1.2MHz of bandwidth and 1.5V/µs of slew rate at a low supply voltage of 2.7V. It is supplied from 2.7V (±1.35V) to 5.5V (±2.75V). The common mode voltage range extends below the negative rail and the output provides rail-to-rail performance.

The LLV321 is fabricated on a CMOS process. The combination of low power, rail-to-rail performance, low voltage operation, and tiny package options makes the device well suited for use in personal electronics equipment such as cellular handsets, pagers, PDAs, and other battery powered applications.

The LLV321 is also applied in portable test instruments, telephone systems, low cost general purpose applications, cellular phones, MP3 players, personal data assistants, A/D buffer, DSP interface, audio applications, smart card readers, keyless entry, Infrared receivers for remote controls, digital still cameras and hard disk drives.



- * Input Voltage Varies From -0.25V to +1.5V
- * Supply Current: 80µA
- * Output Voltage Varies from 0.01V to 2.69V
- * Gain Bandwidth: 1.2MHz
- * Slew Rate: 1.5V/us
- * Fully Specified at +2.7V and +5V Supplies
- * Operating Temperature Range: -40°C ~ +125°C
- * Halogen Free

ORDERING INFORMATION

Ordering Number	Package	Packing
LLV321G-AL5-R	SOT-353	Tape Reel



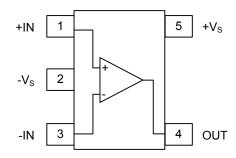
MARKING



SOT-353

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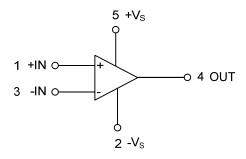
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION		
1	+IN	Positive Input		
2	-Vs	Negative Supply Voltage		
3	-IN	Negative Input		
4	OUT	Output		
5	+V _S	Positive Supply Voltage		

■ LOGIC SYMBOL



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	VI	-V _S -0.5~+V _S +0.5	V
Supply Voltages	Vs	0~+6	V
Maximum Junction Temperature	T _J	+175	°C
Storage Temperature Range	T _{STG}	-65~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Operating	Vs	2.5~5.5	V
Ambient Operating Temperature	T_OPR	-40~+125	°C

■ ELECTRICAL CHARACTERISTICS

 $(T_C = 25^{\circ}C, V_S = +2.7V, G = 2, R_L = 10k\Omega \text{ to } V_S/2, R_F = 10k\Omega, V_{O(DC)} = V_{CC}/2$; unless otherwise specified)

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
AC Performance							
Gain Bandwidth Product	GBWP	$C_L = 50 pF$, $R_L = 2k\Omega$ to $V_S/2$		1.2		MHz	
Phase Margin	Фт			52		deg	
Gain Margin	Gm			17		dB	
Slew Rate	SR	V _O = 1V _{PP}		1.5		V/µs	
Input Voltage Noise	en	>50kHz		36		nV/√Hz	
DC Performance							
Input Offset Voltage (Note 1)	Vos			1.7	7	mV	
Average Drift	TCVos			8		μV/°C	
Input Bias Current (Note 2)	I_B			<1		nA	
Input Offset Current (Note 2)	Ios			<1		nA	
Power Supply Rejection Ratio (Note 1)	PSRR	DC	50	65		dB	
Supply Current	Is			80	120	μΑ	
Input Characteristics							
Input Common Mode Voltage Range	V_{CML}	Low	0	-0.25		V	
(Note 1)	V_{CMH}	High		1.5	1.3	V	
Common Mode Rejection Ratio (Note 1)	CMRR		50	70		dB	
Output Characteristics							
Output Valtage Curing (Nate 4)	V_{OL}	$R_L = 10k\Omega$ to $V_S/2$; Low	0.1	0.01		V	
Output Voltage Swing (Note 1)	V_{OH}	$R_L = 10k\Omega$ to $V_S/2$; High		2.69	2.6	V	

Note: 1. Guaranteed by testing or statistical analysis at +25°C.

- 2. +IN and -IN are gates to CMOS transistors with typical input bias current of <1nA. CMOS leakage is too small to practically measure.
- 3. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

■ ELECTRICAL CHARACTERISTICS (Cont.)

 $(T_C = 25^{\circ}C, V_S = +5V, G = 2, R_L = 10k\Omega \text{ to } V_S/2, R_F = 10k\Omega, V_{O(DC)} = V_{CC}/2; \text{ unless otherwise specified})$

V 3/ = , 1 ₹F 1	51(22; ¥0(DC) ¥CC/2; armood 51		о оросинос,		
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GBWP	C_L = 50pF, R_L =2k Ω to V_S /2		1.4		MHz
Φ_{m}			73		deg
G _m			12		dB
SR			1.5		V/µs
en	>50kHz		33		nV/√Hz
Vos			1	7	mV
TCVos			6		μV/°C
I_{B}			<1		nA
I _{OS}			<1		nA
PSRR	DC	50	65		dB
Av		50	70		dB
Is			100	150	μΑ
V_{CML}	Low	0	-0.4		V
V_{CMH}	High		3.8	3.6	V
CMRR		50	75		dB
Vo	$R_L = 2k\Omega$ to $V_S/2$; Low/High		0.036~4.95		V
V _{OL}	$R_L = 10k\Omega$ to $V_S/2$; Low (Note 1)	0.1	0.013		>
V _{OH}	$R_L = 10k\Omega$ to $V_S/2$; High (Note 1)		4.98	4.9	٧
Io	Sourcing; V _O =0V	5	+34		mA
Io	Sinking; V _O =5V	10	-23		mA
	SYMBOL GBWP \$\Phi_m\$ Gm SR en Vos TCVos IB Ios PSRR AV Is V_CML V_CMH CMRR Vo Vol Vol Io	$ \begin{array}{c c} \text{SYMBOL} & \text{TEST CONDITIONS} \\ \hline \textbf{GBWP} & \textbf{C}_L = 50 \text{pF}, \textbf{R}_L = 2 \text{k}\Omega \text{to} \textbf{V}_S / 2 \\ \hline \textbf{\Phi}_m & \\ \hline \textbf{G}_m & \\ \hline \textbf{SR} & \\ \hline \textbf{en} & > 50 \text{kHz} \\ \hline \\ \hline \textbf{V}_{OS} & \\ \hline \textbf{TCV}_{OS} & \\ \hline \textbf{I}_B & \\ \hline \textbf{I}_{OS} & \\ \hline \textbf{PSRR} & \textbf{DC} \\ \hline \textbf{AV} & \\ \hline \textbf{I}_S & \\ \hline \\ \hline \textbf{V}_{CML} & \textbf{Low} \\ \hline \textbf{V}_{CMH} & \textbf{High} \\ \hline \textbf{CMRR} & \\ \hline \\ \hline \textbf{V}_O & \textbf{R}_L = 2 \text{k}\Omega \text{to} \textbf{V}_S / 2; \textbf{Low} / \textbf{High} \\ \hline \textbf{CMRR} & \\ \hline \\ \hline \textbf{V}_{OH} & \textbf{R}_L = 10 \text{k}\Omega \text{to} \textbf{V}_S / 2; \textbf{High} \\ \textbf{(Note 1)} & \\ \hline \textbf{V}_{OH} & \textbf{R}_L = 10 \text{k}\Omega \text{to} \textbf{V}_S / 2; \textbf{High} \\ \textbf{(Note 1)} & \\ \hline \textbf{I}_O & \textbf{Sourcing;} \textbf{V}_O = 0 \textbf{V} \\ \hline \end{array} $	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{ c c c c c c c } \hline SYMBOL & TEST CONDITIONS & MIN & TYP & MAX \\ \hline \hline & GBWP & C_L = 50pF, R_L = 2k\Omega \ to \ V_S/2 & 1.4 & \\ \hline & \Phi_m & 73 & \\ \hline & G_m & 12 & \\ \hline & SR & 1.5 & \\ \hline & en & > 50kHz & 33 & \\ \hline \hline & V_{OS} & 1 & 7 & \\ \hline & TCV_{OS} & 6 & \\ \hline & I_B & <1 & \\ \hline & I_{OS} & <1 & \\ \hline & PSRR & DC & 50 & 65 & \\ \hline & Av & 50 & 70 & \\ \hline & I_S & 100 & 150 & \\ \hline \hline & V_{CML} & Low & 0 & -0.4 & \\ \hline & V_{CMH} & High & 3.8 & 3.6 & \\ \hline & CMRR & 50 & 75 & \\ \hline & V_O & R_L = 2k\Omega \ to \ V_S/2; \ Low/High & 0.036~4.95 & \\ \hline & V_{OL} & R_L = 10k\Omega \ to \ V_S/2; \ High & 0.01 & 0.013 & \\ \hline & V_{OH} & R_L = 10k\Omega \ to \ V_S/2; \ High & 4.98 & 4.9 & \\ \hline & I_O & Sourcing; \ V_O=0V & 5 & +34 & \\ \hline \end{array} $

Note: 1. Guaranteed by testing or statistical analysis at +25°C.

- 2. +IN and -IN are gates to CMOS transistors with typical input bias current of <1nA. CMOS leakage is too small to practically measure.
- 3. Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

■ APPLICATION INFORMATION

General Description

The UTC **LLV321** is a low cost, single supply, low voltage and voltage feedback amplifier which is characterized a rail- to- rail output. It is designed to operate on a CMOS process, and is unity gain stable. Figure 1 shows the typical non-inverting circuit schematic

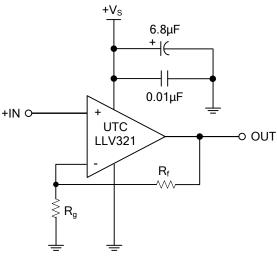


Figure 1. Typical Non-Inverting Configuration

Power Dissipation

For the UTC **LLV321**, the maximum internal power dissipation is directly depending on the maximum junction temperature. If the maximum junction temperature is higher than 150°C, some performances are declined. If the maximum junction temperature becomes higher than 175°C for an extended time, device failure may be cause.

Driving Capacitive Loads

In figure 2, a small series resistance (R_S) at the output of the amplifier, will improve stability and settling performance. Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the UTC **LLV321** requires a 450 Ω series resistor to drive a 200pF load. The response is as seen in TYPICAL CHARACTERISTIC.

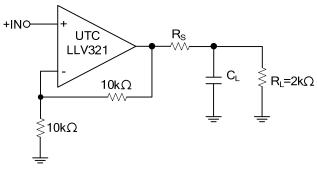
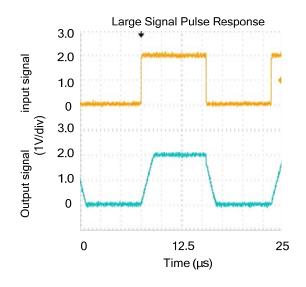
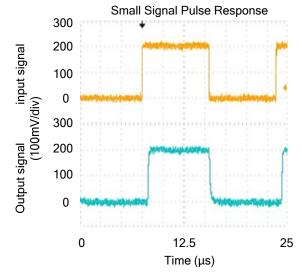
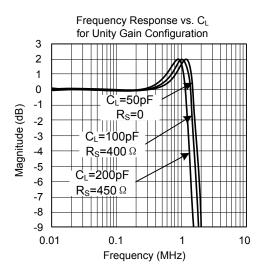


Figure 2. Typical Topology for Driving a Capacitive Load

TYPICAL CHARACTERISTIC







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