Design Issues In High Speed SPI (HSSPI) Serial EEPROM
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Introduction

The availability of higher density serial EEPROMs means they are being designed into applications that were considered far fetched just a few years ago. In many instances serial EEPROMs have replaced their byte wide counter parts as the ideal nonvolatile storage device.

The increased capacity demands the transfer of larger blocks of information. A major bottleneck is the transfer speed of the interface between the EEPROM and the controller. The new generation of SPI Serial devices from Xicor attempt to remedy the problem by increasing the date transfer rate to 5MHz.

This application note discusses the implementation of systems based on various microcontrollers which are capable of 5MHz sustained throughput on the SPI bus.

The key benefit of higher throughput and reduced transfer time is higher system reliability. During system power failures the microprocessor has a limited time to finish its current task and save all the important system parameters to the EEPROM. The improved speed can quickly transfer up to 32 bytes to the internal buffer of the EEPROM. In some cases (i.e. PowerPC processors) the above operation is transparent to the CPU, after the buffer address and transfer byte count are set prior to starting the SPI controller.

Advanced features integrated on the HSSPI serial EEPROMs include the Block Lock, which allows write control to guard against inadvertent or unauthorized write operations. This is ideal for protecting sensitive data (i.e. Kernel, Setup Parameters, Security Keys, ID numbers, Serial numbers). The Status Register is a great way to monitor performance of the device. When read, it returns information on the state of the internal write operations. By monitoring the WIP bit the software can detect an early end of write, instead of waiting the maximum specified write time after the last byte was transferred to the device.

The SPI bus has many advantages over other commonly employed serial buses. One major benefit is that most microcontrollers have hardware capability to directly interface to the SPI bus as the master. This reduces the software overhead required to operate the interface and frees up the CPU to handle other tasks at hand. Improved upload time in the HSSPI is apparent here by evaluating the result of comparison at different transfer clock rates:

Clock	Size	Upload Time
100KHz	64Kb	327.68mS
2MHz	64Kb	32.77mS
5MHz (HSSPI)	64Kb	13.11mS

PowerPC Microprocessors and DSPs

The systems that can greatly benefit from the high speed SPI are products based on the high performance microprocessors or DSPs.

The SPI port on the PowerPC processors (MPC821/23/60) is versatile. The clock rate is programmable to run at 5MHz using a 25MHz system clock. The clock control register allows modification of the clock phase and polarity to match the peripheral device. Multiple transmit and receive buffers can be initialized for automatic process by the SPI module, freeing up the main CPU. Presence of slow devices on a fast SPI bus forces the master controller to reload its baud rate generator with a new value anytime it communicates with that device. This lowers the overall system performance by increasing software overhead and time delays.
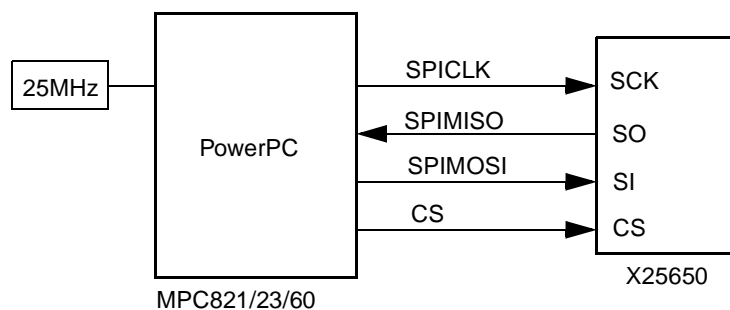
There are a few DSP products in the market with on chip, fast SPI ports. One, the Motorola DSP56002, has a Synchronous Serial Interface(SSI) port that can be configured to interface with an SPI type device. This is done by selecting the synchronous mode, gated clock-on and on-demand mode. The programmable baud rate generator allows setting the transfer rate to 5 MHz. The interface is double byte buffered and requires extensive interface software for continuous data flow.

68HC16 QSPI

The QSPI port on the M68HC16 is versatile with programmable baud rate option. Using a 16MHz system clock the clock speed can be programmed to operate at up to 4.1 MHz. The internal dual port RAM is split into three segments; Command queue, transmit and receive buffers. All the CPU has to do is to refresh the command and transmit buffers and QSPI takes care of the rest. The QSPI timing is programmable, Xicor's High Speed SPI serial devices work in either mode 0 (SCK clock idle state is LOW, Input data is latched on the leading edge of the clock and output data is changed on the following edge) or mode 1 (SCK clock idle state is HIGH, output data is changed on the leading edge of SCK and input data is latched on the following edge of SCK). The 68HC16 has four Peripheral Chip Select (PCS0:3) pins that can be controlled by bit fields in the commands byte.

General Purpose Synchronous Communications Port-MCS196, MCS251, MCS51

Most microcontrollers are equipped with UARTs which support synchronous communications mode. In the MCS251, MCS51 and MCS196 families the UART, in mode 0, configures the TXD pin to output eight clock pulses and the RXD pin to function as a bidirectional data I/O. In the MCS51 and MCS251, the maximum clock rate is 1/12 of system clock. The MCS196 clock rate can be set to 4MHz using a 16MHz system clock.

For half-duplex SPI operation the SI and SO pins of the serial memories can be tied together