AN1232
APPLICATION NOTE

RUGGEDNESS IMPROVEMENT OF RF DMOS DEVICES

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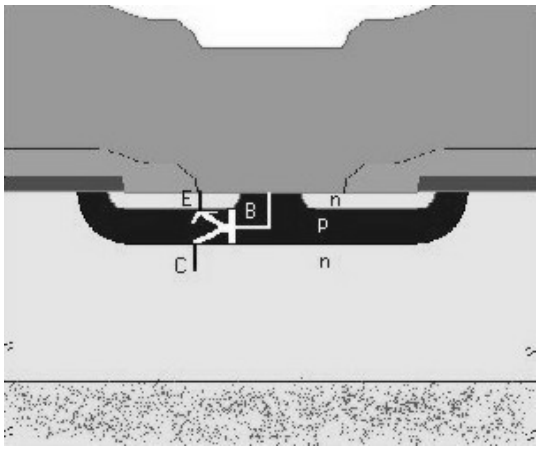
1. ABSTRACT

RF amplifiers often experience impedance mismatch between output and load. Such an impedance mismatch generates a reflected wave towards the RF power transistor, making a much more stringent working environment for the transistor. Working conditions grow critical when the load is disconnected from the output of the RF power transistor, since, in this case, the reflected wave amplitude becomes comparable to the incident one.

RF transistors are able to withstand severe impedance mismatch conditions particularly essential for applications such as plasma generators or nuclear magnetic resonators which operate under rough conditions. DMOS devices used in such applications appeared to lack the necessary ruggness when operating under severe RF load mismatch conditions. Such weakness was believed to be intrinsic.
Based on the need to improve the ruggedness of RF power DMOS, an investigation was carried out and a theoretical model simulating the failure mode mechanism was developed. Finally, relevant corrective actions were accordingly undertaken.

2. PROPOSED MODEL.

Figure 1: npn Bipolar Parasitic Transistor



Under impedance mismatch conditions the RF power transistor is subjected to a reflected wave with an amplitude that cannot be controlled and, in the worse case, with a voltage value that can exceed the BVdss of the device itself. Hence, the DMOS works as a voltage clamp for this wave. Under such conditions the device is subjected to an electric current whose amplitude is proportional to the power of the incident wave. Simultaneously, the DMOS experiences a temperature rise proportional to the

duration, voltage swing (BVdss) and amplitude of the above current. In the DMOS cross section, shown in figure 1, the presence of an npn bipolar parasitic transistor, in which the base and emitter are shorted by means of the DMOS source metallization, are clearly noticed.

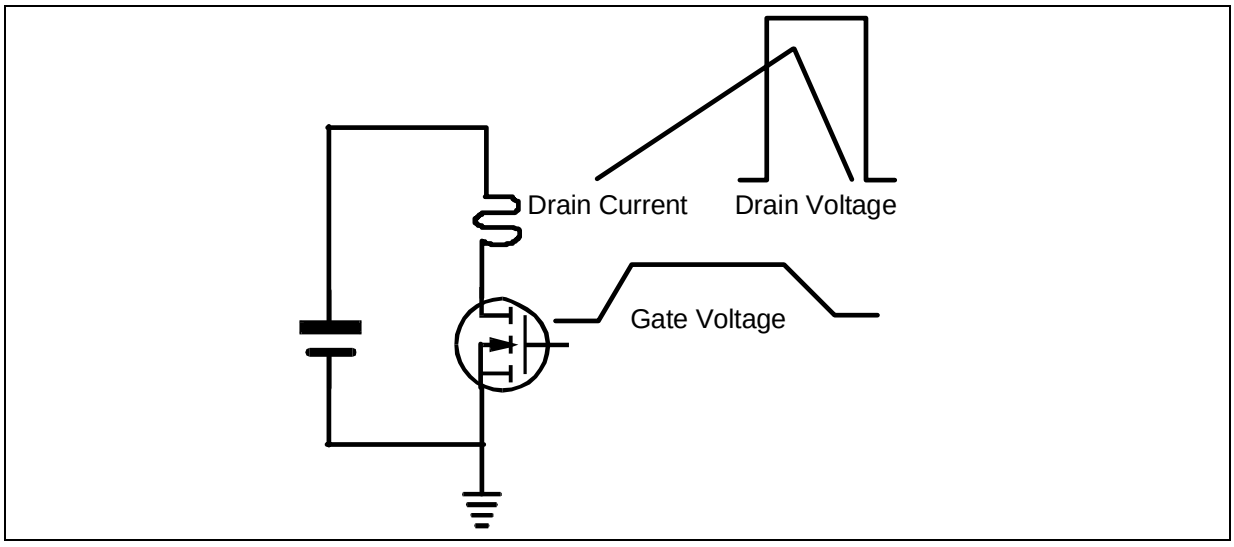
Under static conditions the parasitic transistor is inhibited by the short circuit, but under dynamic conditions, when the reverse breakdown current flows through the device, the short circuit condition itself is modified. In fact, this current crosses the base-emitter junction through the base resistance which is increased by the depletion layer due to the reverse voltage. This results in a variation in V_{be}.

We can assume that: $V_{be}=R_{be}*I_{dis}$ (*)

If I_{dis} (base distributed current) and R_{be} (base distributed resistance) are large enough, the potential on the emitter side opposed to the short circuit is sufficient to turn-on the bipolar transistor, thus concentrating the current and destroying the device.

A simplified model was developed (see figure 2) to simulate the mismatch condition on the drain of the DMOS by means of the inductance L.

Figure 2: Mismatch Condition Model



During the turn off period the device is in breakdown condition and subjected to the current induced by the inductance, thus the device dissipates power. Of course, depending on the turn off duration, we have to distinguish between the turn on of the parasitic transistor and the thermal derating, with relevant operations out of the reverse safe operating area of the DMOS. In fact, during such operations it is possible that the device exceeds the maximum allowed junction temperature (200°C). In the case of load mismatch, however, the value of the inductance is far from causing a thermal overstress. Therefore, a turn on due to R_{be} is far more likely to happen.

Another occurrence is when the voltage, due to the reflected wave, is applied on the drain of the DMOS at zero current. In this case the capacitance of the body-drain junction is involved. This capacitance will suddenly change value due to the changed potential, hence making a current whose value is given by:
$I_{dis}=C_{bd}*dV/dt$ (**)

this together with (*) gives:

$V_{be}=R_{be}*C_{bd}*dV/dt$ (***)

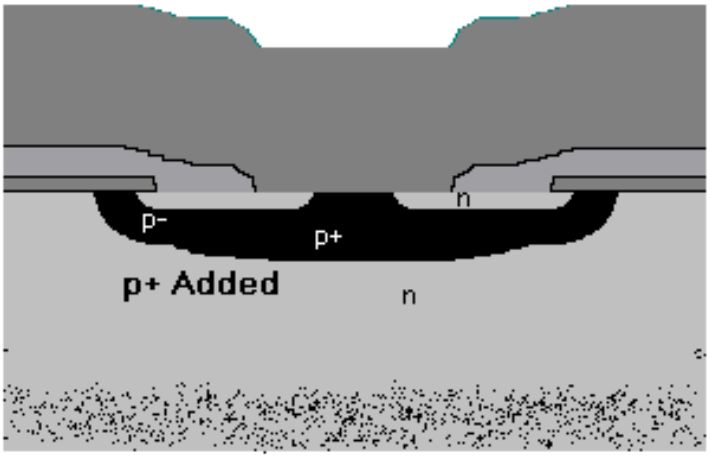
Therefore, one can see that even a zero current switching condition can cause the turn on of the parasitic transistor.

3. ACTIONS.

In order to validate the model several tests were performed. The failure current was measured during an UIS (Unclamped Inductive Switching) test. In particular the failure current density was also tested. Results are listed in table 1.

In a typical DMOS structure the body acts as the base of the parasitic transistor while the source behaves as the emitter. The Rs pinched values are typically in the KWs range. By using the existing diffusion processes it is not possible to change the body doping value in order to reduce either the DC gain (h_{fe}) or the R_{be}. This would have a dramatic impact on the DMOS threshold voltage. The only way to work on the parasitic transistor, without changing the characteristics of the DMOS, is to add a further doping level called deep-body doping. By doing so the Rs pinched is dramatically reduced to 100 ohm/square and the DC gain (hfe) of the parasitic transistor becomes close to one. This extra doping is implanted following the body doping process and prior to the body diffusion process. The Dmos structure is therefore modified as shown in figure 3.

Figure 3: Deep Body Doping



Since the deep body process is separated from the main body process (a further masking level and implant are required), typical DMOS parameters are unaffected. Optimum values for UIS and in VSWR can be obtained by using this structure and varying the deep body implant doses. Results from the test performed on the SD2921 device are listed in table 1.

Table 1.

Deep Body Dose	UIS Failure (A)	VSWR
None	10	5:1
1e15	26	15:1
2e15	39	20:1
3e15	45	30:1

4. CONCLUSION

We have demonstrated that DMOS ruggness, under varying load mismatches, is dramatically improved with a single implant process through photoresist without modifying the DMOS layout. Also, RF power performances remain unaffected. From now on, deep body doping process will be applied to all products in the production phase.

VSWR, a characteristic ruggedness parameter for RF power transistors, is linked to the standard ruggedness parameters of the DMOS. Therefore, a UIS test, easily implemented and commonly applied in EWS (Electrical Wafer Sort), can give useful information on the ruggedness of RF power devices.