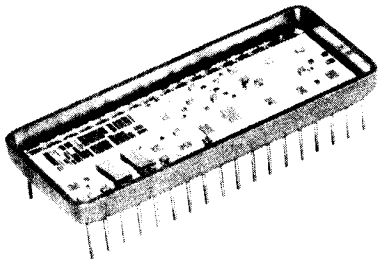
ADH-8516



12 BIT HYBRID A/D CONVERTER
2.0 μs Conversion Time; ±0.012% F.S. Range Linearity Error

A

FEATURES

- *VERY FAST HYBRID A/D WITH 3-STATE OUTPUTS*
- *CODING: Binary, Offset Binary, and Two's Complement*
- *VOLTAGE RANGES: ±2.5V, ±5V, ±10V, 0-5V, 0-10V, 0-20V*
- *BOTH SERIAL AND PARALLEL OUTPUT*
- *INTERNAL OR EXTERNAL CLOCK*
- *POWER CONSUMPTION 1.8W TYP*

DESCRIPTION

Complete in a 36 pin DIP package, the ADH-8516 is the smallest 12 bit 2.0μsec analog to digital converter available. With a suitable track and hold amplifier such as Data Device Corporation's ADH-050, it can achieve word rates of 450 kHz. Conversion time may be reduced below 2.0μsec by pin programmable short cycling if less resolution is acceptable. Gain and offset can be trimmed to zero, making the accuracy equal to the ±1/2 LSB linearity. The ADH-8516 can be pin programmed to automatically ignore a new start command until internal conversion is completed, or to start a new cycle at once and abort any conversion in process, or to cycle continuously. The internal reference voltage is externally accessible.

APPLICATIONS

Because of its high speed and 3-state outputs, the ADH-8516 is especially suited for multiplexing and for interfacing with microprocessors. Applications include high-speed data acquisition systems, autocorrelation computers, PCM communications systems, radar signal processors, moving target indicators, and electronic countermeasures systems. Utilizing the advantages of thin film and MSI technologies, the ADH-8516 has very high reliability and is ideal for remotely located and hard to access equipment where small size and high MTBF are critical.

SPECIFICATIONS

Typical values at 25°C case temperature and nominal power supply voltages

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	12	
ACCURACY AND DYNAMICS		ADH-8516-11	ADH-8516-12
Linearity Error	% F.S. Range	±0.024 Max.	±0.012 Max.
Linearity Error Tempco	ppm/°C	4 Max.	2 Max.
Gain Error (Trimmable to zero)	% F.S. Range	0.2 Typ.	0.2 Typ.
Gain Error Tempco	ppm/°C	30 Max.	20 Max.
Offset (Trimmable to zero)			
Unipolar	mV	10 Typ.	5 Typ.
Bipolar	mV	30 Typ.	10 Typ.
Offset Tempco			
Unipolar	ppm/°C	10 Typ.	5 Typ.
Bipolar	ppm/°C	25 Typ.	10 Typ.
Conversion Time	μsec	2.0 Max. for 12 bits Programmable to 1.2 Typ. for 8 bits	
Cycle Time	μsec	2.0 Typ.; 2.2 Max.	
ANALOG INPUT			
Input Ranges		Pin-Programmable	
Unipolar	V	0 to +5; 0 to +10; 0 to +20	
Bipolar	V	±2.5; ±5.0; ±10.0	
Max Voltage Without Damage	V	1.5 times F.S. input range	
Input Impedance			
0 to +5V and +2.5V Ranges	kΩ	0.625	
0 to +10V and ±5.0V Ranges	kΩ	1.25	
0 to +20V and ±10.0V Ranges	kΩ	2.5	
DIGITAL INPUT/OUTPUT (DTL/TTL COMPATIBLE)			
Digital Inputs			
Loading		1 Std. TTL load	
Start Conversion (SC)		Positive pulse; 20 nsec min., 1.5 μsec max.; Triggers on leading edge	
Clock Input (CI)		Min. period = 150 nsec; 40 – 60% duty cycle	
3-State Enable Lines		Two enable lines; MS Byte and LS Byte. Logic "0" enables output data bits	

PARAMETER	UNIT	VALUE		
DIGITAL INPUT/OUTPUT (DTL/TTL COMPATIBLE) (Cont'd)				
Short Cycle		Programs reduction in bits to obtain faster conversion		
Retrigger Input ($\overline{S}$)		Determines whether conversion can be initiated before end of cycle		
GI		Programs MSB inversion		
Digital Outputs (Buffered)				
Loading		5 Std. TTL loads, except CO = 2 Std. TTL loads		
12 Parallel Output Lines		GO, and B2 through B12; three-state		
Serial Output (SO)		Non-return to zero (NRZ)		
Clock Out (CO)		13 negative 50 nsec. typ. pulses; period = 150 nsec typ.		
Conversion Complete (CC)		Logic "0" during conversion		
B1 (MSB) and $\overline{B1}$		For pin-programmable MSB inversion		
INTERNAL REF. OUTPUT				
+ Ref Out Voltage	V	10.0 ±0.2		
+ Ref External Current Load	mA	±2 Max.		
– Ref Out Voltage	V	–4.3 Nominal		
(–Ref for Trimming Only)				
POWER REQUIREMENTS				
Supply Voltages	V	+15±3%	–15±3%	+5±5%
Max. Voltage Without Damage	V	+18	–18	+7
Current Typ.	mA	50	35	135
Max.	mA	65	65	250
TEMPERATURE RANGE (CASE)				
Operating				
–1 Option	°C	–55 to +125		
–3 Option	°C	0 to +70		
Storage	°C	–55 to +125		
PHYSICAL DATA				
Type of Package		36-Pin Double DIP		
Size	Inch	0.78 x 1.9 x .21 (1.98 x 4.83 x 0.53 cm)		
Weight	Oz.	0.64 Typ. (18g)		

TECHNICAL INFORMATION

1. INTRODUCTION

The major elements of the ADH-8516 analog to digital converter, as shown in Figure 1, are an analog voltage comparator, a 12 bit successive approximation register (SAR), and a 12 bit digital to analog converter. These elements are connected in a closed loop so as to perform A/D conversion by successive approximation. The clock and gating circuits control the SAR and the timing, as shown in the timing diagram, Figure 2.

The successive approximation process operates as follows. First bit 1 (the MSB) is set to 1, and its analog equivalent (1/2 F.S.) is produced by the D/A and compared with the input voltage V_{IN} by the comparator. If V_{IN} is greater than bit 1, the bit remains at 1 and bit 2 is tried next. If V_{IN} is less than bit 1, the bit is set to 0 before bit 2 is tried. Any succeeding bit that does not cause the combined bit weight to exceed V_{IN} remains set at 1, and any bit that causes the combined weight to exceed V_{IN} is set to 0. When the LSB has been tried, the control logic transmits a conversion complete (CC) signal. The output of the register at that time is a digital number representing the quantized analog voltage V_{IN} as a fraction of the D/A internal reference voltage.

In the ADH-8516, output digital data is gated by two enable lines so that two 8 line bytes for microprocessor interfacing can be generated. If the MS and LS Byte Enable lines are grounded, as explained below, the gates will transmit logic 1 and 0 data normally.

2. PIN FUNCTIONS

The versatility of the ADH-8516 has been maximized by making the fullest use of all 36 output pins. Figure 3 shows pin connections for normal, untrimmed, operation when 3-state output is not required.

The REF OUT, GAIN ADJ, and −REF OUT pins are used for trimming. The BIP pin connection determines whether the input accepted is unipolar (0 to +5V, 0 to +10V, or 0 to +20V) or bipolar (±2.5V, ±5V, or ±10V). Pins 10V IN and 20V IN accommodate all input ranges as shown in the connection table, Figure 3.

There are two ground pins, an ANALOG GND and a DIGITAL AND POWER GND. These grounds should be connected together at one and only one point by the user, as indicated at pin 4 in Figure 3. The ANALOG GND is represented by ⏚ , and the DIGITAL AND POWER GND is represented by ⏚ in Figure 3.

Conversions are initiated by a logic high pulse at the START pin. SHORT CYCLE and S are used to initiate special retriggerable and shorter cycle operating modes. Conversion status is indicated by the conversion complete logic signal, CC.

CO and CI are clock output and clock input, respectively. These pins are connected together when the internal clock is used. If an external clock is used, it is connected to CI. The internal clock is automatically disabled so long as CO remains disconnected.

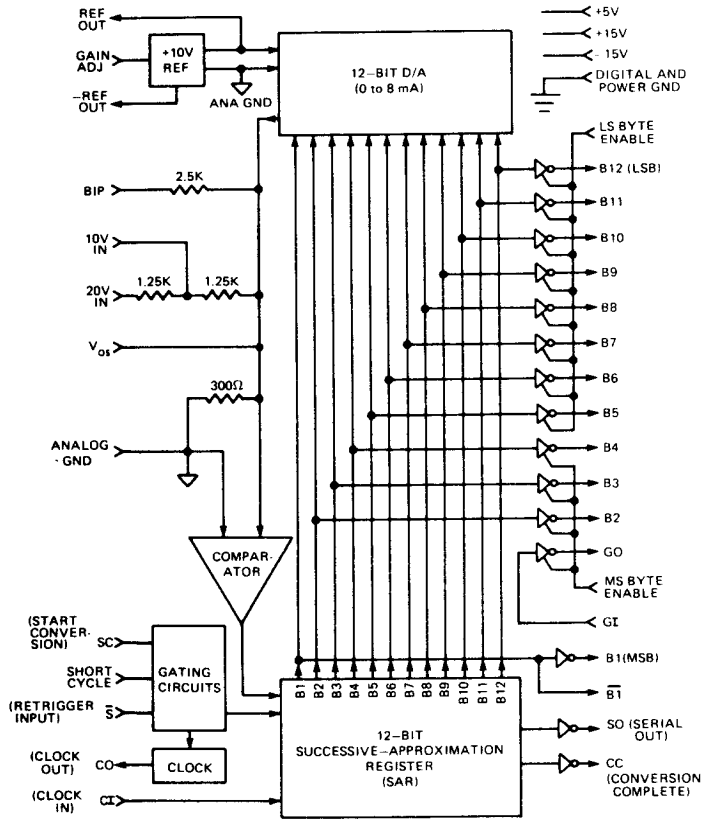


FIGURE 1. ADH-8516 BLOCK DIAGRAM

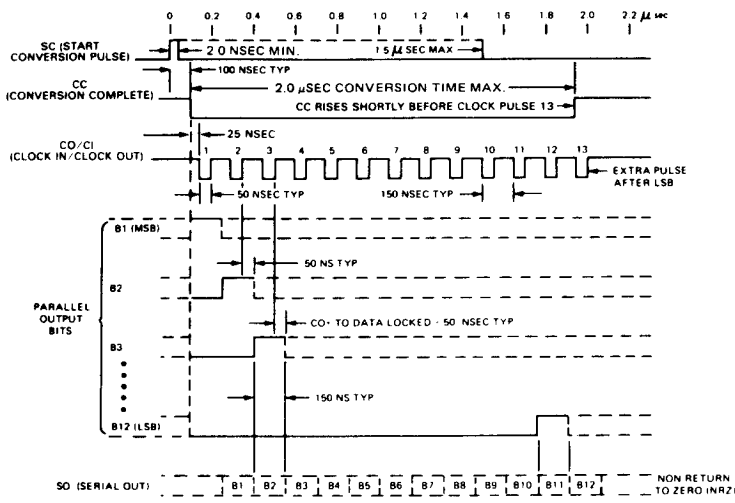


FIGURE 2. ADH-8516 TIMING DIAGRAM
Non-Retriggerable Mode; Internal Clock

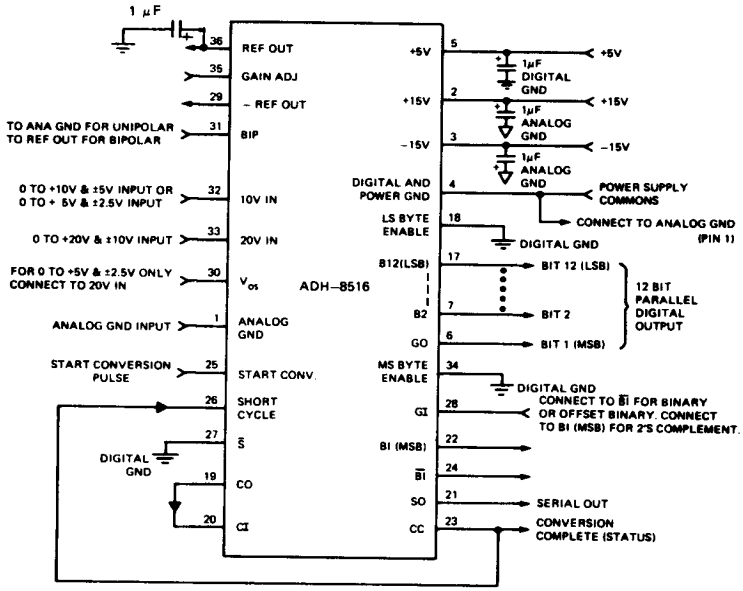


FIGURE 3. INPUT/OUTPUT CONNECTIONS FOR NORMAL OPERATION (NON-RETRIGGERABLE)

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE	INPUT TERMINAL	JUMPER CONNECTIONS (Pin Numbers are given in parentheses)
±2.5V	±3.75V	0.625kΩ	10V IN (32)	BIP (31) to REF OUT (36); 20V IN (33) to V_{OS} (30)
0 to 5V	+7.5V	0.625kΩ	10V IN (32)	BIP (31) to ANALOG GND (1); 20V IN (33) to V_{OS} (30)
±5.0V	±7.5V	1.25kΩ	10V IN (32)	BIP (31) to REF OUT (36)
0 to 10V	+15V	1.25kΩ	10V IN (32)	BIP (31) to ANALOG GND (1)
±10.0V	±15V	2.5kΩ	20V IN (33)	BIP (31) to REF OUT (36)
0 to 20V	+30V	2.5kΩ	20V IN (33)	BIP (31) to ANALOG GND (1)

FIGURE 4. INPUT VOLTAGE RANGES AND CONNECTIONS (PIN NUMBERS ARE GIVEN IN PARENTHESES)

Buffered parallel digital output is available at pin GO and pins B2, B3, . . . B11, B12 (LSB). The gate output GO is either the MSB (for binary and offset binary coding) or its complement, $\overline{MSB}$ (for 2's complement coding). The gate GI must be connected to B1 for MSB output, or to $\overline{B1}$ (MSB) for $\overline{MSB}$ output. The complement $\overline{MSB}$ is available for both bipolar and unipolar operation. Bit transitions are given in Figure 5.

Pin SO provides serial digital output. Timing for the serial output is depicted in Figure 2. The Serial Out is a non return to zero type (NRZ).

3. POWER SUPPLIES

As shown in Figure 3, the +15V, −15V, and +5V power inputs must be bypassed by capacitors of 1μF or greater. Note that the +5V input terminal is bypassed to Power and Digital Ground, while the +15V and −15V input terminals are bypassed to Analog Ground.

4. GAIN AND OFFSET TRIM ADJUSTMENTS

The gain and offset of the ADH–8516 are factory trimmed to the tolerances listed in the specifications table. Both errors can be trimmed to zero using the trim adjustment circuits shown in Figure 8.

5. 3-STATE PARALLEL DIGITAL OUTPUT

The parallel digital outputs are gated to provide two 8 line bytes for microprocessor interfacing. When the Enables for the gates in Figure 1 are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate output is high impedance (Z), and the microprocessor sees an essentially open line.

Connections for 3-state output are shown in Figure 9. The first byte is enabled by the MS Byte Enable, and transmits bits 1 to 4 only. Byte locations 4, 5, 6, 7 are connected only to high impedance outputs, and are not used. Note that bits 5 through 12 are not transmitted in byte 1 because the LS Byte Enable is at logic 1, so its gates have a high impedance output. During the second byte, only the LS Byte Enable is low, so bits 5 to 12 are transmitted and the gates for bits 1 to 4 have a high impedance output.

TRANSITION VALUE		DIGITAL BIT OUTPUTS											
UNIPOLAR	BIPOLAR	MSB											LSB
BINARY	OFFSET BINARY	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12
+F.S. – 3/2 LSB	+F.S. – 3/2 LSB	1	1	1	1	1	1	1	1	1	1	1	1
		1	1	1	1	1	1	1	1	1	1	1	0
+3/4 F.S. – 1/2 LSB	+1/2 F.S. – 1/2 LSB	1	1	0	0	0	0	0	0	0	0	0	0
		1	0	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. + 1/2 LSB	+1/2 LSB	1	0	0	0	0	0	0	0	0	0	0	1
		1	0	0	0	0	0	0	0	0	0	0	0
+1/2 F.S. – 1/2 LSB	–1/2 LSB	1	0	0	0	0	0	0	0	0	0	0	0
		0	1	1	1	1	1	1	1	1	1	1	1
+1/4 F.S. + 1/2 LSB	–1/2 F.S. + 1/2 LSB	0	1	0	0	0	0	0	0	0	0	0	1
		0	1	0	0	0	0	0	0	0	0	0	0
+3/2 LSB	–F.S. + 3/2 LSB	0	0	0	0	0	0	0	0	0	0	1	0
		0	0	0	0	0	0	0	0	0	0	0	1
+1/2 LSB	–F.S. + 1/2 LSB	0	0	0	0	0	0	0	0	0	0	0	1
		0	0	0	0	0	0	0	0	0	0	0	0

For Two's Complement coding, all values are the same as those listed above for Offset Binary coding, except that the MSB is reversed (MSB bits "0" becomes "1" and "1" becomes "0"). See Figure 6 for F.S. and 1/2 LSB values.

FIGURE 5. THEORETICAL TRANSITION VALUES

6. RETRIGGERABLE MODE

When $\overline{S}$ is grounded as in Figure 3, the ADH–8516 is considered to be in a non-retriggerable mode. A start conversion pulse at the START pin is ignored, and a new cycle cannot begin, until the CC output indicates that conversion is complete. If the START input is still high when conversion is complete, a new cycle will begin when the CC output rises (see Figure 2).

In the retriggerable mode, on the other hand, a new conversion will begin as soon as a pulse is received at the START input. If a previous conversion is in progress, it will be aborted. Programming the ADH–8516 for the retriggerable mode requires only that the $\overline{S}$ pin be connected to START instead of to digital ground.

7. CONTINUOUS CONVERSION

The ADH–8516 can be programmed to cycle continuously, beginning another conversion cycle as soon as the previous one has been completed. Continuous conversion will take place if the START input is maintained at logic 1, with pin $\overline{S}$ at digital ground.

8. SHORT CYCLING

It is possible to reduce the number of bits tested by the SAR during the successive approximation process (see Figure 1), and thereby shorten the conversion time without sacrificing linearity. The resolution will then correspond to the actual number of bits tested. The tradeoff between conversion time and accuracy is made by connecting the SHORT CYCLE pin to one of the digital outputs bits instead of to CC. 3-state outputs cannot be used because the byte enable lines must be continuously enabled by grounding them in order to detect the short cycle condition. The following table lists the SHORT CYCLE connections for several possible conversion times and accuracies:

RESOLUTION	SHORT CYCLE CONNECTION TO	CONVERSION TIME (TYP.)
11 BITS	B12	1.65 μs
10 BITS	B11	1.50 μs
9 BITS	B10	1.35 μs
8 BITS	B9	1.20 μs

DIGITAL CODING AND ACCURACY TESTS

The digital coding is described by the transition table in Figure 5. Coding is straight binary for unipolar ranges (0 – 5V, 0 – 10V, and 0 – 20V) and offset binary for bipolar ranges (±2.5V, ±5V, and ±10V). The analog input voltage levels listed in the left hand columns of Figure 5 should correspond to the transition points between the digital codes shown at the right. The voltages for Full Scale (F.S.) and 1/2 LSB for each input voltage range are listed in Figure 6.

The accuracy of the ADH-8516 is specified by its linearity error, gain, and offset. The relationships between these terms and the measured bit transitions listed in Figure 5 are discussed in the Background Information section for A/D converters in this catalog.

VOLTAGE RANGE	FULL SCALE (VOLTS)	1/2 LSB (VOLTS)
±2.5V	2.50000	0.00061
±5V	5.00000	0.00122
±10V	10.00000	0.00244
0 – 5V	5.00000	0.00061
0 – 10V	10.00000	0.00122
0 – 20V	20.00000	0.00244

FIGURE 6. FULL SCALE (F.S.) and 1/2 LSB VALUES

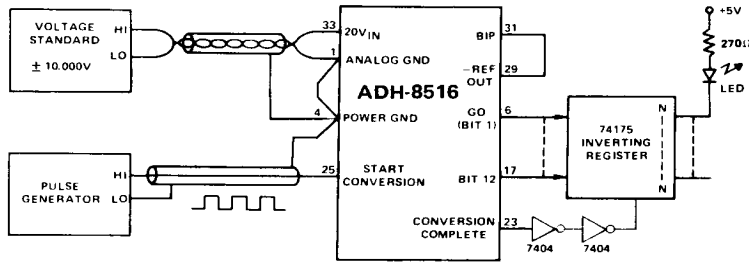


FIGURE 7. CIRCUIT FOR TESTING ACCURACY

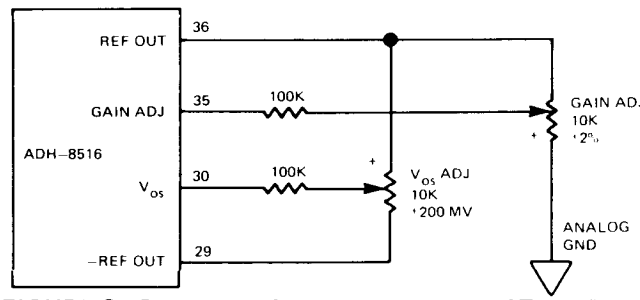


FIGURE 8. GAIN AND OFFSET TRIM ADJUSTMENTS

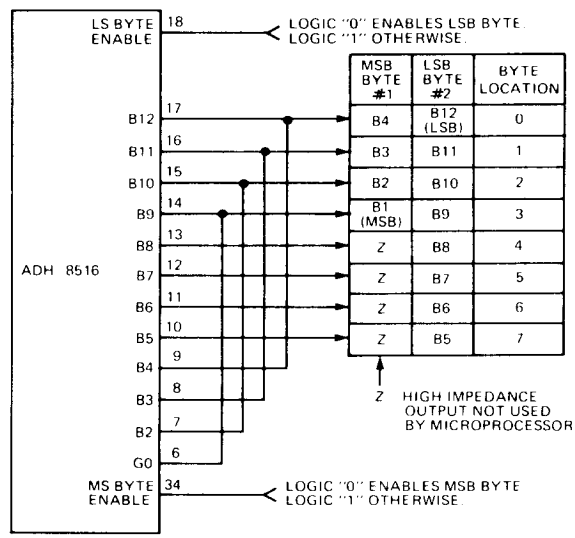


FIGURE 9. CONNECTIONS FOR COMBINING MS BYTE AND LS BYTE ON EIGHT LINES FOR INTERFACING WITH MICROPROCESSORS

A

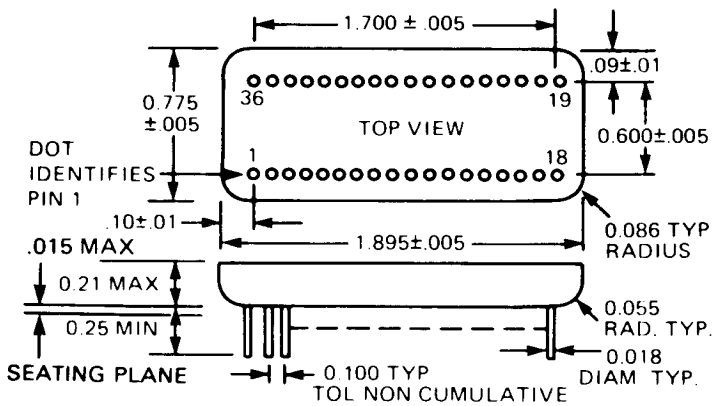
ORDERING INFORMATION

ADH–8516 –11 – 1 – 883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - —B = Screened to MIL-STD-883 but without QCI testing.
  - Blank = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.
- Operating Temperature Ranges (Case):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Linearity:
  - 11 = 11 bits (±0.024% F.S. range)
  - 12 = 12 bits (±0.012% F.S. range)

MECHANICAL OUTLINE

36 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Pin material meets solderability requirements of MIL-STD-202E, Method 208C
4. Package is Kovar with electroless nickel plating.
5. Case is grounded through pin 1 (analog ground)

The arrangement shown in Figure 7 may be used to measure the bit transitions. Offset trim, gain trim, and other standard connections are not shown. Shielded twisted pair cable is used to connect the Voltage Standard, and each of the twelve bits requires its own LED indicator. Readings should be taken with the converter energized, in thermal equilibrium at 25°, and after a warm-up time of 5 minutes. The Pulse Generator can be set at any frequency up to the maximum specified for the ADH-8516. The power supply voltages should be at their nominal values.

The suggested test procedure is as follows:

(1) Trim the offset by sweeping the input through the transition at all bits off in Figure 5 (−F.S. + 1/2 LSB for bipolar coding). Adjust the offset potentiometer until there is a 50% dither of the LSB.

(2) Trim the gain by sweeping the input through the transition at +F.S. − 3/2 LSB. Adjust the gain potentiometer for a 50% dither of the LSB.

(3) Repeat steps (1) and (2) because there might be a slight interaction between the offset and gain adjustments.

(4) Measure the input voltage levels at which other transitions occur. The differences between these voltages and the theoretical transition values will be within ±1/2 LSB.

RELIABILITY

The use of MSI and thin film resistance networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All ADH-8516's are built in accordance with requirements of MIL-STD-883.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Analog Gnd	19	CO
2	+15V	20	$\overline{CI}$
3	−15V	21	SO
4	Power and Digital Gnd	22	B1 (MSB)
5	+5V	23	CC
6	G0	24	$\overline{B1}$
7	B2	25	Start
8	B3	26	Short Cycle
9	B4	27	$\overline{S}$
10	B5	28	GI
11	B6	29	−Ref Out
12	B7	30	V_{OS}
13	B8	31	BIP
14	B9	32	10V IN
15	B10	33	20V IN
16	B11	34	MS BYTE Enable
17	B12 (LSB)	35	Gain Adj
18	LS BYTE Enable	36	Ref Out

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