Comparing the Performance of Broadcom IPSEC Boards

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IPSEC-WP100-R
08/02/02

REVISION HISTORY

Revision	*Date*	*Change description*
IPSEC-WP100-R	08/02/02	Initial release

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The BCMIPS200, BCMIPS300, and BCMIPS470 devices are Broadcom encryption acceleration boards designed for the IPSEC protocol. The boards accelerate the DES and Triple DES (3DES) bulk encryption algorithms and the SHA-1 and MD5 authentication algorithms that are used in IPSEC protocol.

The BCMIPS200 device is a small form factor 32 bit PCI card, capable of 33 MHz and 66 MHz bus operation. The BCMIPS300 device adds 64 bit, 66 MHz PCI operation, and the BCMIPS470 device improves on the performance of the BCMIPS300 device.

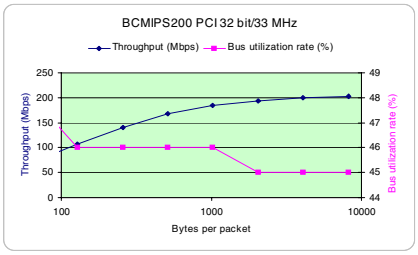
Broadcom conducted a test to compare the performance of the different BCMIPS boards on different speed and bit-width PCI busses. All of the tests used 3DES encryption and SHA1 authentication.

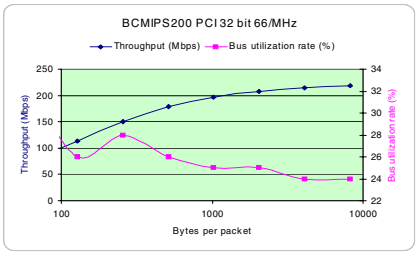
As evident from the test data, the encryption of longer packets results in higher throughput. This is because the command overhead is reduced. The control data includes a 4 byte command counter, 32 bytes of command and data pointers per packet, and 80 bytes of key and command definition data. This data crosses the bus one time to the accelerator. The payload crosses the bus two times (in and out), and the authentication operation causes 20 bytes of hash value to be written across the bus. When all of the packets have been processed, a final word is written to indicate completion.

This white paper presents the plotted and tabulated board performance test data, the plotted and tabulated comparisons of differences in board performance metrics, a description of the test methodology, and a description of the test system.

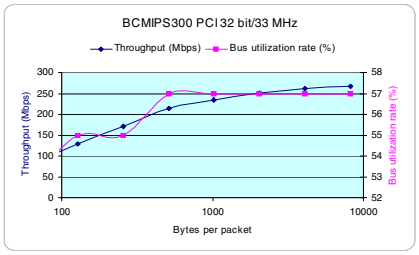
BCMIPSXXX BOARD PERFORMANCE TEST DATA

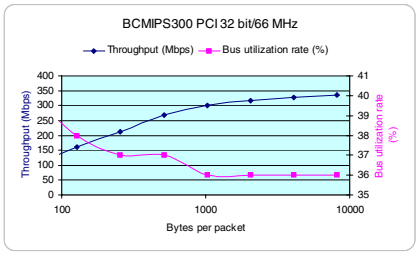
BCMIPS200 BOARDS

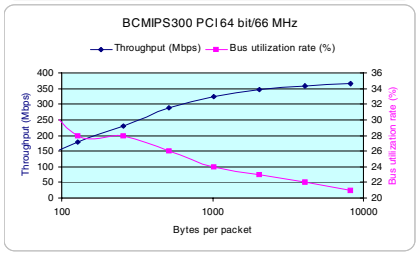




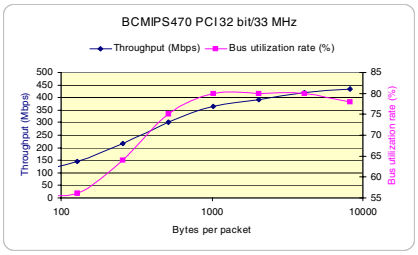
BCMIPS300 BOARDS

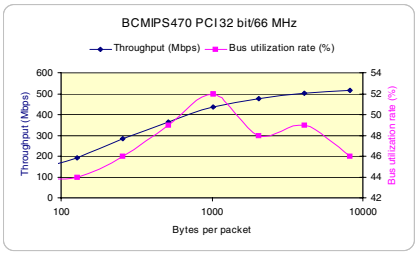


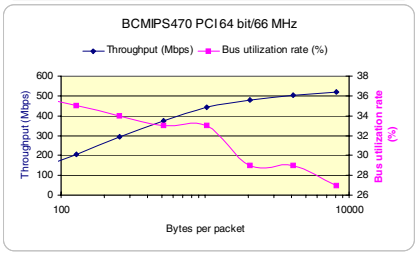




BCMIPS470 BOARDS





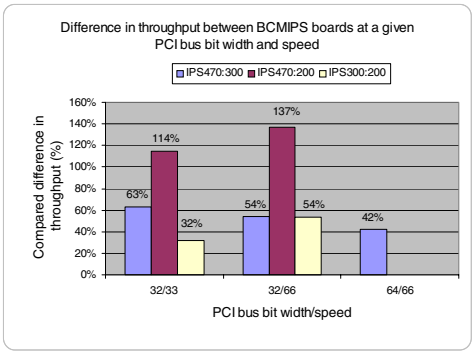


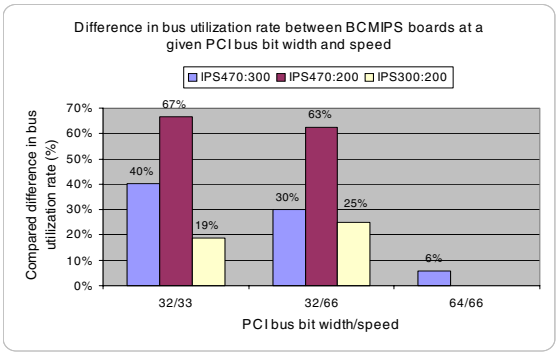
BCMIPSXXX board performance test data

IPSEC accelerator	*PCI speed (MHz)*	*PCI bus width (bits)*	*Units*	*Throughput/Bus utilization rate*							
				Number of bytes per packet							
				64	*128*	*256*	*512*	*1024*	*2046*	*4096*	*8192*
BCMIPS200	33	32	Mbps	70	106	140	168	185	193	200	203
			%	48	46	46	46	46	45	45	45
	66	32	Mbps	76	113	150	179	197	207	214	218
			%	32	26	28	26	25	25	24	24
BCMIPS300	33	32	Mbps	81	130	170	215	235	251	262	267
			%	53	55	55	57	57	57	57	57
	66	32	Mbps	103	161	211	268	301	316	328	335
			%	40	38	37	37	36	36	36	36
	66	64	Mbps	113	179	231	289	324	346	358	365
			%	34	28	28	26	24	23	22	21
BCMIPS470	33	32	Mbps	99	144	216	301	363	391	420	435
			%	56	56	64	75	80	80	80	78
	66	32	Mbps	126	193	282	363	436	476	503	516
			%	44	44	46	49	52	48	49	46
	66	64	Mbps	129	205	292	374	442	480	504	518
			%	36	35	34	33	33	29	29	27

BCMIPSXXX BOARD PERFORMANCE METRICS

The throughput and the bus utilization rate at a given bit width and speed of the PCI bus is different for each of the BCMIPS boards. The compared differences in throughput and the bus utilization rate between the BCMIPS470 board and the BCMIPS200 board, between the BCMIPS470 board and the BCMIPS300 board, and between the BCMIPS300 board and the BCMIPS200 board are illustrated and tabulated below.





32 BIT/33 MHZ PCI BUS

- 32 percent higher maximum throughput for the BCMIPS300 board compared to the BCMIPS200 board.
- 114 percent higher maximum throughput for the BCMIPS470 board compared to the BCMIPS200 board.
- 63 percent higher maximum throughput for the BCMIPS470 board compared to the BCMiPS300 board.
- 19 percent higher maximum bus utilization rate for the BCMIPS300 board compared to the BCMIPS200 board.
- 67 percent higher maximum bus utilization rate for the BCMIPS470 board compared to the BCMIPS200 board.
- 40 percent higher maximum bus utilization rate for the BCMIPS470 board compared to the BCMIPS300 board.

32 BIT/66 MHZ PCI BUS

- 54 percent higher maximum throughput for the BCMIPS300 board compared to the BCMIPS200 board.
- 137 percent higher maximum throughput for the BCMIPS470 board compared to the BCMIPS200 board.
- 54 percent higher maximum throughput for the BCMIPS470 board compared to the BCMIPS300 device.
- 25 percent higher maximum bus utilization rate for the BCMIPS300 board compared to the BCMIPS200 board.
- 63 percent higher maximum bus utilization rate for the BCMIPS470 board compared to the BCMIPS200 board.
- 30 percent higher maximum bus utilization rate for the BCMIPS470 board compared to the BCMIPS300 board.

64 BIT/66 MHZ PCI BUS

- 42 percent higher maximum throughput for the BCMIPS470 board compared to the BCMIPS300 board.
- 6 percent higher maximum bus utilization rate for the BCMIPS470 board compared to the BCMIPS300 board.

TEST METHODOLOGY

MEASURING ENCRYPTION THROUGHPUT

Broadcom measured the encryption throughput by running a series of packets through the accelerator (all with the same payload length), measuring the time between command submission and completion, and dividing the time by the number of packets. The typical number of packets is 64, though for the longer records (> 1024 bytes), the number of packets is 10.

DETERMINING PCI BUS UTILIZATION RATE

Broadcom determined the bus utilization rate by running a very long sequence of packets of the indicated size through the accelerator and using a VMetro PBT-615 bus analyzer to measure the PCI bus utilization. The bus utilization rate (expressed as a percentage) is the ratio of the amount of time that the host and the accelerator have control of the PCI bus and the total time.

TEST SYSTEM

The system used to test the BCMIPSXXX boards is based on a 1 GHz Pentium® III processor, mounted onto an Intel® server motherboard (G7ESZ) using the ServerWorks™ chipset, and 512 MB RAM. The operating system is Red Hat™ Linux™ 7.1 distribution with the Broadcom BCM582x device driver. To reduce the number of bus transactions, the stock device driver was modified to poll completion status rather than device status. This modification will be introduced into future device driver releases. Also, the driver was modified to repeat a single encryption operation 1 million times (simulating a steady-state system) for the purpose of measuring bus utilization.

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