HIGH SPEED 8 BIT A/D CONVERTER



Actual Size

DESCRIPTION AND APPLICATIONS

The DDC 5101 is a very high speed, 8 bit, successive approximation A/D converter, packaged in a 24 pin hermetic double DIP. All specifications are met with a conversion time of 900 nsec. Linearity error of 1/2 LSB and no missing codes are guaranteed over the entire operating temperature range. Functional laser trimming of a thin film resistor network results in extremely accurate and highly stable adjustment-free performance (See figure 1).

The DDC 5101 provides 9 user selectable input ranges, as well as 0° C to $+70^{\circ}$ C or -55° C to $+85^{\circ}$ C temperature ranges. The DDC 5101 is a pin for pin replacement for the MN5101 A/D Converter.

Because of its high reliability, hermetically sealed small package, and adjustment free operation over a wide temperature range, the DDC 5101 is ideally suited for the most demanding military and industrial requirements. Typical applications include systems for radar signal digitizing, high speed data acquisition and electronic countermeasures.

FEATURES

- PIN FOR PIN REPLACEMENT FOR MN5101
- HIGH SPEED CONVERSION 900 nsec Max
- 24 PIN HERMETIC DOUBLE DIP

• ±1/2 LSB LINEARITY
No Missing Codes Over Temperature

- ADJUSTMENT FREE
- AVAILABLE SCREENED IN ACCORDANCE WITH MIL-STD-883

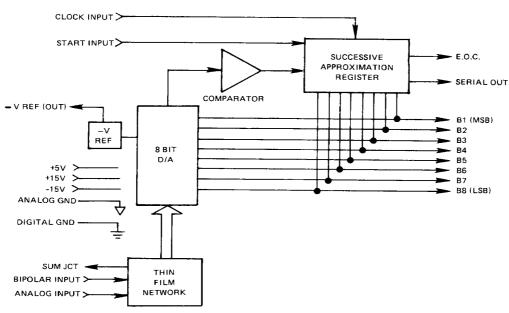


FIGURE 1. BLOCK DIAGRAM



PECIFICATIONS	UNITS		VALUE		
PARAMETER		8			
RESOLUTION	bits	MIN	TYP	MAX	
ACCURACY & DYNAMICS		Mild			
Absolute Accuracy*	LSB			±1/2	
+25° C	LSB			±1 ±2	
0 to +70° C (-3)	1.SB			±2	
-55 to +85° C (-1)	550			±1/a	
Linearity	LSB			±1/2	
0 to +70° C (-3)	1 200			900	
-55 to +85°C (-1)	ns			900	
Conversion Time (see * in Technical Information)	1				
*Absolute Accuracy includes Gain, Linearity and Drift E	rrors.				
ANALOG INPUTS	Į.		Unipolar Inputs	1	
Unipolar Ranges	V	0 to ±5	0 to ±10	0 to ± 20	
Input Voltage		1.5K	3.0K	6.0K	
Input Impedance (ohms)	Ω	1.5%	Bipolar Inputs		
Bipolar Ranges		±2.5	±5.0	±10.0	
Input Voltage	V	1.5K	3.0K	6.0K	
Input Impedance (ohms)	Ω	1.55		+25	
Maximum Input Without Damage	V	L			
DIGITAL INPUT/OUTPUT					
DIGITAL INPUT/OUTPOT					
Threshold Logic Levels Logic "1" Input	ì	2.0V		0.8V	
Logic "1" Input		l .			
Clock Input		8.8 must have drive cap	ability of 1 Std. TTL Lo	ad	
Frequency	MHz	8.8 must have drive cap	+ Conversion pulse dura	tion must be a 25 nsec mir	
Start Conversion Input	\	Positive logic, bits 1 thr	ough 8		
8 Bit Parallel Output		Non return zero (NRZ)	50 3 . 5		
Serial Data Output		Non return zero (NRZ) 5 Std. TTL Loads			
Drive Capability	ì	5 310. 112 20005			
Digital Coding	\	Complementary Binary			
Unipolar Ranges		Complementary Offset Binary			
Bipolar Ranges		Complementary		,	
POWER SUPPLY CHARACTERISTICS		+15 ± 3%	-15 ± 3%	+5 ± 5 %	
Power Supply Range	V		16 typ, 25 max	89 typ, 125 max	
	mA.	24 typ, 27 max	±0.03 typ	±0.01 typ	
Current	%F.S.R./%P.S	±0.01 typ		1 -0.0	
Power Supply Rejection	mW	1045 typ, 1405 max			
Power Consumption					
PHYSICAL CHARACTERISTICS	in	1.3 x 0.8 x 0.2 (34 x 2	1 x 5 mm)		
	in oz	1.3 × 0.8 × 0.2 (34 × 2 0.25 (7.2g)	1 x 5 mm)		

TECHNICAL INFORMATION

The DDC 5101 A/D Converter resets after a low logic signal is applied to the START pin. This signal must be at least 25nsec in duration, to insure proper reset (See figure 2). The converter remains initialized as long as the start line stays low. The conversion begins on the first low to high clock pulse after the START line goes high. Eight bits are tried in succession, MSB through LSB and serial data is available as each bit is set. Parallel data is valid 900nsec after the conversion begins.* Data is valid as long as E.O.C. is low. A new conversion may be commenced at any time during a conversion by driving the START line to logic "0".

INPUT CONFIGURATIONS

INPUT RANGE	INPUT PIN	INPUT IMPEDANCE (Ω)	PIN JUMPERS
0 to - 5V	11	1.5K	8 to 10,10 to 7, 9.
0 to -10V	11	3.0K	10 to 7, 9.
0 to -20V	12	6.0K	10 to 7, 9.
0 to + 5V	11	1.5K	8 to 7, 9, 12.
0 to +10V	11	3.0K	8 to 7, 9.
0 to +20V	12	6.0K	8 to 7, 9.
±2.5V	11	1.5K	8 to 9,12; 10 to 7.
±5.0V	11	3.0K	8 to 9; 10 to 7.
±10V	12	6.0K	8 to 9; 10 to 7.

DIGITAL OUTPUT CODING

The digital output coding for the DDC 5101 is Complementary Binary (unipolar input ranges) and Complementary Offset Binary (bipolar input ranges). The table below shows the specific code and voltage at which that code occurs for each of the nine input ranges.

ANALOG INPUT (VOLTS)							DIGITAL CODE			
	4014	0 201/			0 to +20V	±2.5V	±5.0V	±10.0V	MSB	LSB
0 to -5V		1		+9.961	+19.922	+2.500	+5.000	+10.000	0000	0000
0.000	0.000	0.000	+4.981	+9.922	+19.844	+2.481	+4.961	+ 9.922	0000	0001
-0.019	-0.039	-0.078 -9.922	+2.500	+5.000	+10.000	+0.019	+0.039	+ 0.078	0111	1111
-2.481	-4.961	-9.922 -10.000	+2.481	+4.961	+ 9.922	0.000	0.000	0.000	1000	0000
-2.500	-5.000			+0.039	+ 0.078	-2.461	4.922	- 9.844	1111	1110
l		1	0.000	0.000	0.000	-2.481	-4.961	- 9.922	1111	1111
-4.961 -4.981	-9.922 -9.961	-19.844 19.922	+0.019 0.000				1		1	

^{*900} nsec conversion time is achieved with clock input frequency of 8.8MHz. Faster conversion times are available; please contact DDC for details.

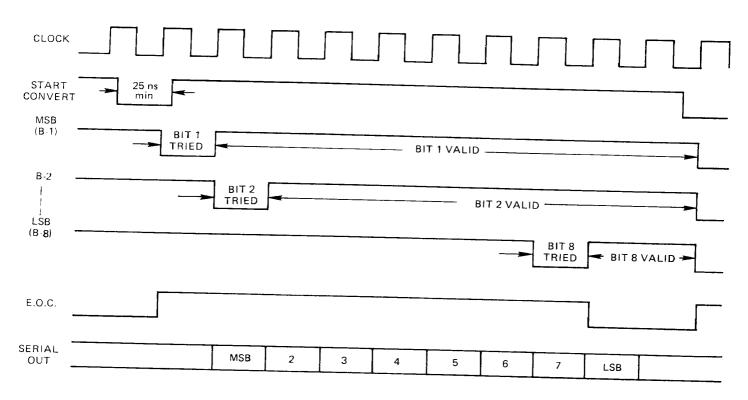
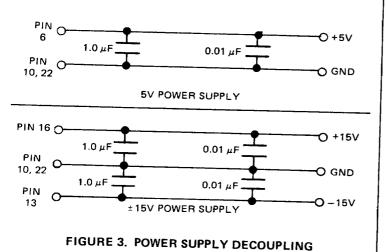


FIGURE 2. TIMING DIAGRAM

POWER SUPPLY DECOUPLING

The recommended power supply decoupling procedure is illustrated in Figure 3. The by-pass components shown in the diagram are 1.0 μF electrolytic capacitors paralleled with 0.01 μF disc ceramic capacitors.

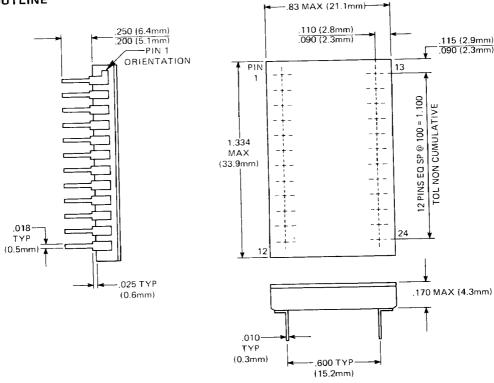


	PIN CONNECTION TABLE						
PIN	FUNCTION	PIN	FUNCTION				
1	SERIAL OUT	13	-15V				
2	B4	14	-V REF				
3	B3	15	NC				
4	B2	16	+ 15V				
5	B1 (MSB)	17	B8 (LSB)				
6	+5∨	18	В7				
7	BIPOLAR	19	! B6				
8	SUM JCT	20	B5				
9	BIPOLAR	21	E.O.C.				
10	ANALOG GND	22	DIGITAL GND				
11	INPUT	23	CLOCK				
12	INPUT	24	START				

A/D CONVERTERS



MECHANICAL OUTLINE



HYBRID PROCESSING

All of DDC's hybrid converter products are manufactured to meet military standards for high reliability. DDC hybrids are build in conjunction with the requirements of MIL-STD-883, Test Methods and Procedures for Microelectronics. The screening procedures are based on methods 5008.

