National Semiconductor

PRELIMINARY

T-75-45-05

DS26C32C Quad Differential Line Receiver

General Description

The DS26C32 is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

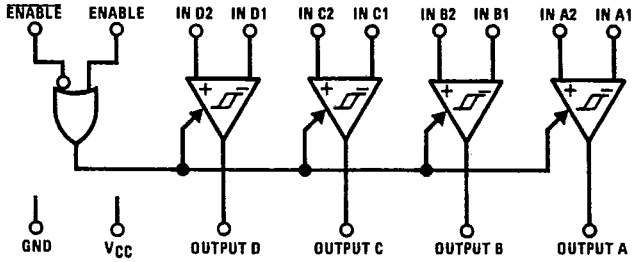
The DS26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Each receiver is also equipped with input fail-safe circuitry, which causes the output to go to a logic "1" state when the inputs are open.

The DS26C32 provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- Low power CMOS design
- ±0.2V sensitivity over the entire common mode range
- Typical propagation delays: 20 ns
- Typical input hysteresis: 50 mV
- Input fail-safe circuitry
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses

Logic Diagram



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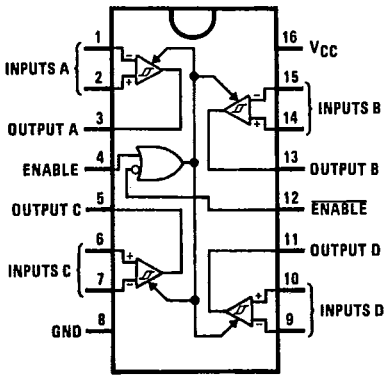
Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS26C32CJ, DS26C32CM, DS26C32CN, DS26C32MJ or DS26C32MN
See NS Package J16A, M16A or N16A

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1

Hi-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

For complete specifications see the Interface Databook.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Current Per Output	±25 mA

Operating Conditions

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	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±5% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−0.2		+0.2	V
R_{IN}	Input Resistance	$-7V < V_{CM} < +7V$ (One Input AC GND)		10		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND		−1.1		mA
		$V_{IN} = -10V$, Other Input = GND		+1.6		mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, $V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA	3.84	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, $V_{DIFF} = +1V$ I_{OUT} = 6.0 mA		0.2	0.33	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}} = V_{IH}$		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, $V_{DIFF} = +1V$		12		mA
V_{HYST}	Input Hysteresis			50		mV

AC Electrical Characteristics V_{CC} = 5V ±5% (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V		20		ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		12		ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		14		ns

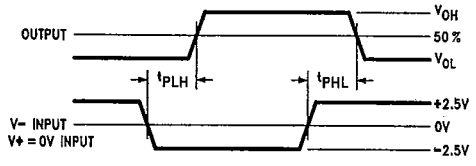
Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the −40°C to +85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Test and Switching Waveforms

Propagation Delay



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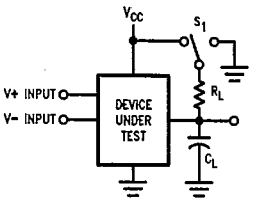
Test Circuit for TRI-STATE Output Tests



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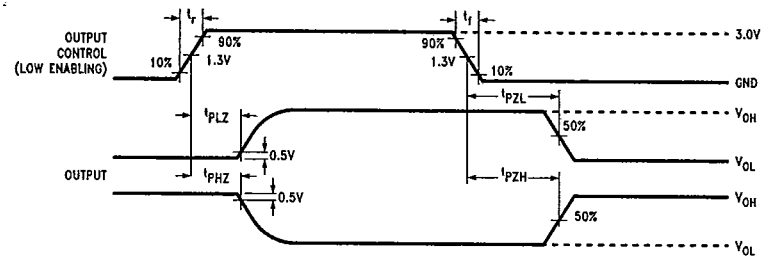
C_L includes load and test jig capacitance.
S1 = V_{CC} for t_{PZL} and t_{PLZ} measurements.
S1 = Gnd for t_{PZH} and t_{PHZ} measurements.

TRI-STATE Output Enable and Disable Waveforms



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