64-Common X 132-Segment plus 1-Icon Bit Map Type LCD Controller and Driver

■ GENERAL DESCRIPTION

The **NJU6676** is a bit map LCD driver to display graphics or characters. It contains 8,580 bits display data RAM, microprocessor interface circuits, instruction decoder, 132-segment drivers, 64-common drivers and 1-icon drivers.

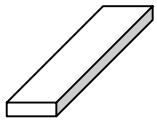
The bit image display data is transferred to the display data RAM by serial or 8-bit parallel interface.

65 x 132 dots graphics or 8-character 4-line by 16 x 16 dots character with icon are displayed by **NJU6676** itself.

The wide operating voltage from 2.2 to 5.5V and low operating current are useful for small size battery operating items.

The build-in Electrical Variable Resistance is very precision, furtheremore the rectangle outlook is very applicable to COG or Slim TCP.

■ PACKAGE

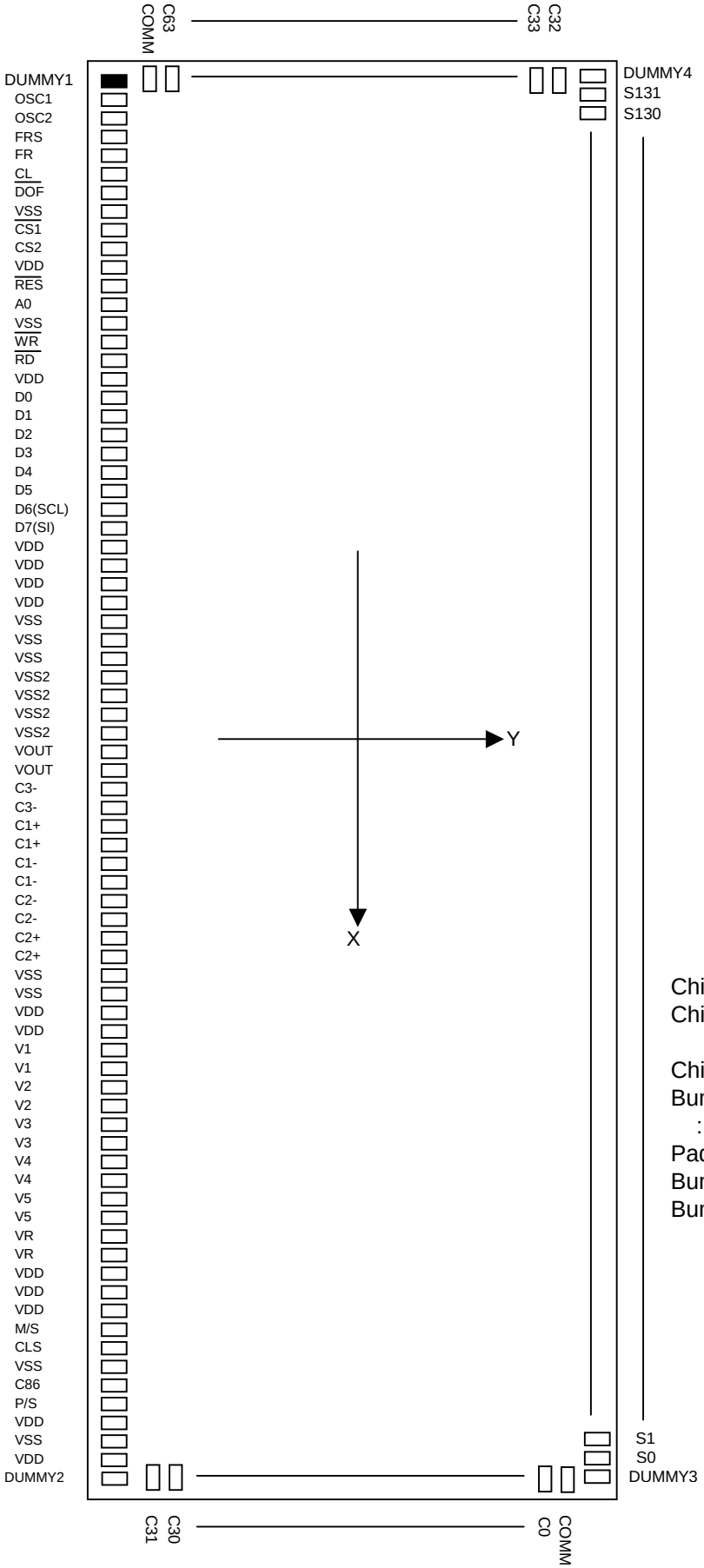


NJU6676CH

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 8,580 bits
- 197 LCD Drivers - 65-common and 132-segment
- Direct Microprocessor Interface for both of 68 and 80 type MPU
- Serial Interface
- Programmable Bias selection ; 1/7,1/9 bias
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Static indicator, Display Start Line Set, Bias Select, Inverse Display, Common Driver order Assignment, Power control set, Page Address Set, Column Address Set,Status Read, All On/Off, ADC Select, Read Modify Write, Power Saving.
- Power Supply Circuits for LCD Incorporated
  Voltage Booster Circuits (4-time Maximum), Regulator, Voltage Follower x 4
- Precision Electrical Variable Resistance (64-step)
- Low Power Consumption 80uA(Typ.).
- Operating Voltage (All the voltages are based on VDD=0V.)
  - Rogic Operating Voltage : -2.2V ~ -5.5V
  - Voltage Booster Operating Voltage : -2.5V ~
  - LCD Driving Voltage : -6.0V ~ -18.0V
- Rectangle outlook for COG
- Package Outline : Bump-chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Center : X=0um, Y=0um
Chip Size
:X=8.72mm,Y=2.37mm
Chip Thickness : 675um ± 30um
Bump Size
: 45um x 83um
Pad Pitch : 60um(Min.)
Bump Height : 15um(Typ.)
Bump Material : Au

■ PAD COORDINATES

Chip Size 8.72 x 2.37mm(Chip Center X=0um, Y=0um)

PAD No.	Terminal	X(um)	Y(um)
1	DUMMY1	-4139	-1025
2	OSC1	-3347	-1025
3	OSC2	-3287	-1025
4	FRS	-3129	-1025
5	FR	-2909	-1025
6	CL	-2688	-1025
7	DOF	-2468	-1025
8	VSS	-2311	-1025
9	CS1	-2251	-1025
10	CS2	-2191	-1025
11	VDD	-2131	-1025
12	RES	-2071	-1025
13	A0	-2011	-1025
14	VSS	-1951	-1025
15	WR	-1891	-1025
16	RD	-1831	-1025
17	VDD	-1771	-1025
18	D0	-1613	-1025
19	D1	-1393	-1025
20	D2	-1172	-1025
21	D3	-952	-1025
22	D4	-731	-1025
23	D5	-511	-1025
24	D6(SCL)	-291	-1025
25	D7(SI)	-70	-1025
26	VDD	155	-1025
27	VDD	215	-1025
28	VDD	275	-1025
29	VDD	335	-1025
30	VSS	395	-1025
31	VSS	455	-1025
32	VSS	515	-1025
33	VSS2	575	-1025
34	VSS2	635	-1025
35	VSS2	695	-1025
36	VSS2	755	-1025
37	VOUT	815	-1025
38	VOUT	875	-1025
39	$C3^-$	935	-1025
40	$C3^-$	995	-1025
41	$C1^+$	1055	-1025
42	$C1^+$	1115	-1025
43	$C1^-$	1175	-1025
44	$C1^-$	1235	-1025
45	$C2^-$	1295	-1025
46	$C2^-$	1355	-1025
47	$C2^+$	1415	-1025
48	$C2^+$	1475	-1025
49	VSS	1535	-1025
50	VSS	1595	-1025

PAD No.	Terminal	X(um)	Y(um)
51	VDD	1655	-1025
52	VDD	1715	-1025
53	V1	1775	-1025
54	V1	1835	-1025
55	V2	1895	-1025
56	V2	1955	-1025
57	V3	2015	-1025
58	V3	2075	-1025
59	V4	2135	-1025
60	V4	2195	-1025
61	V5	2255	-1025
62	V5	2315	-1025
63	VR	2375	-1025
64	VR	2435	-1025
65	VDD	2495	-1025
66	VDD	2555	-1025
67	VDD	2615	-1025
68	M/S	2675	-1025
69	CLS	2810	-1025
70	VSS	2870	-1025
71	C86	2930	-1025
72	P/S	3065	-1025
73	VDD	3125	-1025
74	VSS	3185	-1025
75	VDD	3245	-1025
76	DUMMY2	4139	-1025
77	C31	4200	-935
78	C30	4200	-875
79	C29	4200	-815
80	C28	4200	-755
81	C27	4200	-695
82	C26	4200	-635
83	C25	4200	-575
84	C24	4200	-515
85	C23	4200	-455
86	C22	4200	-395
87	C21	4200	-335
88	C20	4200	-275
89	C19	4200	-215
90	C18	4200	-155
91	C17	4200	-95
92	C16	4200	-35
93	C15	4200	25
94	C14	4200	85
95	C13	4200	145
96	C12	4200	205
97	C11	4200	265
98	C10	4200	325
99	C9	4200	385
100	C8	4200	445

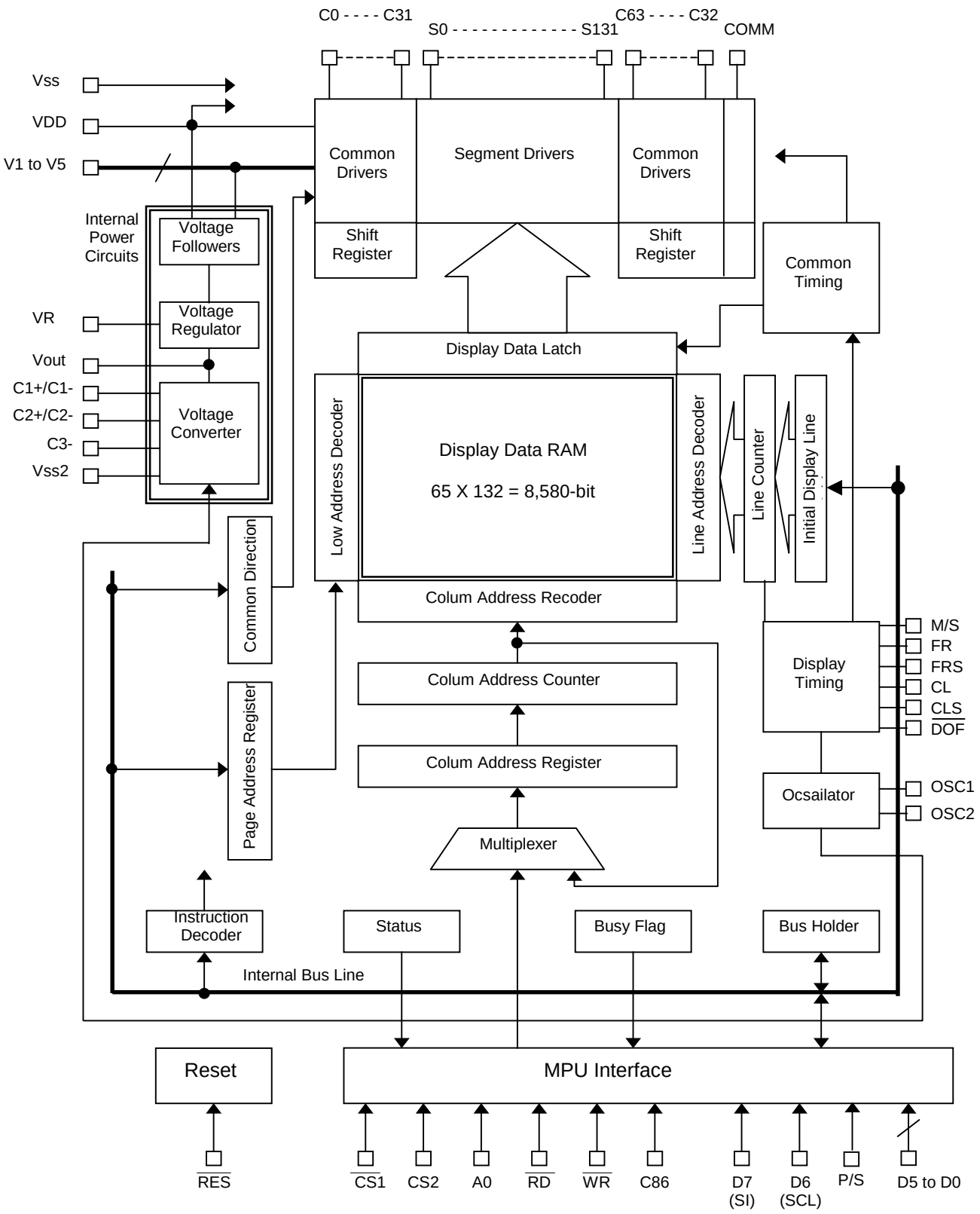
PAD No.	Terminal	X(um)	Y(um)
101	C7	4200	505
102	C6	4200	565
103	C5	4200	625
104	C4	4200	685
105	C3	4200	745
106	C2	4200	805
107	C1	4200	865
108	C0	4200	925
109	COMM	4200	985
110	DUMMY3	4119	1025
111	S0	3933	1025
112	S1	3873	1025
113	S2	3813	1025
114	S3	3753	1025
115	S4	3693	1025
116	S5	3633	1025
117	S6	3573	1025
118	S7	3513	1025
119	S8	3453	1025
120	S9	3393	1025
121	S10	3333	1025
122	S11	3273	1025
123	S12	3213	1025
124	S13	3153	1025
125	S14	3093	1025
126	S15	3033	1025
127	S16	2973	1025
128	S17	2913	1025
129	S18	2853	1025
130	S19	2793	1025
131	S20	2733	1025
132	S21	2673	1025
133	S22	2613	1025
134	S23	2553	1025
135	S24	2493	1025
136	S25	2433	1025
137	S26	2373	1025
138	S27	2313	1025
139	S28	2253	1025
140	S29	2193	1025
141	S30	2133	1025
142	S31	2073	1025
143	S32	2013	1025
144	S33	1953	1025
145	S34	1893	1025
146	S35	1833	1025
147	S36	1773	1025
148	S37	1713	1025
149	S38	1653	1025
150	S39	1593	1025

PAD No.	Terminal	X(um)	Y(um)
151	S40	1533	1025
152	S41	1473	1025
153	S42	1413	1025
154	S43	1353	1025
155	S44	1293	1025
156	S45	1233	1025
157	S46	1173	1025
158	S47	1113	1025
159	S48	1053	1025
160	S49	993	1025
161	S50	933	1025
162	S51	873	1025
163	S52	813	1025
164	S53	753	1025
165	S54	693	1025
166	S55	633	1025
167	S56	573	1025
168	S57	513	1025
169	S58	453	1025
170	S59	393	1025
171	S60	333	1025
172	S61	273	1025
173	S62	213	1025
174	S63	153	1025
175	S64	93	1025
176	S65	33	1025
177	S66	-27	1025
178	S67	-87	1025
179	S68	-147	1025
180	S69	-207	1025
181	S70	-267	1025
182	S71	-327	1025
183	S72	-387	1025
184	S73	-447	1025
185	S74	-507	1025
186	S75	-567	1025
187	S76	-627	1025
188	S77	-687	1025
189	S78	-747	1025
190	S79	-807	1025
191	S80	-867	1025
192	S81	-927	1025
193	S82	-987	1025
194	S83	-1047	1025
195	S84	-1107	1025
196	S85	-1167	1025
197	S86	-1227	1025
198	S87	-1287	1025
199	S88	-1347	1025
200	S89	-1407	1025

PAD No.	Terminal	X(um)	Y(um)
201	S90	-1467	1025
202	S91	-1527	1025
203	S92	-1587	1025
204	S93	-1647	1025
205	S94	-1707	1025
206	S95	-1767	1025
207	S96	-1827	1025
208	S97	-1887	1025
209	S98	-1947	1025
210	S99	-2007	1025
211	S100	-2067	1025
212	S101	-2127	1025
213	S102	-2187	1025
214	S103	-2247	1025
215	S104	-2307	1025
216	S105	-2367	1025
217	S106	-2427	1025
218	S107	-2487	1025
219	S108	-2547	1025
220	S109	-2607	1025
221	S110	-2667	1025
222	S111	-2727	1025
223	S112	-2787	1025
224	S113	-2847	1025
225	S114	-2907	1025
226	S115	-2967	1025
227	S116	-3027	1025
228	S117	-3087	1025
229	S118	-3147	1025
230	S119	-3207	1025
231	S120	-3267	1025
232	S121	-3327	1025
233	S122	-3387	1025
234	S123	-3447	1025
235	S124	-3507	1025
236	S125	-3567	1025
237	S126	-3627	1025
238	S127	-3687	1025
239	S128	-3747	1025
240	S129	-3807	1025
241	S130	-3867	1025
242	S131	-3927	1025
243	DUMMY4	-4119	1025
244	C32	-4200	985
245	C33	-4200	925
246	C34	-4200	865
247	C35	-4200	805
248	C36	-4200	745
249	C37	-4200	685
250	C38	-4200	625

PAD No.	Terminal	X(um)	Y(um)
251	C39	-4200	565
252	C40	-4200	505
253	C41	-4200	445
254	C42	-4200	385
255	C43	-4200	325
256	C44	-4200	265
257	C45	-4200	205
258	C46	-4200	145
259	C47	-4200	85
260	C48	-4200	25
261	C49	-4200	-35
262	C50	-4200	-95
263	C51	-4200	-155
264	C52	-4200	-215
265	C53	-4200	-275
266	C54	-4200	-335
267	C55	-4200	-395
268	C56	-4200	-455
269	C57	-4200	-515
270	C58	-4200	-575
271	C59	-4200	-635
272	C60	-4200	-695
273	C61	-4200	-755
274	C62	-4200	-815
275	C63	-4200	-875
276	COMM	-4200	-935

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

Power Supply Peripheral

No.	Symbol	Description
11,17 26~29 51,52 65~67 73,75	VDD	VDD=+3V
8,14, 3031, 32,49 50,70,74	VSS	VSS=0V
33~36	VSS2	Reference voltage for voltage booster
53,54 55,56 57,58 59,60 61,62	V1 V2 V3 V4 V5	LCD Driving Voltage Supplying Terminal. When the internal voltage booster is not used, supply each level of LCD driving voltage from outside with following relation. VDD≥V1≥V2≥V3≥V4≥V5 When the internal power supply is on, the internal circuits generate and supply following LCD bias voltage from V1 to V4 terminal.

Bias	V1	V2	V3	V4
1/7 Bias	V5+6/7VLCD	V5+5/7VLCD	V5+2/7VLCD	V5+1/7VLCD
1/9 Bias	V5+8/9VLCD	V5+7/9VLCD	V5+2/9VLCD	V5+1/9VLCD

(VLCD=VDD-V5)

LCD Driving Power Supply Peripheral

No.	Symbol	Description
41,42 43,44	C1+ C1-	Boosted capacitor connecting terminals used for voltage booster.
47,48 45,46	C2+ C2-	Boosted capacitor connecting terminals used for voltage booster.
39,40	C3-	Boosted capacitor connecting terminals used for voltage booster.
37,38	Vout	Voltage booster output terminal. Connect the boosted capacitor between this terminal and VSS2.
63,64	VR	Voltage adjust terminal. V5 level is adjusted by external bleeder resistance connecting between VDD and V5 terminal.

MPU Interface Peripheral

No.	Symbol	Description
18~25 (24,25)	D0~D7 (SCL, SI)	P/S="H" : Tri-state bi-directional Data I/O terminal in 8-bit parallel operation. P/S="L" : D7=Serial data input terminal. D6=Serial data clock signal input terminal. Data from SI is loaded at the rising edge of SCL and latched as the parallel data at 8th rising edge of SCL.
13	A0	Connect to the Address bus of MPU. The data on the D0 to D7 is distinguished between Display data and Instruction by status of A0.
12	$\overline{RES}$	Reset terminal. When the RES terminal goes to “L”, the initialization is performed. Reset operation is executing during “L” state of RES.
9 10	$\overline{CS1}$ CS2	Chip select terminal. Data Input/Output are available during CS1=”L” and CS2=”H”.

A0	H	L
Distin .	Display Data	Instruction

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>16</td><td>$\overline{RD}$
(E)</td><td><In case of 80 Type MPU> RD signal of 80 type MPU input terminal. Active "L" During this signal is "L" , D0 to D7 terminals are output. <In case of 68 Type MPU> Enable signal of 68 type MPU input terminal. Active "H"</td></tr>
<tr><td>15</td><td>$\overline{WR}$
(R/W)</td><td><In case of 80 Type MPU> Connect to the 80 type MPU WR signal. Actie "L". The data on the data bus input syncronizing the rise edge of this signal. <In case of 68 Type MPU> The read/write control signal of 68 type MPU input terminal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>71</td><td>C86</td><td>MPU interface type selection terminal.
<table>
<tr><td>C86</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>72</td><td>P/S</td><td>Serial or parallel interface selection terminal.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0~D7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td>“L”</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI(D7)</td><td>Write Only</td><td>SCL(D6)</td></tr>
</table>
RAM data and status read operation do not work in mode of the serial interface. In case of the serial interface (P/S="L"),RD and WR must be fixed "H" or "L", and D0 to D5 are high impedance.</td></tr>
<tr><td>2
3</td><td>OSC1
OSC2</td><td>System clock input terminal for Maker testing.(This terminal should be Open) For external clock operation, the clock shoud be input to OSC1 terminal.</td></tr>
<tr><td>69</td><td>CLS</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS=”H” : Internal oscillator circuit is enabld
CLS=”L” : Internal oscillator circuit is disabled (requires external input)
When CLS=”L”, input the display clock through the CL terminal.</td></tr>
<tr><td>68</td><td>M/S</td><td>This terminal selects the master/slave operation for the NJU6676. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the LCD, synchronizing the LCD system.
M/S = ”H” : Master operation
M/S = ”L” : Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>OSC.</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>$\overline{DOF}$</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Available</td><td>Available</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>Not Avail.</td><td>Available</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>*</td><td>Not Avail.</td><td>Not Avail.</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table>
*:Don’t Care</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>6</td><td>CL</td><td>Display clock input/output terminal.
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
<tr><td>“L”</td><td>*</td><td>Input</td></tr>
</table>
*:Don’t Care</td></tr>
<tr><td>5</td><td>FR</td><td>LCD alternating current signal I/O terminal.
M/S = ”H” : Output
M/S = ”L” : Input</td></tr>
<tr><td>7</td><td>$\overline{DOF}$</td><td>LCD Display blanking control terminal.
M/S = ”H” : Display “On” = “H”, Display “Off” = “L”
M/S = ”L” : External control. Refer to the following table.
<table>
<tr><th rowspan="2">Command</th><th colspan="2">DOF</th></tr>
<tr><th>H</th><th>L</th></tr>
<tr><td>Display On”</td><td>On</td><td>Off</td></tr>
<tr><td>Display Off”</td><td>Off</td><td>Off</td></tr>
</table></td></tr>
<tr><td>4</td><td>FRS</td><td>The output terminal for the static drive.
This terminal is used in conjunction with the FR terminal.</td></tr>
</table>

LCD Drivers

<table>
<tr><th>No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>77
~108</td><td>C31~C0</td><td>LCD driving signal output terminals.
-Segment output terminals : S0 ~ S131
-Common output terminal : C0 ~ C63
Segment output terminal
The following output voltages are selected by the combination of FR and data in the RAM.</td></tr>
<tr><td>111
~242</td><td>S0~S131</td><td>
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal</th><th>Reverse</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
</table></td></tr>
<tr><td>244
~275</td><td>C32~C63</td><td>Common output terminal
The following output voltages are selected by the combination of FR and status of common.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>VDD</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>109,
276</td><td>COMM</td><td>COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.</td></tr>
</table>

(Terminals 1,76,110,243 are Dummy Pad)

Functional description

(1) Block circuits description

(1-1) Busy Flag (BF)
During internal operation, the LSI is being busy and can't accept any instructions except "status read". The BF data is output through D7 terminal by the "status read" instruction.
When the cycle time (tcyc) mentioned in the "AC characteristics" is satisfied, the BF check isn't required after each instruction, so that MPU processing performance can be improved.

(1-2) Initial display line register
The initial display line register assigns a DDRAM line address, which corresponds, to COM0 by "initial display line set" instruction. It is used for not only normal display but also vertical display scrolling and page switching without changing the contents of the DDRAM.
However, the 65th address for icon display can't be assigned for initial display line address.

(1-3) Line counter
The line counter provides a DDRAM line address. It initializes its contents at the switching of frame timing signal (FR), and also counts-up in synchronization with common timing signal.

(1-4) Column address counter
The column address counter is an 8-bit preset counter which provides a DDRAM column address, and it is independent of below-mentioned page address register.
It will increment (+1) the column address whenever "display data read" or "display data write" instructions are issued. However, the counter will be locked when no-existing address above (84)H are addressed. The count-lock will be able to be released by the "column address set" instruction again. The counter can invert the correspondence between the column address and segment driver direction by means of "ADC set" instruction.

(1-5) Page address register
The page address register provides a DDRAM page address.
The last page address "8" should be used for icon display because the only D0 is valid.

(1-6) Display data RAM (DDRAM)
The DDRAM contains 8,580-bit, and stores display data which is 1-to-1 correspondents to LCD panel pixels.
When normal display mode, the display data "1" turns on and "0" turns off LCD pixels. When inverse display mode, "1" turns off and "0" turns on.

Fig.1 Display data RAM (DDRAM) Map

Page Address	Data	Display Pattern	Line Address	Common Driver
D3,D2,D1,D0 (0,0,0,0)	D0	Page 0	(00)H	COM0
	D1		01	COM1
	D2		02	COM2
	D3		03	COM3
	D4		04	COM4
	D5		05	COM5
	D6		06	COM6
	D7		07	COM7
D3,D2,D1,D0 (0,0,0,1)	D0	Page 1	08	COM8
	D1		09	COM9
	D2		0A	COM10
	D3		0B	COM11
	D4		0C	COM12
	D5		0D	COM13
	D6		0E	COM14
	D7		0F	COM15
D3,D2,D1,D0 (0,0,1,0)	D0	Page 2	10	COM16
	D1		11	COM17
	D2		12	COM18
	D3		13	COM19
	D4		14	COM20
	D5		15	COM21
	D6		16	COM22
	D7		17	COM23
	D0		18	COM24
	D1		19	COM25
	D2		1A	COM26
:	:	:	:	:
	D5		35	COM53
	D6		36	COM54
	D7		37	COM55
D3,D2,D1,D0 (0,1,1,1)	D0	Page 7	38	COM56
	D1		39	COM57
	D2		3A	COM58
	D3		3B	COM59
	D4		3C	COM60
	D5		3D	COM61
	D6		3E	COM62
	D7		3F	COM63
(1,0,0,0)	D0	Page 8	*	COMI

Column Address	ADC	"0"	00	01	02	03	04	05	06		82	83
		"1"	83	82	81	80	7F	7E	7D		01	00
	Segment Drivers		0	1	2	3	4	5	6		130	131

Initial

For example the Initial display is 08H.

Note) COMI is independent of the "Initial display line set" instruction and always corresponds to the 65th line.

(1-7) Common direction register
The common direction register specifies common driver's scanning direction.

Register A3	PAD No. / Pin name	Common drivers			
		108	77	275	244
		C0 ---------- C31		C63 ---------- C32	
0		COM0 ---------- COM31		COM63 ---------- COM32	
1		COM63 ---------- COM32		COM0 ---------- COM31	

(1-8) Reset circuit
The reset circuit initializes the LSI to the following status by using of the reset signal into the $\overline{RES}$ terminal.

Reset status using the $\overline{RES}$ terminal:

1. LCD Driver Set off
2. Display off
3. Normal Display (Non-inverse display)
4. ADC select : Normal mode (D0=0)
5. Power control register clear
6. Serial interface register clear
7. LCD bias select : 1/9 bias
8. Read modify write off
9. Static indicator off
10. Initial display line address : (00)H
11. Column address : (00)H
12. Page address : (0) page
13. Common direction register : Normal mode (D3=0)
14. EVR mode off and EVR register : (20)H
15. Test mode off
16. Entire display off : Normal mode

The $\overline{RES}$ terminal should be connected to MPU's reset terminal, and the reset operation should be executed at the same timing of the MPU reset.
As described in the "DC characteristics", it is necessary to input 10us or over "L" level signal into the $\overline{RES}$ terminal in order to carry out the reset operation. The LSI will return to normal operation after about 1us from the rising edge of the rest signal.
In case of using external power supply for LCD driving voltage, the $\overline{RES}$ terminal is required to be being "L" level when the external power supply is turned-on.
The "Reset" instruction in Table.4 can't be substituted for the reset operation by using of the $\overline{RES}$ terminal. It executes above-mentioned only 8 to 16 items.

(1-9) LCD display circuits

a) Common and segment drivers
LCD drivers consist of 64-common drivers, 132-segment divers and 1-icon-common driver.
As shown in Fig.7, LCD driving waveforms are generated by the combination of display data, common timing signal and internal FR timing signal.

b) Display data latch circuit
The display data latch circuit temporally stores 132-bit display data transferred from the DDRAM in the synchronization with the common timing signal, and then it transfers these stored data to the segment drivers.
"Display on/off", "inverse display on/off" and "entire display on/off" instructions control only the contents of this latch circuit, they can't change the contents of the DDRAM.
In addition, the LCD display isn't affected by the DDRAM accuses during its displaying because the data read-out timing from this latch circuit to the segment drivers is independent of accessing timing to the DDRAM.

c) Line counter and latch signal or latch Circuits
The clock line counter and latch signal to the latch circuits are generated from the internal display clock (CL). The line address of display data RAM is renewed synchronizing with display clock (CL).
132bits display data are latched in display latch circuits synchronizing with display clock, and then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

d) Display timing generator
The display timing generates the timing signal for the display system bay combination of the master clock CL and driving signal FR (refer to Fig.2) The frame signal FR and LCD alternative signal generate LCD driving waveform on the two frame alternative driving method.

e) Common timing generation
The common timing is generated by display clock CL (refer to Fig.2)

Fig.2 Display Timing

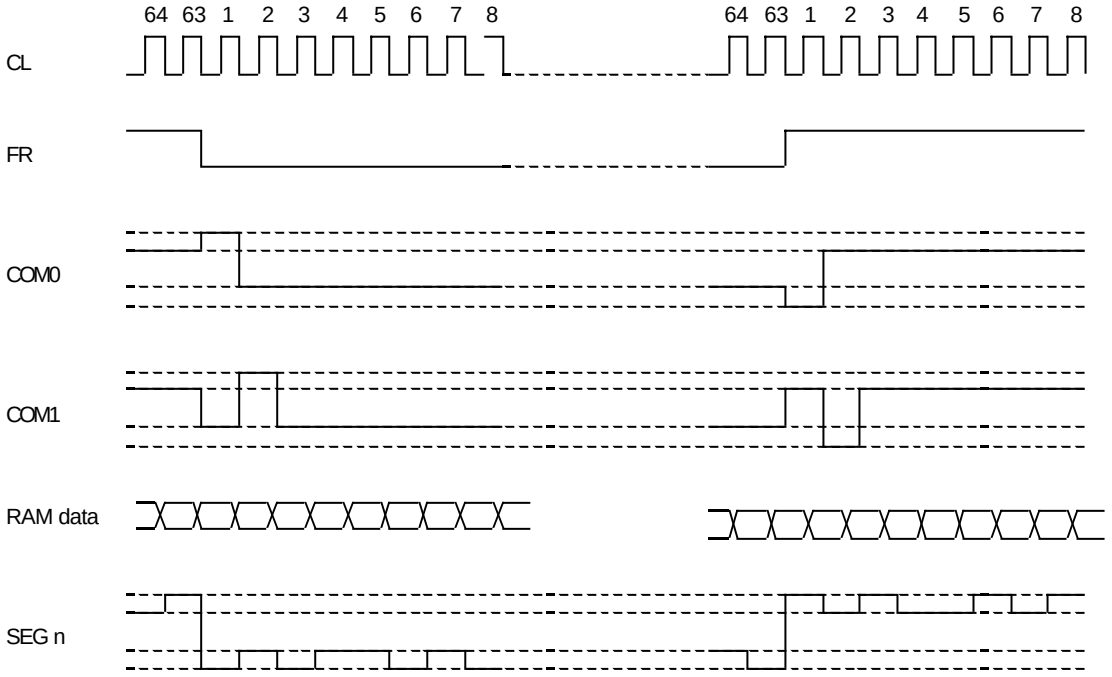


Fig.2 Waveform of Display Timing

f) Oscillator
This is the low power consumption CR oscillator which provides the display clock and voltage converter-timing clock.

e) Internal power circuits
The internal power circuits are composed of x4 boost voltage converter, output voltage regulator including 64-step EVR and voltage followers.
The optimum values of the external passive components for the internal power circuits, such as capacitors for V1 to V5 terminals and feed back resistors for VR terminal, depend on LCD panel size. Therefore, it is necessary to evaluate the actual LCD module with these external components in order to determine the optimum values.
Each portion of the internal power circuits is controlled by "power control set" instruction as shown in Table.1. In addition, the combination of power supply circuits is described in Table.2.

Table.1) Power control set

Bits	Portions	Status	
D2	Voltage converter	1 :On	0: Off
D1	Voltage regulator	1 :On	0: Off
D0	Voltage followers	1 :On	0: Off

Table.2) Power supply combinations

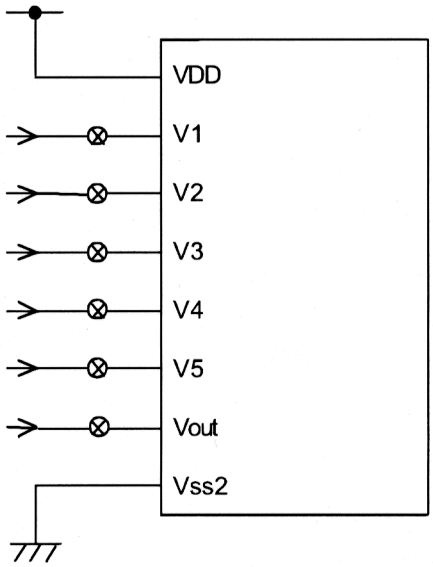
Status	D2	D1	D0	Voltage converter	Voltage regulator	Voltage followers	External voltage	Capacitor terminals
Using all internal power circuits	1	1	1	On	On	On	Vss2	Use
Using voltage regulator and Voltage followers	0	1	1	Off	On	On	Vout, Vss2	Open
Using voltage followers	0	0	1	Off	Off	On	V5, Vss2	Open
Using only external power supply	0	0	0	Off	Off	Off	V1 to V5	Open

Note1) Capacitor input terminals: C1+, C1-, C2+, C2-, C3-
Note2) Do not use other combinations except examples in Table.2.
Note3) Connect decoupling capacitors on V1 to V5 terminals whenever using the voltage followers.

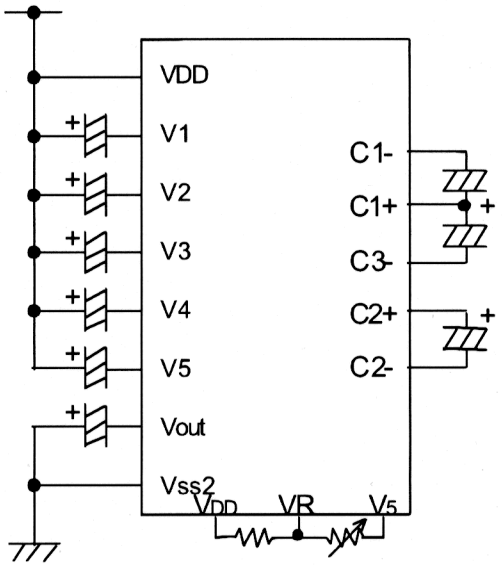
- Power Supply applications
  Power Control Instruction
  D2 : Boost Circuit
  D1 : Voltage Regulator
  D0 : Voltage Follower

1) External power supply operation.

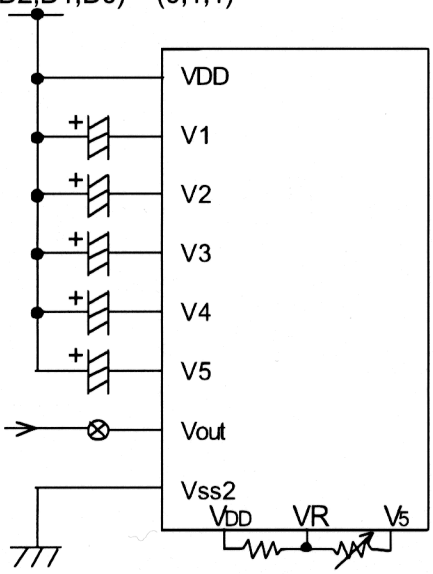
(D2,D1,D0) = (0,0,0)



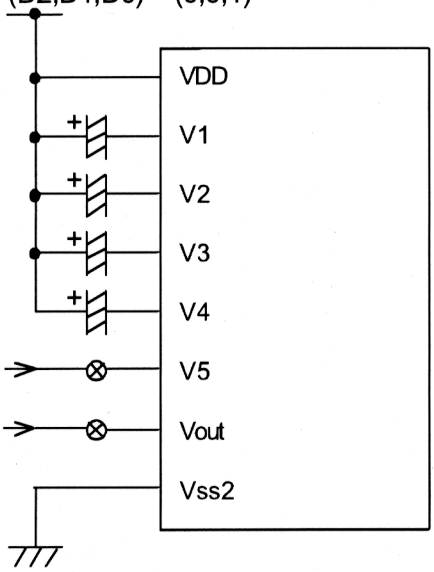
2) Internal power supply operation.
(Voltage Booster, Voltage Adj., Buffer(V/F))
(D2,D1,D0) = (1,1,1)



3) External power supply operation with Voltage Adjustment, Buffer(V/F)
(D2,D1,D0) = (0,1,1)



4) External power supply operation adjusted Voltage to V5.
(D2,D1,D0) = (0,0,1)



⊗ These switches should be open during the power save mode.

(2) Instruction set

The D7 to D0 data is distinguished as display data or instruction data by the combination of A0, $\overline{RD}$ and WR signals.

Table.3 Instruction table

Instruction		Instruction code											Description
		AO	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
1	Display On/Off	0	1	0	1	0	1	0	1	1	1	0 1	0 :Off 1 :On
2	Initial display line set	0	1	0	0	1	D5	D4	D3	D2	D1	D0	Specify DDRAM line address for COM0
3	Page address set	0	1	0	1	0	1	1	D3	D2	D1	D0	DDRAM page address
4	Column address set Upper 4-bit Column address set Lower 4-bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	D3 D3	D2 D2	D1 D1	D0 D0	DDRAM column address of upper 4-bits DDRAM column address of lower 4-bits
5	Status read	0	0	1	D7	D6	D5	D4	0	0	0	0	Read internal status
6	Display data write	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write DDARM data
7	Display data read	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read DDRAM data
8	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Select segment direction
9	Inverse display On/Off	0	1	0	1	0	1	0	0	1	1	0 1	0 : Normal display 1 : Inverse display on
10	Entire display On/Off	0	1	0	1	0	1	0	0	1	0	0 1	0 : Normal display 1 : Entire display on
11	LCD bias select	0	1	0	1	0	1	0	0	0	1	0 1	0 : 1/9 bias 1 : 1/7 bias
12	Read modify write	0	1	0	1	1	1	0	0	0	0	0	Increment column address
13	End	0	1	0	1	1	1	0	1	1	1	0	Release read modify write
14	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
15	Common direction select	0	1	0	1	1	0	0	0 1	*	*	*	Select common direction
16	Power control set	0	1	0	0	0	1	0	1	D2	D1	D0	Set the status of internal power circuits
17	Driver On/Off	0	1	0	1	1	1	0	0	1	1	0 1	0 : Driver Off 1 : Driver On
18	EVR mode set EVR register set	0 0	1 1	0 0	1 *	0 * *	0 D5	0 D4	0 D3	0 D2	0 D1	1 D0	Set EVR mode Set EVR register
19	Static indicator On/Off Static indicator register set	0 0	1 1	0 0	1 *	0 *	1 *	0 *	1 *	1 *	0 D1	0 1 D0	0 : Off 1 : On Set static indicator register
20	Power save mode On/Off	-	-	-	-	-	-	-	-	-	-	-	Dual commands of display Off & entire display On
21	NOP	0	1	0	1	1	1	0	0	0	1	1	
22	Test	0	1	0	1	1	1	1	*	*	*	*	Don't use

(3) Instruction description

3-1) Display On/Off
This instruction selects display turn-on or turn-off regardless of the contents of the DDRAM.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Display On or Off
0	1	0	1	0	1	0	1	1	1	0	0 :Off
										1	1 :On

3-2) Initial display line set
This instruction specifies the DDRAM line address which corresponds to the COM0 position.
By means of repeating this instruction, the initial display line address will be dynamically changed; it means smooth display scrolling will be enabled.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address for COM0
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					:	:	:	:	:	:	:
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

3-3) Page address set
In order to access to the DDRAM for writing or reading display data, both “page address set” and “column address set” instructions are required before accessing.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							:	:	:	:	:
							0	1	1	1	7
							1	0	0	0	8

3-4) Column address set

As above-mentioned, in order to access to the DDRAM for writing or reading display data, it is necessary to execute both "page address set" and "column address set" before accessing. The 8-bit column address data will be valid when both upper 4-bit and lower 4-bit data are set into the column address register.

Once the column address is set, it will automatically increment (+1) whenever the DDRAM will be accessed, so that the DDRAM will be able to be continuously accessed without "column address set" instruction.

The column address will stop increment and the page address will not be changed when the last address (83)H is addressed.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	Upper 4-bit
						0	A3	A2	A1	A0	Lower 4-bit

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

3-5) Status read

This instruction reads out the internal status regarding "busy flag", "ADC select", "display on/off" and "reset".

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	On/Off	RESET	0	0	0	0

BUSY : When D7 is "1", the LSI is being busy and can't accept any instructions.

ADC : It shows the correspondence between the column address and segment drivers.
When D6 is "0", the column address (131-n) corresponds to segment driver n.
When D6 is "1", the column address (n) corresponds to segment driver n.
Please be careful that read out data is opposite of "ADC select" instruction data.

On/Off : It shows display on or off status.
When D5 is "0", the LSI is in display-on status.
When D5 is "1", the LSI is in display-off status.
Please be careful that read out data is opposite of "ADC select" instruction data.

RESET : It shows reset status.
When D4 is "0", the LSI is in normal operation.
When D4 is "1", the LSI is during reset operation.

3-6) Display data write

This instruction writes display data into the selected column address on the DDRAM.

The column address automatically increments (+1) whenever the display data is written by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

3-7) Display data read

This instruction reads out the display data stored in the selected column address on the DDRAM.

The column address automatically increments (+1) whenever the display data is read out by this instruction, so that this instruction can be continuously issued without “column address set” instruction.

After the ”column address set” instruction, a dummy read will be required, please refer to the (5-4).

In case of using serial interface mode, this instruction can’t be used.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

3-8) ADC select

This instruction selects segment driver direction.

The correspondence between the column address and segment driver direction is shown in Fig.1.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Segment driver direction
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Inverse

3-9) Inverse display On/Off

This instruction inverses the status of turn-on or turn-off of entire LCD pixels. It doesn’t change the contents of the DDRAM.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Display status
0	1	0	1	0	1	0	0	1	1	0	Normal
										1	Inverse

3-10) Entire display On/Off

This instruction turns on entire LCD pixels regardless the contents of the DDRAM. It doesn’t change the contents of DDRAM.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Entire display on/off
0	1	0	1	0	1	0	0	1	0	0	Normal
										1	Entire display on

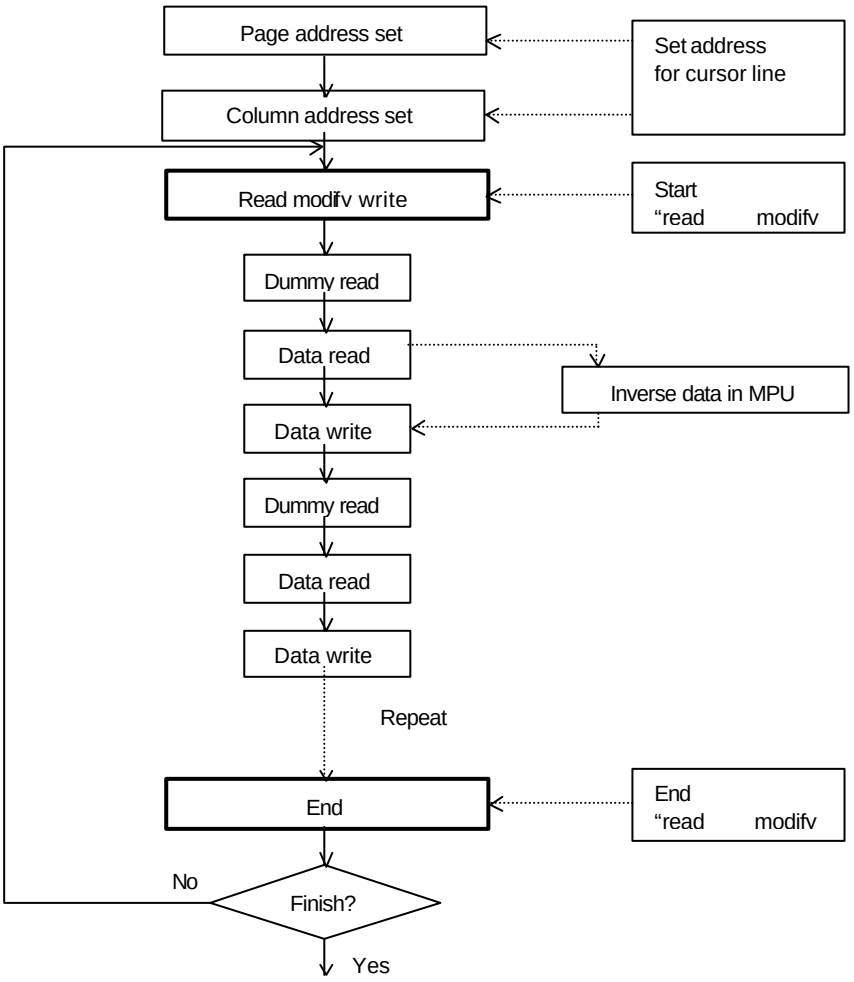
3-11) LCD bias set
This instruction selects LCD bias value.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	LCD bias
0	1	0	1	0	1	0	0	0	1	0	1/9
										1	1/7

3-12) Read modify write
This instruction controls column address increment.
By using of this instruction, the column address can't increment when read operation but it can increment when write operation. This status will be continued until the below-mentioned "end" instruction will be issued.
This instruction can reduce the load of MPU, during the display data in specific DDRAM area is repeatedly changed for cursor blink or others.

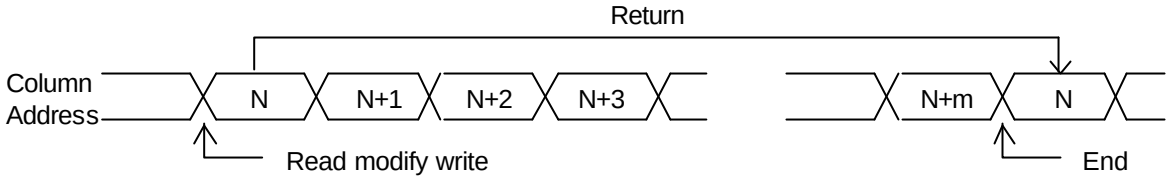
A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

The sequence of cursor blink display



3-13) End
The “end” instruction cancels the read modify write mode and makes the column address return to the initial value just before “read modify write” is started.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



3-14) Reset
This instruction reset the LSI to the following status, however it doesn’t change the contents of the DDRAM. Please be careful that it can’t be substituted for the reset operation by using of the RES terminal.

Reset status by “reset” instruction:

1. Read modify write off
2. Static indicator off
3. Initial display line address : (00)H
4. Column address : (00)H
5. Page address : (0) page
6. Common direction register : Normal mode (D3=0)
7. EVR mode off and EVR register : (20)H
8. Test mode off

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

3-15) Common driver direction select
This instruction selects common driver direction.
Please refer to (1-7) common driver direction for more detail.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Common driver direction
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Inverse

3-16) Power control set

This instruction controls the status of internal power circuits. Please refer to the (4) internal power supply circuits for more detail.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Status
0	1	0	0	0	1	0	1	0			Voltage converte r off
								1			Voltage converter on
									0		Voltage regulator off
									1		Voltage regulator on
										0	Voltage followers off
										1	Voltage followers on

Note) The internal power supply must be Off when external power supply using.

* The wait time depends on the C3 to C7, COUT capacitors, and VDD and VLCD Voltage. Therefore it requires the actual evaluation using the LCD module to get the correct time.

T.B.D

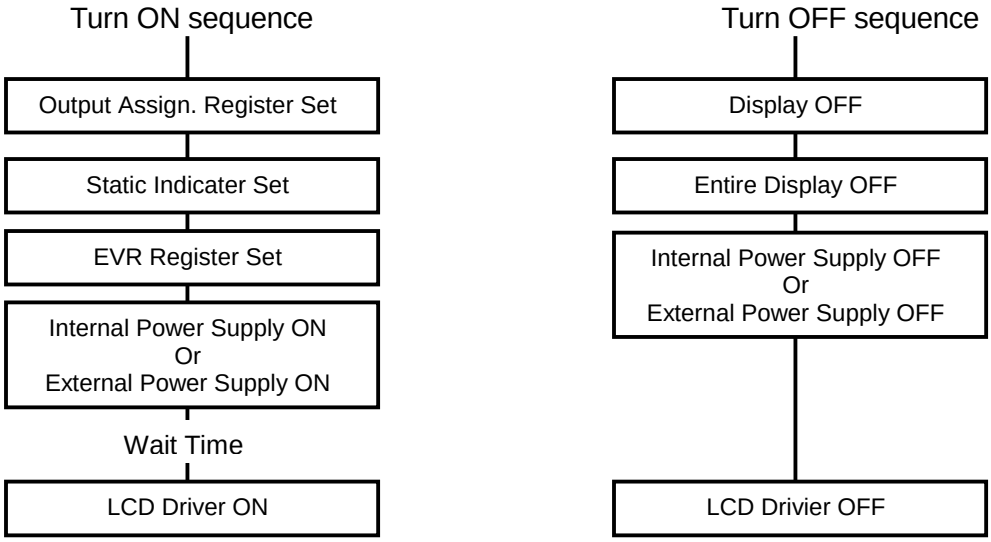
3-17) LCD Driver On/Off

This instruction controls LCD driving waveform output through the COM/SEG terminals.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Driver
0	1	0	1	1	1	0	0	1	1	0	Off
										1	On

The NJU6676 contains low power LCD driving voltage generator circuit reducing own operating current. Therefore , it requires the following sequence procedures at power on for power source stabilized operation.

LCD Driving power supply On/Off sequences
The following sequences required when the power supply is turned On/Off.
When the power supply is turned on again after the turn off (by the power save instruction), the power save release sequence(3-22) is required.



3-18) EVR mode set
This instruction sets the LSI into the EVR mode, and it is always used by the combination with “EVR register set”.
The LSI can’t accept any instructions except the “EVR register set” during the EVR set mode. This mode will be released after the “EVR register set” instruction.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

3-19) EVR register set
This instruction sets 6-bit data into the EVR register to determine the output voltage “V5” of the internal voltage regulator.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	V5
0	1	0	*	*	0	0	0	0	0	0	Minimum
					0	0	0	0	0	1	:
					:	:	;	:	:	:	:
					1	1	1	1	1	0	:
					1	1	1	1	1	1	Maximum

3-20) Static indicator on/off
This instruction selects static indicator turn-on or turn-off, and it is always used by the combination with the “ static indicator register set”.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	Off
										1	On

3-21) Static indicator register set
This instruction sets 2-bit data into the static indicator register.

A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Status
0	1	0	*	*	*	*	*	*	0	0	Off
									0	1	On (Blink at 1.0 s intervals)
									1	0	On (Blink at 0.5s intervals)
									1	1	On (Turn on at all time)

3-22) Power save mode On/Off
This instruction sets the LSI into the power save mode by the combination of "display off" and "whole display on" instructions for reducing operating current as well as static operation's.
The internal status and the contents of the DDRAM will be remained just before the "power save mode on/off" instruction. In addition, the DDRAM can be accessed during the power save mode.
There are two power save modes, sleep mode and standby mode.

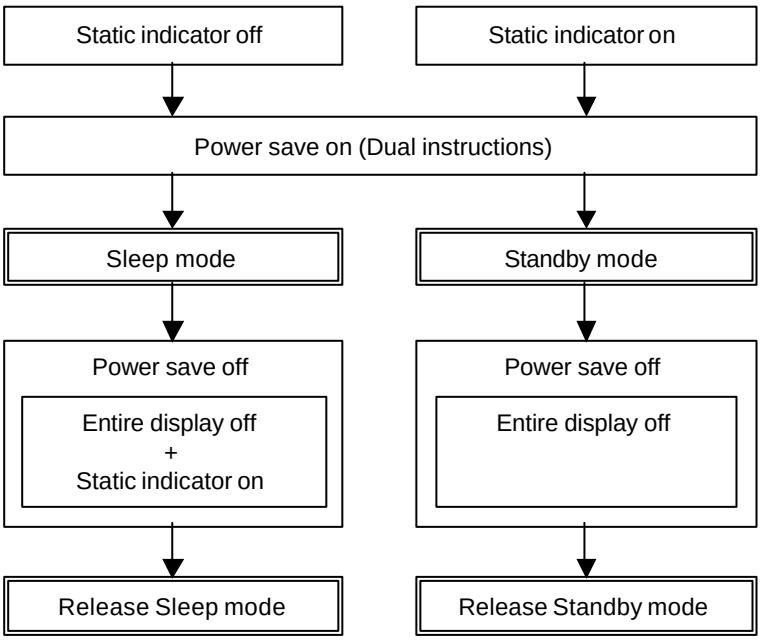
During sleep mode:
All LCD system stops as follows,

1. Oscillator and internal power circuits stop.
2. All common and segment drivers output VDD level.

During standby mode:
The LCD system except the static indicator stops as follows,

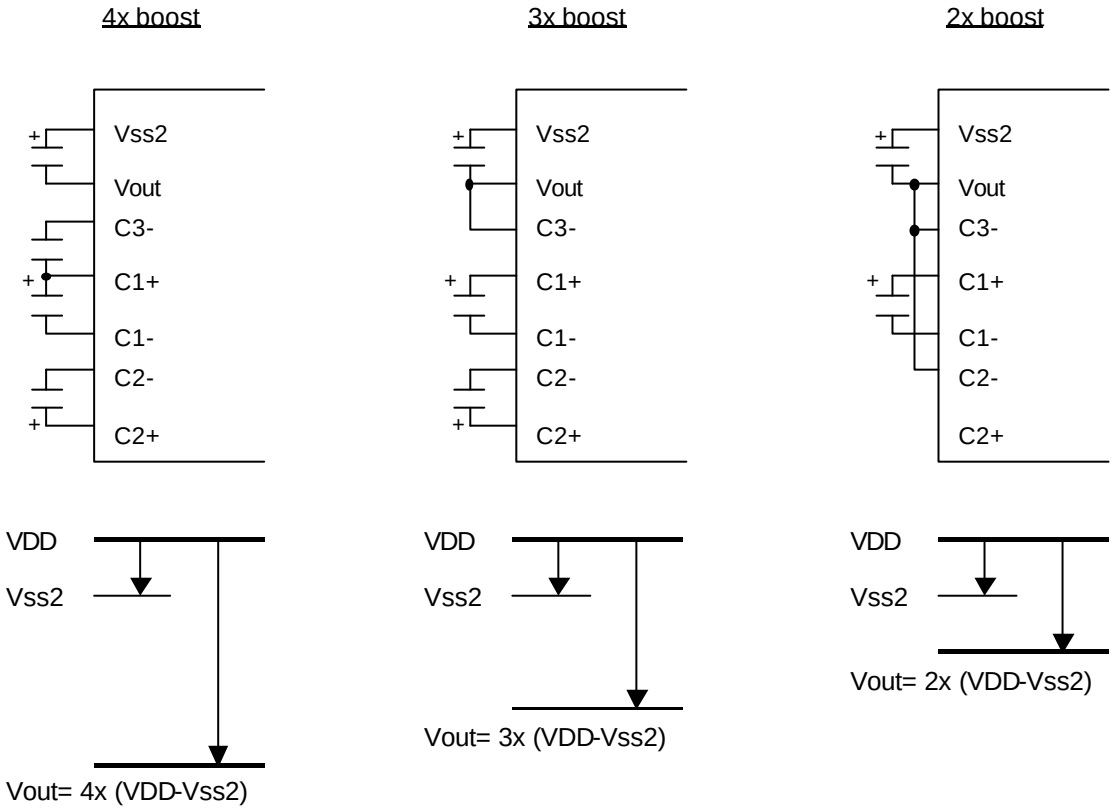
1. Oscillator and internal power circuits stop.
2. All common and segment drivers output VDD level.
3. The only static indicator is operating.

Fig.5 The sequence of power save mode



(4) Internal power circuits
(a)Voltage converter
The voltage converter generates maximum 4x boosted negative-voltage from the voltage between VDD and Vss2. The boosted voltage is output from the VOUT terminal.
The internal oscillator is required to be operating when using this converter, because the divided signal provided from the oscillator is used for the internal timing of this circuit.
The boosted voltage between VDD and Vout must not exceed 18.0V.
The voltage converter requires external capacitors for boosting as shown in Fig.7.

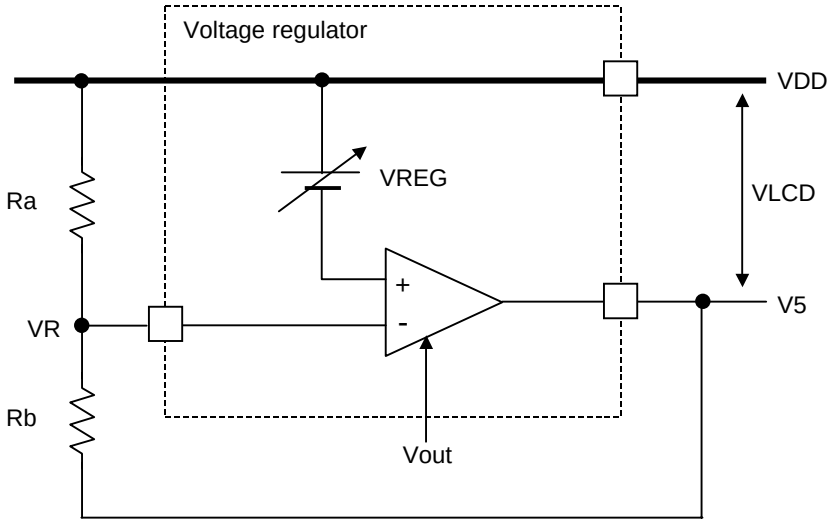
Fig.7 The capacitors connection for the voltage regulator:



(b)Contrast control using the voltage regulator

The voltage regulator determines the LCD driving voltage “V5” according to the Rb/Ra ratio and VREG voltage. The equations to calculate V5 are as follows:

Fig.5 Voltage regulator circuit



VLCD = VDD – V5
= (1+Rb/Ra) x VREG ---[1]
VREG = (n/162) x (VDD-Vss2) ---[2]

VLCD : LCD driving voltage
Ra, Rb : Feed back resistors
VREG : Contrast control voltage
n : Parameter decided instruction

(c)Contrast control voltage VREG

As the equation [2] shows, the VREG value depends on the parameter “n”. The “n” is selected a value within 99 to 162 by using of “EVR register set” instruction as described in Table.8.

Table.8 The relationship between EVR register and VLCD level

Register value	D5	D4	D3	D2	D1	D0	n	VREG	
00	0	0	0	0	0	0	99	(99/162) x (VDD-Vss2)	Minimum
01	0	0	0	0	0	1	100	(100/162) x (VDD-Vss2)	:
02	0	0	0	0	1	0	101	(101/162) x (VDD-Vss2)	:
:	:	:	:	:	:	:	:		:
61	1	1	1	1	0	1	160	(160/162) x (VDD-Vss2)	:
62	1	1	1	1	1	0	161	(161/162) x (VDD-Vss2)	:
63	1	1	1	1	1	1	162	(162/162) x (VDD-Vss2)	Maximum

- VLCD setting example

We recommend the total value of Ra and Rb is between 1MΩ and 5MΩ. When using Ra=1MΩ, Rb=4MΩ and VDD=3V, the VLCD is calculated as follows:

The minimum VLCD:

VLCD =(1+Rb/Ra) X VREG
=(1+4/1) X [(99/162) X 3.0]
=9.15V

The maximum VLCD:

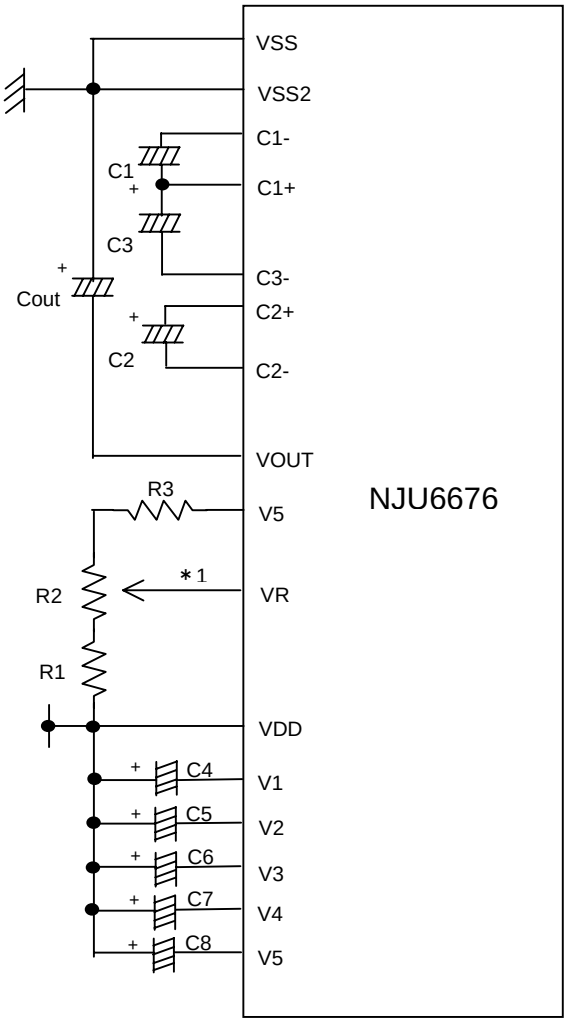
VLCD =(1+Rb/Ra) X VREG
=(1+4/1) X [(162/162) X 3.0]
=15.0V

(d) LCD Driving Voltage Generation Circuits

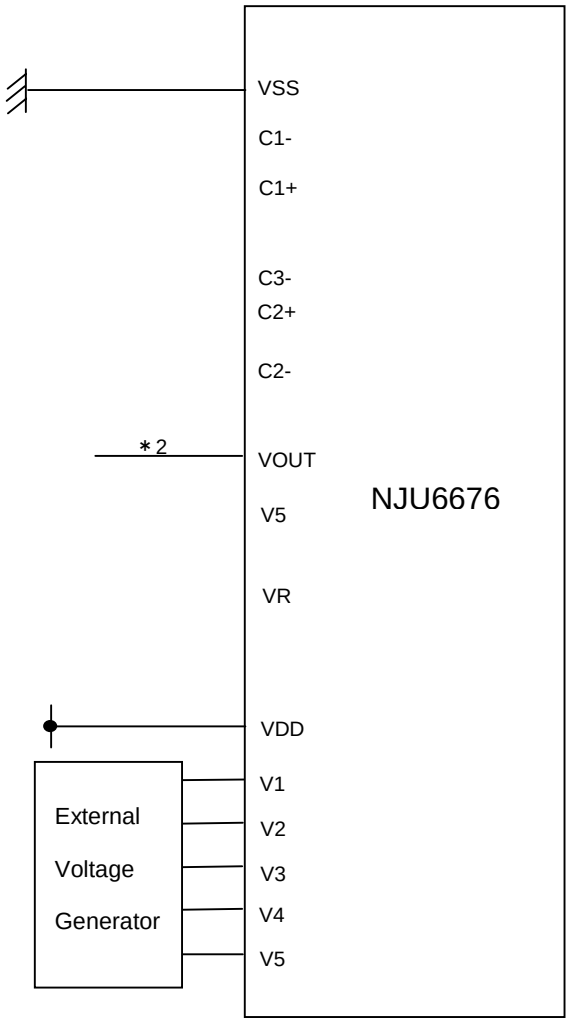
The LCD driving bias voltage of V1,V2,V3,V4 are generated internally by dividing the V5 voltage with the internal bleeder resistance. And it is supplied to the LCD driving circuits after the impedance conversion with voltage follower circuit.

As shown in below, Five capacitors are required to connect to each LCD driving voltage terminal for voltage stabilizing. And the value of capacitors C4, C5, C6, C7, and C8 are determined depending on the actual LCD panel display evaluation.

Using the internal Power Supply



Using the external Power Supply



*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of VOUT is required when external power supply using.

When VSS > V5 --- VOUT=V5

When VSS < V5 --- VOUT=VSS

Reference set up value

VLCD=VDD-V5=9.0 to 10.5V

COUT	~1.0uF
C1/C2/C3	~1.0uF
C4 ~ C8	0.1~0.47uF
R1	2MΩ
R2	500KΩ
R3	2.5MΩ

(5) MPU interface

(5-1) Interface type selection

NJU6676 interfaces with MPU by 8-bit bidirectional data bus (D7 to D0) or serial (SI:D7). The 8 bit parallel or serial interface is determined by a condition of the P/S terminal connecting to "H" or "L" level as shown in Table 4. In case of the serial interface, status and RAM data read out operation is impossible.

Table4

P/S	Type	CS1	A0	RD	WR	C86	SI(D7)	SCL(D6)	D0-D5
H	Parallel	CS1	A0	RD	WR	C86	D7	D6	D0-D5
L	Serial	CS1	A0	-	-	-	SI	SCL	Hi-z

"-" : They should be fixed to "H" or "L".

(5-2) Parallel Interface

The NJU6676 interfaces to 68 or 80 type MPU directly when the parallel interface (P/S="H") is selected. 68 type MPU or 80 is determined by the condition of C86 terminal connecting to "H" or "L" as shown in table 5.

Table 5

C86	Type	CS1	A0	RD	WR	D0-D7
H	68 type MPU	CS1	A0	E	R/W	D0-D7
L	80 type MPU	CS1	A0	RD	$\overline{WR}$	D0-D7

(5-3) Discrimination of Data Bus Signal

The NJU6676 discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 6.

Table 6

Common	68 type	80 type		Function
A0	R/W	RD	WR	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminal $\overline{CS}1$ set to "L"and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition when the chip is not selected. The data input from SI terminal is MSB first like as the order of D7,D6,- - - - D0, and the data are entered into the shift register synchronizing with the rise edge of the serial clock SCL. The data in the shift register are converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction of the serial input data is executed by the condition of A0 at the 8th serial clock rise edge. A0="H" is display data and A0="L" is instruction. When RES terminal becomes "L" or CS1 terminal becomes "H" before 8th serial clock rise edge, NJU6676 recognizes them as a instruction data incorrectly. Therefore a unit of serial data must be structured by 8-bit. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

Note) The read out function, such as the status or RAM data read out, is not supported in this serial interface

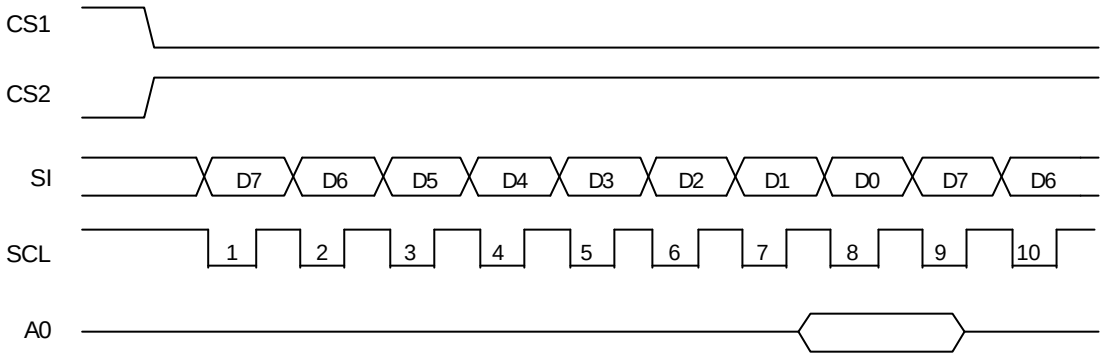


Fig.5

5-5) Access to the Display Data RAM and Internal Register.

The NJU6676 is operating as one of pipeline processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU reads out the data from the Display Data RAM, the read out data in the data read cycle (dummy read) is held in the bus-holder, then it is read out from the bus-holder to the system bus at the next data read cycle. When the MPU writes the data into the Display Data RAM, the data is held in the bus-holder, then it is written into the Display Data RAM by the next data write cycle.

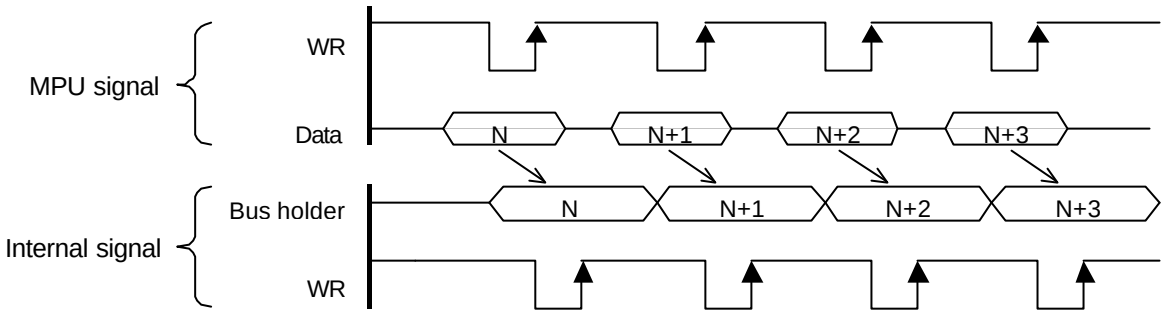
Therefore high speed data transmission between MPU and NJU6676 is available because of it is not limited by the tACC and tDS as display data RAM access time and is limited by the system cycle time (R) or (W).

If the cycle time is not be kept in the MPU operation, NOP should be inserted to the system instead of the waiting operation.

The read out operation does not read out the data in the pointed address just after the address set operation. And second read out operation can read out the data correctly from the pointed address.

Therefore, one dummy read operation is required after address setting or write cycle as shown in FIG. 6..

Write timing



Read timing

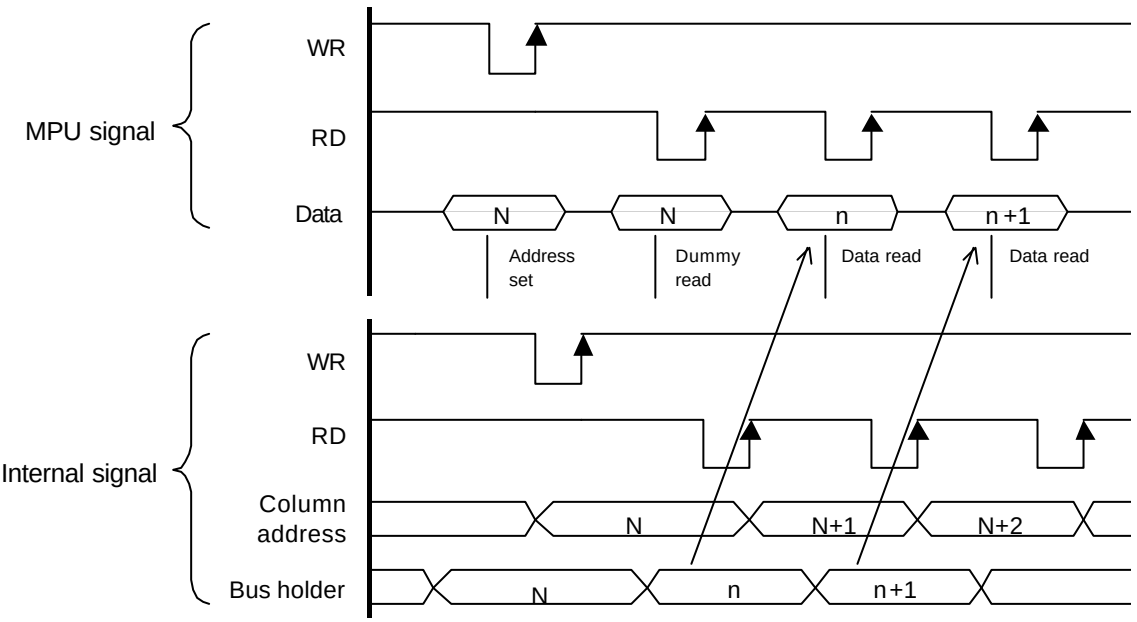


Fig.6

5-5) Chip select
CS1, CS2 are Chip Select terminals. In case of $\overline{CS1}$="L" and CS2="H", the interface with MPU is available. In case of $\overline{CS1}$="H" or CS2="L", the D0 to D7 are high impedance and A0, RD, WR, D7(SI) and D6(SCL) inputs are ignored. If the serial interface is selected when CS1="H" or CS2="L", the shift register and the counter are reset. However, the reset is always operated in any conditions of CS1 and $\overline{CS2}$.

■ ABSOLUTE MAXIMUMN RATINGS

Ta=25°C

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to +7.0	V
Supply voltage	Vss2	-7.0 to+0.3 -6.0 to +0.3 (When using 3x voltage converter) -4.5 to +0.3 (When using 4x voltage converter)	V
Supply voltage	V5 Vout	-18.0 to +0.3	V
Supply voltage	V1,V2 V3,V4	V5 to +0.3	V
Input voltage	Vin	-0.3 to VDD+0.3	V
Operating temperature	Topr	-30 to +80	°C
Storage temperature	Tstg	-55 to +100 (TCP) -55 to +125 (Chip)	°C

Note1) All voltages are relative to the Vss = 0V reference.
The relationship among the supply voltages should be maintained the following condition.
VDD≥V0≥V1≥V2≥V3≥V4≥V5;VDD>Vss≥Vout

Note2) When using the external power supply for LCD driving, the external power should be turn on at the same timing of VDD or after VDD.

Note3) The LSI should be operated inside of the absolute maximum ratings in order to prevent excessive stress. Otherwise, the stresses beyond the absolute maximum ratings may cause permanent damage to the LSI.

Note4) The decoupling capacitor between VDD terminal and Vss terminal is required in order to stabilize the LSI operation.

DC Electrical Characteristics

VDD=2.7V to 3.3V, Vss=0V, Ta=-30 to +80°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Power supply(1)	VDD	Recommend	2.7	-	3.3	V	5
		Possible	2.2	-	5.5	V	
Power supply(2)	Vss1		VDD-6.0	-	VDD-2.5	V	
Power supply(3)	V5	VLCD=VDD-V5	VDD-18	-	VDD-6	V	
	V1,V2		0.4xV5	-	VDD	V	
	V3,V4		V5	-	0.6xV5	V	
"H" level input voltage	VIHC1		0.8VDD	-	VDD	V	
"L" level input voltage	VILC1		Vss	-	0.2VDD	V	
"H" level output voltage	VOHC1	IOH=-0.5mA	0.8VDD	-	VDD	V	
"L" level output voltage	VOLC1	IO=0.5mA	Vss	-	0.2VDD	V	
Input leakage current	ILI		-1.0	-	1.0	UA	
Output leakage current	ILO		-3.0	-	3.0	uA	
LCD on resistance	RON1	VLCD=14.0V, Ta=25°C	-	2.0	3.5	kΩ	6
	RON2	VLCD=8.0V, Ta=25°C	-	3.2	5.4	kΩ	
Input pin capacitance	CIN	Ta=25°C	-	10	-	pF	9
Oscillation frequency	FOSC	Ta=25°C	18	22	26	KHz	
Reset time	TR	Using RES terminal	1.0	-	-	us	10
Reset pulse width	TRW		10	-	-	us	11

Internal power supply

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input voltage	VDD1	VDD-Vss Using 3x voltage converter	-6.0	-	-2.5	V	
	VDD2	VDD-Vss Using x4 voltage converter	-4.5	-	-2.5	V	12
Voltage converter Output voltage	Vout		-18.0	-	-	V	
Voltage converter Output on resustance	RSTEP	C1 to C3, Cout=1.0uF Using x4 booster	-	2500	3500	Ω	
Volateg regulator Operating voltage	Vout	Voltage converter off	VDD -18.0V	-	VDD -6.0V	V	13
Voltage follower Operating voltagae	V5	Voltage regulator off	VDD -18.0V	-	VDD -6.0V	V	
Operating current	IDDQ1	When sleep mode	-	0.01	5.0	uA	14
	IDDQ2	When standby mode	-	4	10	uA	
	IDD1	VDD=3V, V5=-11V	-	80	140	uA	
	IDD2	Checker flag display	-	20	40	uA	
	IDD3	Without MPU access	-	18	35	uA	
	IDD4	All COM/SEG open	-	15	30	uA	
Reference Voltage	VREG	VDD=3V, Ta=25°C			3.0	%	

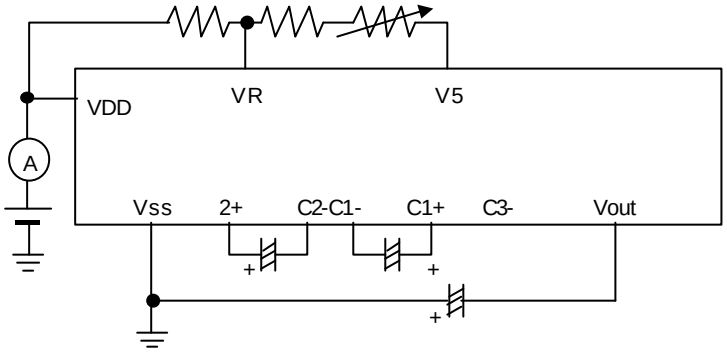
Note5) This parameter can't be guaranteed for spike voltage during MPU access.
Note6) Apply to the resistance between each driver (COM, SEG) and power supply terminal (V1,V2,V3,V4) when 0.1V voltage difference is supplied between these terminals.
Note7,8)Apply to the condition when internal power circuits aren't used.
Note7) Apply to the condition when MPU doesn't access to the LSI.
Note8) Apply to the condition when writing checker flag pattern to the DDRAM at the timing of tcyc.
Note9) Apply to A0, D7 to D0, RD, WR, CS, RES, C86 and P/S terminals.
Note10) Specified the time between the rising edge of the RES signal and completion of reset operation.

Note11) specified the minimum pulse width of RES signal.
Note12) Apply to theVDD when using quadrupler.
Note13) LCD driving voltage can be adjusted within the voltage follower operating range.
Note14) Each value are specified in the following conditions:

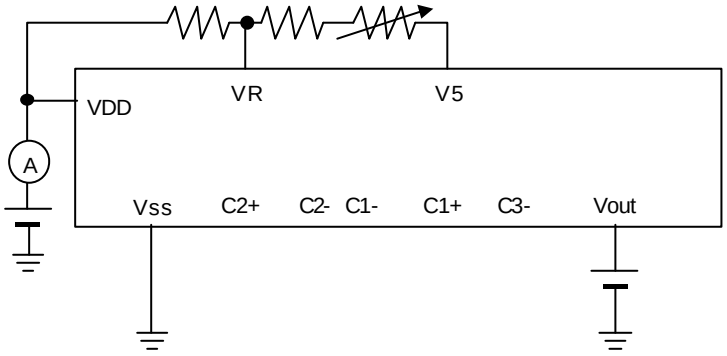
Symbol	Power Control			Operating Condition			External Voltage Supply (Input Terminal)
	D2	D1	D0	Voltage converter	Voltage regulator	Voltage followers	
Iout1	1	1	1	On	On	On	Use(VSS2)
Iout2	0	1	1	Off	On	On	Use(VOUT,VSS2)
Iout3	0	0	1	Off	Off	On	Use(V5,VSS2)
Iout4	0	0	0	Off	Off	Off	Use(V1~V5)

IDD 1,2,3,4 measurement circuits:

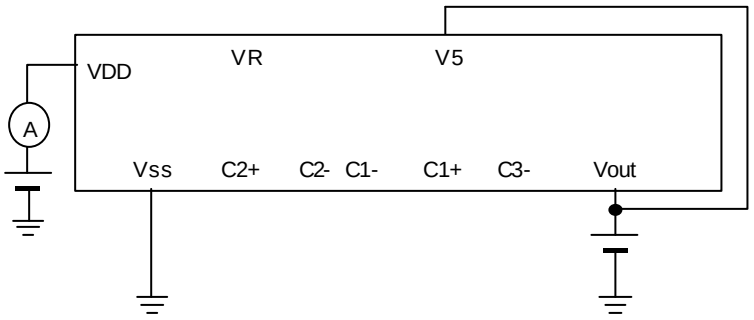
IDD1



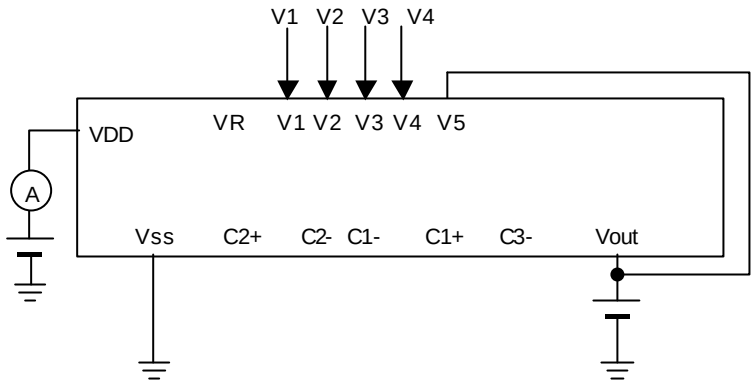
IDD2



IDD3

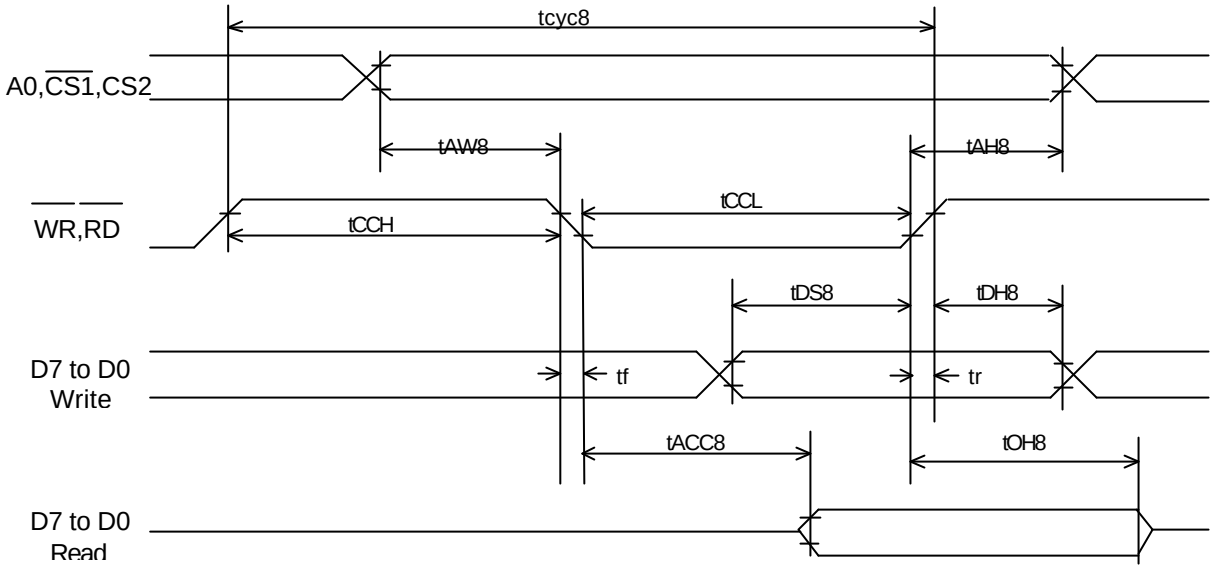


IDD4



■ BUS TIMING CHARACTERISTICS

Read and Write characteristics (80 type MPU)



(Vss=0V, VDD=4.5 to 5.5V, Ta=-30 to 80°C)

Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,CS1, CS2	tAH8		0	-	ns
Address set up time		tAW8		0	-	ns
System cycle time	WR,RD	tcyc8		166	-	ns
Control "H" pulse width (Read)		tCCHR		30	-	ns
Control "H" pulse width (Write)		tCCHW		70	-	ns
Control "L" pulse width (Read)		tCCLR		30	-	ns
Control "L" pulse width (Write)		tCCLW		30	-	ns
Data set up time	D7 ~ D0	tDS8		30	-	ns
Data hold time		tDH8		10	-	ns
RD access time		tACC8	CL=100pF	-	70	ns
Output disable time		tOH8		5	50	ns
Input signal rising, falling edge	CS1,CS2 RW,RD,A0, D7 ~ D0	tr,tf			15	ns

(Vss=0V, VDD=2.7 to 4.5V, Ta=-30 to 80°C)

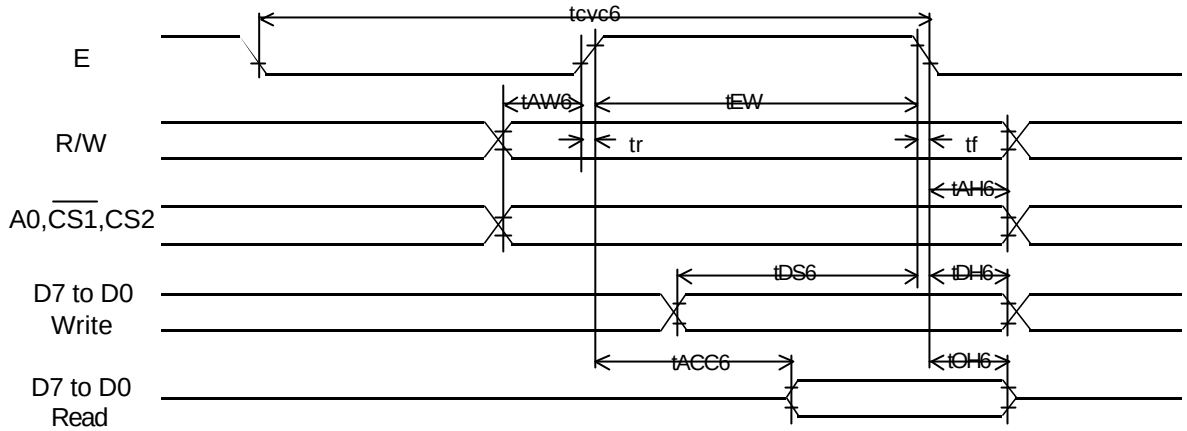
Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,CS1, CS2	tAH8		0	-	ns
Address set up time		tAW8		0	-	ns
System cycle time	WR,RD	tcyc8		300	-	ns
Control "H" pulse width (Read)		tCCHR		60	-	ns
Control "H" pulse width (Write)		tCCHW		120	-	ns
Control "L" pulse width (Read)		tCCLR		60	-	ns
Control "L" pulse width (Write)		tCCLW		60	-	ns
Data set up time	D7 ~ D0	tDS8		40	-	ns
Data hold time		tDH8		15	-	ns
RD access time		tACC8	CL=100pF	-	140	ns
Output disable time		tOH8		10	100	ns
Input signal rising, falling edge	CS1,CS2 RW,RD,A0, D7 ~ D0	tr,tf			15	ns

(Vss=0V, VDD=2.2 to 2.7V, Ta=-30 to 80°C)

Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,CS1, CS2	tAH8		0	-	ns
Address set up time		tAW8		0	-	ns
System cycle time	WR,RD	tcyc8		1000	-	ns
Control "H" pulse width (Read)		tCCHR		120	-	ns
Control "H" pulse width (Write)		tCCHW		240	-	ns
Control "L" pulse width (Read)		tCCLR		120	-	ns
Control "L" pulse width (Write)		tCCLW		120	-	ns
Data set up time	D7 ~ D0	tDS8		80	-	ns
Data hold time		tDH8		30	-	ns
RD access time		tACC8	CL=100pF	-	280	ns
Output disable time		tOH8		10	200	ns
Input signal rising, falling edge	CS1,CS2 RW,RD,A0, D7 ~ D0	tr,tf			15	ns

Note) Each timing is specified based on 0.2xVDD and 0.8xVDD.

Read and Write characteristics (68 type MPU)



(Vss=0V, VDD=4.5 to 5.5V, Ta=-30 to 80°C)

Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,CS1, CS2	tAH6		0	-	ns
Address set up time		tAW6		0	-	ns
System cycle time		tcyc6		166	-	ns
Enable "H" pulse width (Read)	E	tCCHR		70	-	ns
Enable "H" pulse width (Write)		tCCHW		30	-	ns
Enable "L" pulse width (Read)		tCCLR		30	-	ns
Enable "L" pulse width (Write)		tCCLW		30	-	ns
Data set up time	D7 ~ D0	tDS6		30	-	ns
Data hold time		tDH6		10	-	ns
RD access time		tACC6	CL=100pF	-	70	ns
Output disable time		tOH6		10	50	ns
Input signal rising, falling edge	E,R/W,A0, D7 ~ D0	tr,tf			15	ns

(Vss=0V, VDD=2.7 to 4.5V, Ta=-30 to 80°C)

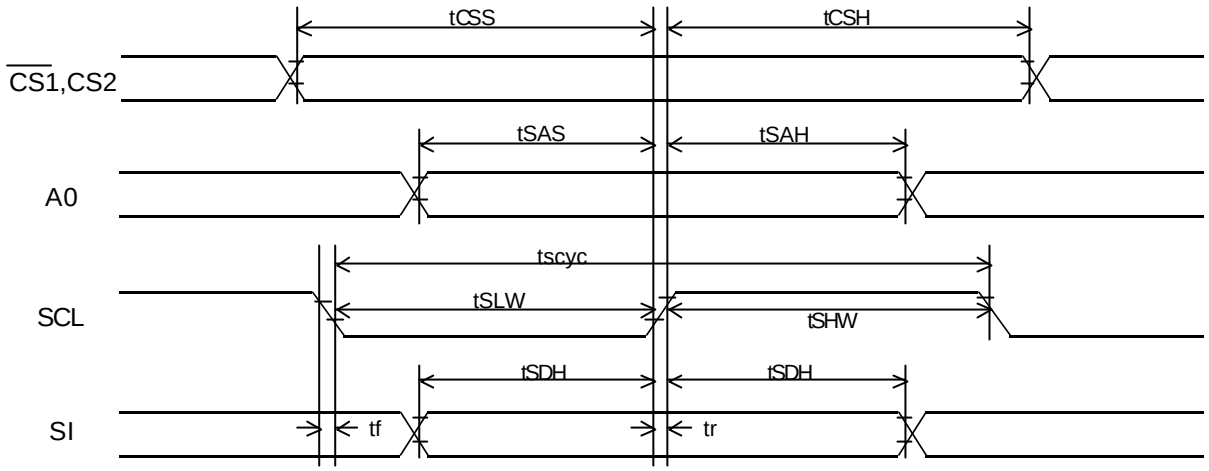
Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,CS1, CS2	tAH6		0	-	ns
Address set up time		tAW6		0	-	ns
System cycle time		tcyc6		300	-	ns
Enable "H" pulse width (Read)	E	tCCHR		120	-	ns
Enable "H" pulse width (Write)		tCCHW		60	-	ns
Enable "L" pulse width (Read)		tCCLR		60	-	ns
Enable "L" pulse width (Write)		tCCLW		60	-	ns
Data set up time	D7 ~ D0	tDS6		40	-	ns
Data hold time		tDH6		15	-	ns
RD access time		tACC6	CL=100pF	-	140	ns
Output disable time		tOH6		10	100	ns
Input signal rising, falling edge	E,R/W,A0, D7 ~ D0	tr,tf			15	ns

(Vss=0V, VDD=2.2 to 2.7V, Ta=-30 to 80°C)

Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0,CS1, CS2	tAH6		0	-	ns
Address set up time		tAW6		0	-	ns
System cycle time		tcyc6		1000	-	ns
Enable "H" pulse width (Read)	E	tCCHR		240	-	ns
Enable "H" pulse width (Write)		tCCHW		120	-	ns
Enable "L" pulse width (Read)		tCCLR		120	-	ns
Enable "L" pulse width (Write)		tCCLW		120	-	ns
Data set up time	D7 ~ D0	tDS6		80	-	ns
Data hold time		tDH6		30	-	ns
RD access time		tACC6	CL=100pF	-	280	ns
Output disable time		tOH6		10	200	ns
Input signal rising, falling edge	E,R/W,A0, D7 ~ D0	tr,tf			15	ns

Note) Each timing is specified based on 0.2xVDD and 0.8xVDD.

Write characteristics (Serial interface)



(Vss=0V, VDD=4.5 to 5.5V, Ta=-30 to 80°C)

Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	tscyc		200	-	ns
SCL “H” pulse width		tSHW		75	-	ns
SCL “L” pulse width		tSLW		75	-	ns
Address set up time	A0	tSAS		50	-	ns
Address hold time		tSAH		100	-	ns
Data set up time	SI	tSDS		50	-	ns
Data hold time		tSDH		50	-	ns
CS-SCL time	CS1,CS2	tCSS		100	-	ns
		tCSH		100	-	ns
Rising, falling edge	SCL,A0, CS1,CS2,SI	tr,tf			15	ns

(Vss=0V, VDD=2.7 to 4.5V, Ta=-30 to 80°C)

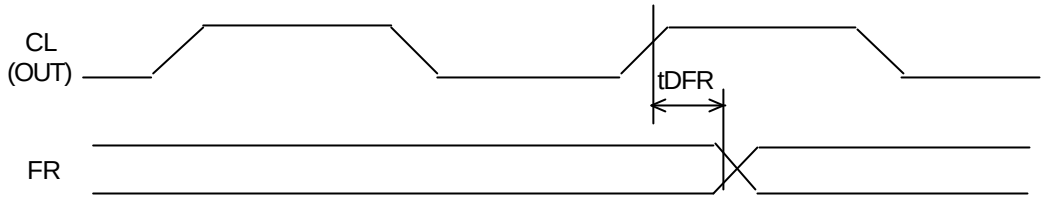
Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	tscyc		250	-	ns
SCL "H" pulse width		tSHW		100	-	ns
SCL "L" pulse width		tSLW		100	-	ns
Address set up time	A0	tSAS		150	-	ns
Address hold time		tSAH		150	-	ns
Data set up time	SI	tSDS		100	-	ns
Data hold time		tSDH		100	-	ns
CS-SCL time	CS1,CS2	tCSS		150	-	ns
		tCSH		150	-	ns
Rising, falling edge	SCL,A0, CS1,CS2,SI	tr,tf			15	ns

(Vss=0V, VDD=2.2 to 2.7V, Ta=-30 to 80°C)

Parameter	Terminal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	tscyc		400	-	ns
SCL "H" pulse width		tSHW		150	-	ns
SCL "L" pulse width		tSLW		150	-	ns
Address set up time	A0	tSAS		250	-	ns
Address hold time		tSAH		250	-	ns
Data set up time	SI	tSDS		150	-	ns
Data hold time		tSDH		150	-	ns
CS-SCL time	CS1,CS2	tCSS		250	-	ns
		tCSH		250	-	ns
Rising, falling edge	SCL,A0, CS1,CS2,SI	tr,tf			15	ns

Note) Each timing is specified based on 0.2xVDD and 0.8xVDD.

Display control timing characteristics



(V_{SS}=0V, V_{DD}=4.5~5.5V, Ta=-30~80°C)

Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR Delay Time	FR	t_{DFR}	CL=50pF	-	10	40	ns

(V_{SS}=0V, V_{DD}=2.7~4.5V, Ta=-30~80°C)

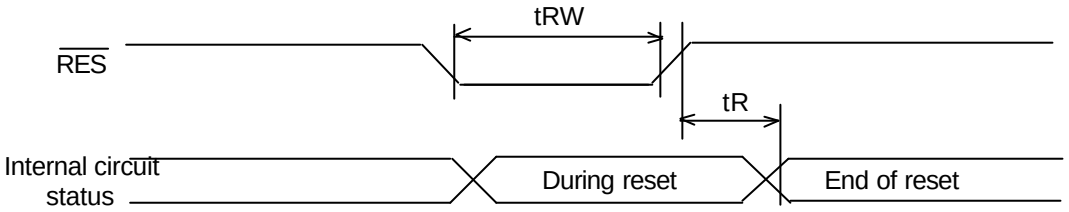
Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR Delay Time	FR	t_{DFR}	CL=50pF	-	10	80	ns

(V_{SS}=0V, V_{DD}=2.2~2.7V, Ta=-30~80°C)

Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR Delay Time	FR	t_{DFR}	CL=50pF	-	50	200	ns

Note) Each timing is specified based on 0.2xVDD and 0.8xVDD.
Note) The delay time is applied to the master operation only.

Reset input timing



(V_{SS}=0V, V_{DD}=4.5~5.5V, Ta=-30~80°C)

Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Time	RES	t_R		-	-	0.5	us
Reset "L" Level Pulse Width		t_{RW}		0.5	-	-	us

(V_{SS}=0V, V_{DD}=2.7~4.5V, Ta=-30~80°C)

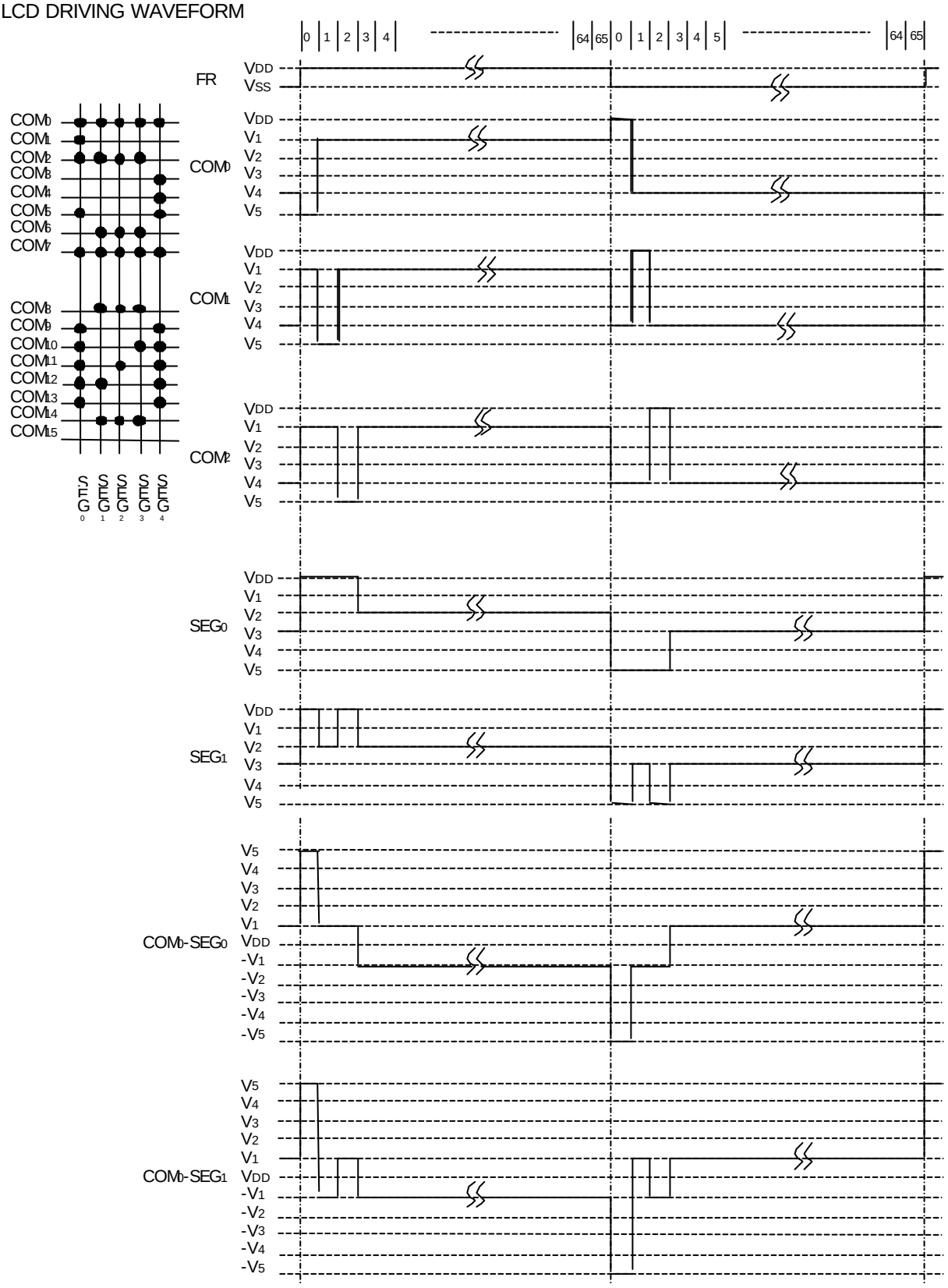
Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Time	RES	t_R		-	-	1.0	us
Reset "L" Level Pulse Width		t_{RW}		1.0	-	-	us

(V_{SS}=0V, V_{DD}=2.2~2.7V, Ta=-30~80°C)

Parameter	Terminal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Time	RES	t_R		-	-	1.5	us
Reset "L" Level Pulse Width		t_{RW}		1.5	-	-	us

Note) Each timing is specified based on 0.2xVDD and 0.8xVDD.

■ LCD DRIVING WAVEFORM



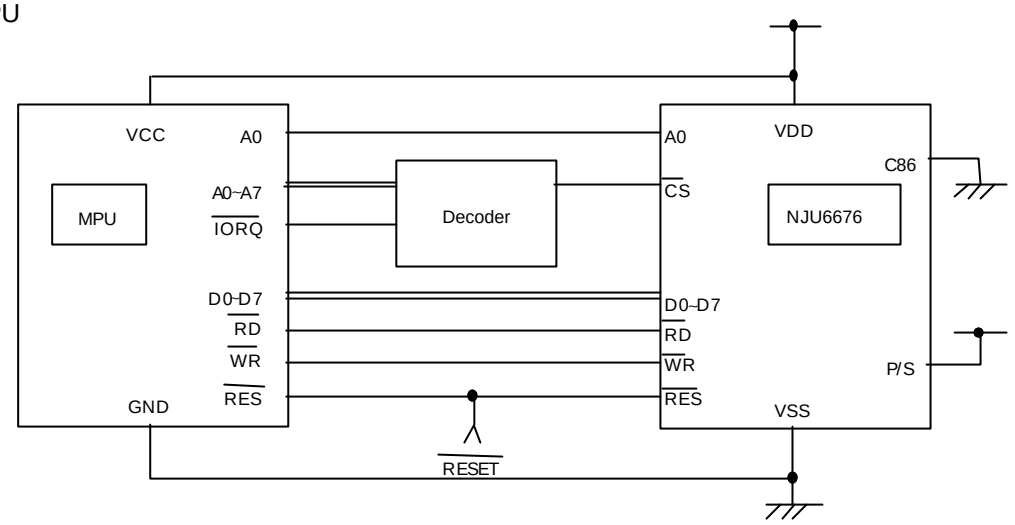
■APPLICATION CIRCUIT

- Microprocessor Interface Example

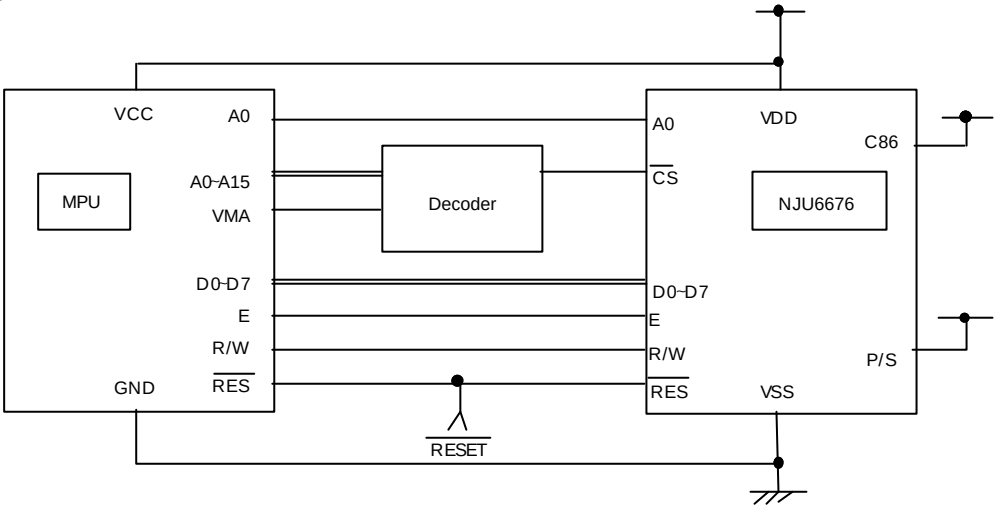
The NJU6676 interfaces to 80 type or 68 type MPU directly.
And the serial interface also communicates with MPU.

* : C86 terminal must be fixed VDD or VSS.

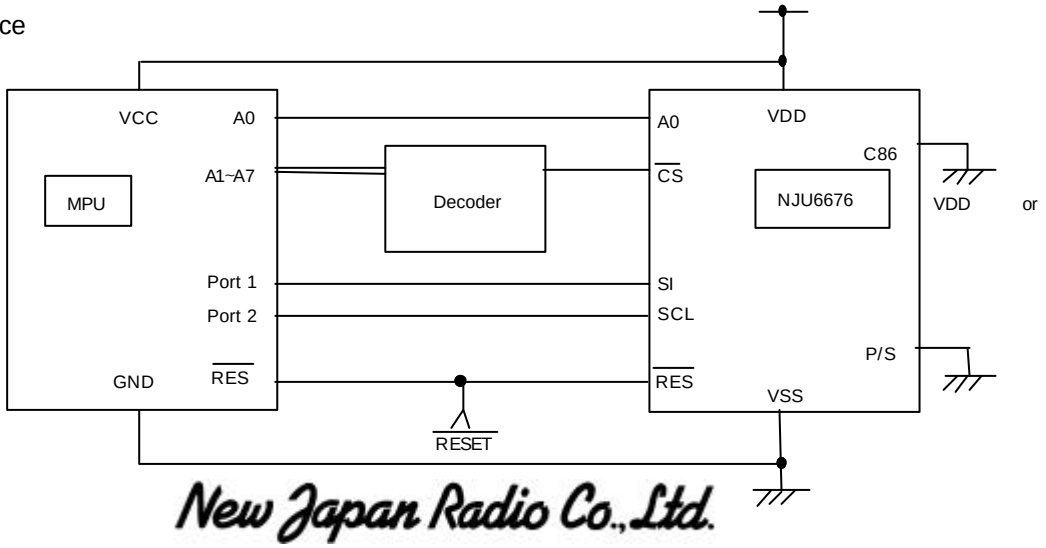
● 80 Type MPU



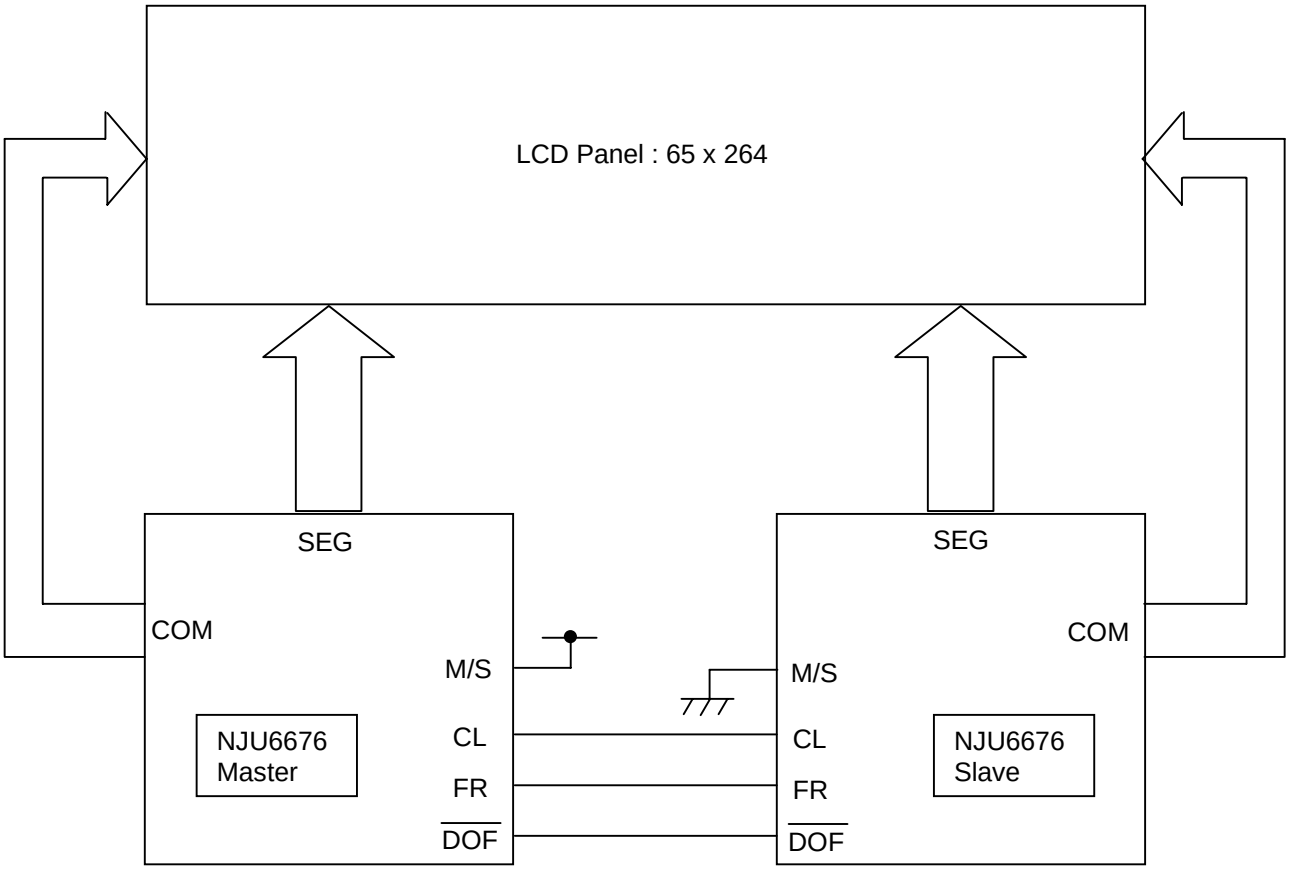
● 68 Type MPU



● Serial Interface



- 65 x 264 dots Driving Application Circuits Example
  (Common and Segment Drivers Extension by using two of NJU6676)



[CAUTION]
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