PJP24N10 / PJF24N10

100V N-Channel Enhancement Mode MOSFET

FEATURES

- $R_{DS(ON)}$, V_{GS}@10V,I_{DS}@30A=24mΩ
- Low On Resistance
- Excellent Gate Charge x $R_{DS(ON)}$ Product (FOM)
- Fully Characterized Avalanche Voltage and Current
- Specially Designed for AC Adapter, High-Frequency Switch and Synchronous Rectification
- Component are in compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

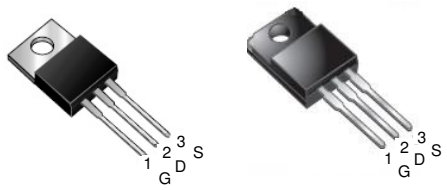
- Case: TO-220AB / ITO-220AB Molded Plastic
- Terminals : Solderable per MIL-STD-750,Method 2026

ORDERING INFORMATION

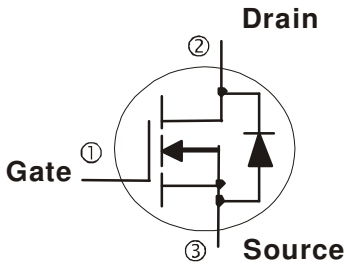
TYPE	MARKING	PACKAGE	PACKING
PJP24N10	P24N10	TO-220AB	50PCS/TUBE
PJF24N10	F24N10	ITO-220AB	50PCS/TUBE

TO-220AB / ITO-220AB

TO-220AB ITO-220AB



INTERNAL SCHEMATIC DIAGRAM



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	Symbol	PJP24N10	PJF24N10	Units
Drain-Source Voltage	V_{DS}	100		V
Gate-Source Voltage	V_{GS}	±20		V
Continuous Drain Current	I_D	42	42	A
Pulsed Drain Current [1]	I_{DM}	160	160	A
Maximum Power Dissipation T_A=25°C Derating Factor	P_D	89 0.71	32 0.42	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 to +150		°C
Avalanche Energy with Single Pulse I_{AS}=17A, VDD=80V, L=4.7mH	E_{AS}	680		mJ
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	1.4	3.8	°C/W
Junction-to Ambient Thermal Resistance	$R_{\theta JA}$	62.5	100	°C/W

Note: 1. Maximum DC current limited by the package

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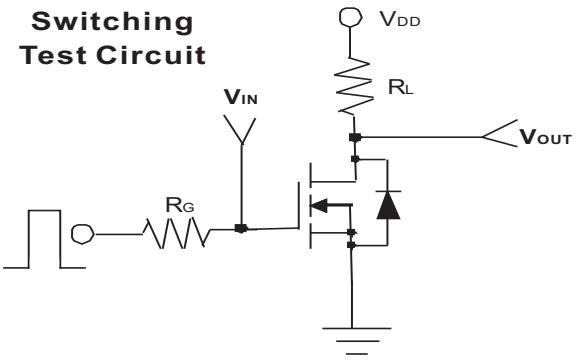
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

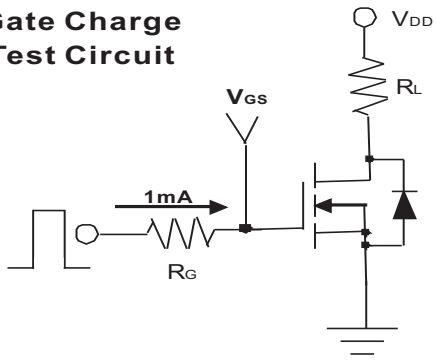
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	2.0	-	4.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}= 10V, I_D= 30A	-	18.6	24	mΩ
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	-	-	1	uA
Gate Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V, I_D=30A, V_{GS}=10V	-	60.6	78	nC
Gate-Source Charge	Q_{gs}		-	8.2	-	
Gate-Drain Charge	Q_{gd}		-	21.4	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=1A V_{GS}=10V, R_G=1.6Ω	-	18.4	26	ns
Turn-On Rise Time	t_r		-	9.2	12	
Turn-Off Delay Time	$t_{d(off)}$		-	56	68	
Turn-Off Fall Time	t_f		-	18.8	26	
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V f=1.0MHz	-	1450	3200	pF
Output Capacitance	C_{oss}		-	155	200	
Reverse Transfer Capacitance	C_{rss}		-	110	165	
Source-Drain Diode						
Max. Diode Forward Current	I_S	-	-	-	42	A
Diode Forward Voltage	V_{SD}	I_S=30A , V_{GS}=0V	-	-	1.3	V

NOTE: Plus Test : Pluse Width ≤ 300us, Duty Cycle ≤ 2%.

Switching Test Circuit



Gate Charge Test Circuit



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Typical Characteristics Curves (Ta=25℃, unless otherwise noted)

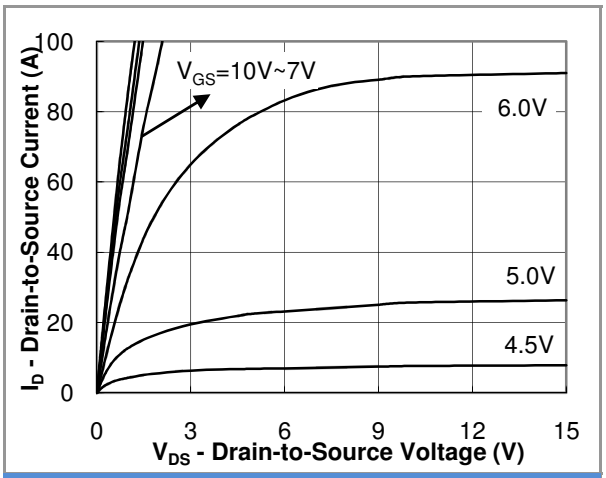

Fig.1 Output Characteristic

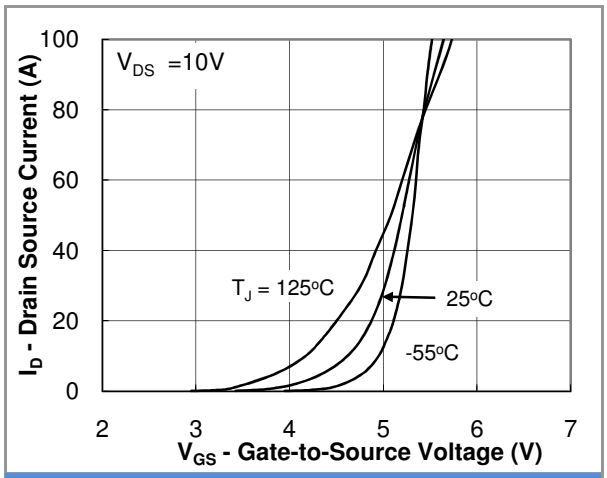

Fig.2 Transfer Characteristic

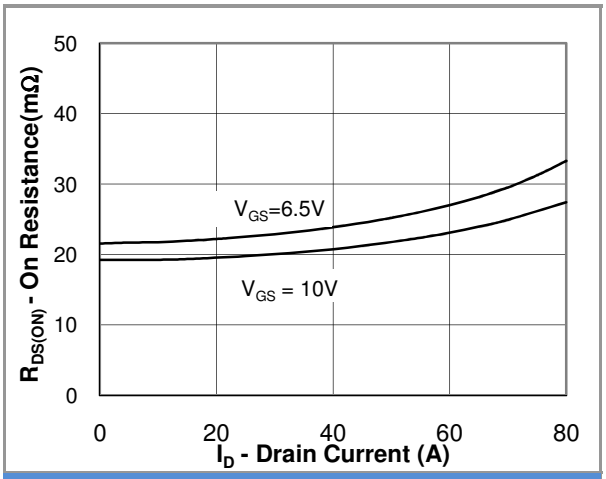

Fig.3 On Resistance vs Drain Current

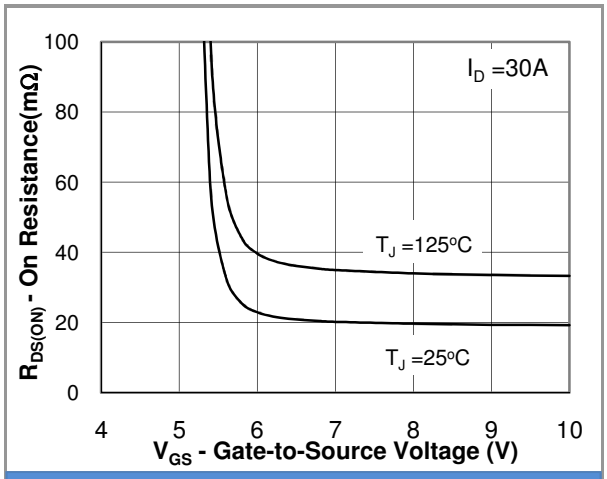

Fig.4 On Resistance vs Gate to Source Voltage

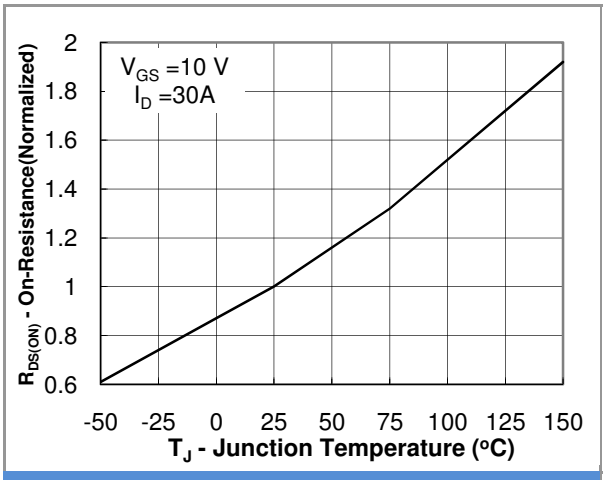

Fig.5 On Resistance vs Junction Temperature

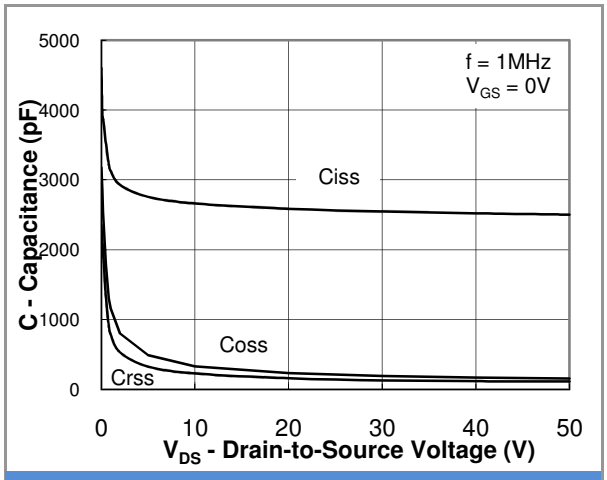

Fig.6 Capacitance

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Typical Characteristics Curves (Ta=25℃, unless otherwise noted)

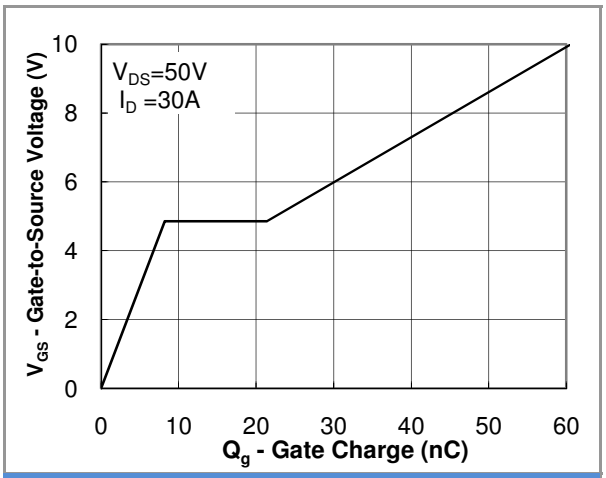

Fig. 7 Gate Charge Waveform

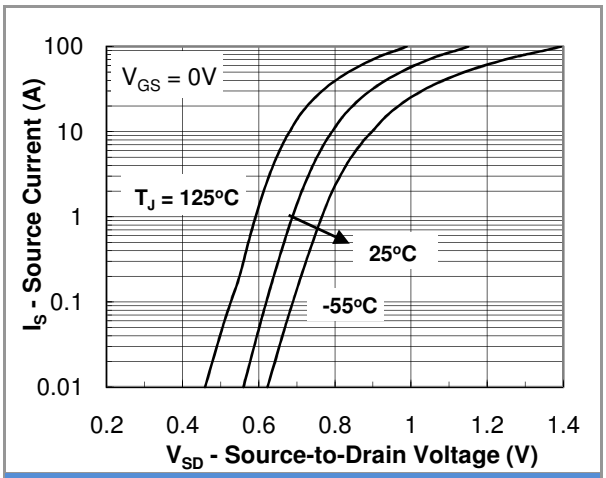

Fig.8 Source-Drain Diode Forward Voltage

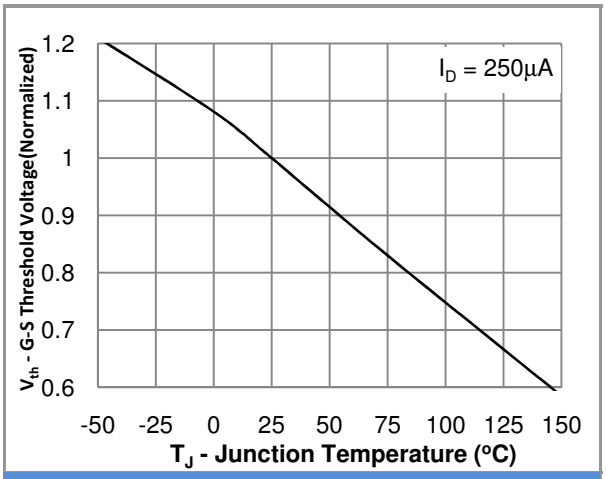

Fig.9 Breakdown Voltage vs Junction Temperature

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LEGAL STATEMENT