e2v technologies

# CCD201-20 Back Illuminated 2-Phase IMO Series Electron Multiplying CCD Sensor

## INTRODUCTION

The CCD201 is a large format sensor ($>1k^2$) in the L3Vision™ range of products from e2v technologies. This device uses a novel output amplifier circuit that is capable of operating at an equivalent output noise of less than one electron at pixel rates of over 15 MHz. This makes the sensor well suited for scientific imaging where the illumination is limited.

The sensor is a frame transfer device and can operate in inverted mode to suppress dark current as this is now the dominant noise source (even at high readout rate). The image and store sections are designed to operate in 2-phase mode, to maximise the highest achievable parallel transfer frequency.

The sensor functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register before conversion to a voltage by an output amplifier.

The sensor has two output amplifiers; a low noise, high responsivity output for normal CCD operation and a large signal amplifier for when multiplication gain is employed.

Operation of the high gain mode is controlled by adjustment of the multiplication phase amplitude R∅2HV.

## GENERAL DATA

| | |
|---|---|
| Active image area | 13.3 x 13.3 mm |
| Image section active pixels | 1024 (H) x 1024 (V) |
| Image pixel size | 13 x 13 µm |
| Number of output amplifiers | 2 |
| Fill factor | 100% |
| Additional dark reference columns | 32 |
| Additional overscan rows | 8 |

## PACKAGE DETAILS (see Fig. 15)

### Ceramic Package

| | |
|---|---|
| Overall dimensions | 37.4 x 26.5 mm |
| Number of pins | 36 |
| Inter-pin spacing | 2.54 mm |
| Mounting position | any |

The pin 1 marker is shown in Fig. 15.

## STORAGE AND OPERATION TEMPERATURE EXTREMES

| | MIN | MAX |
|---|---|---|
| Storage temperature (°C) | −200 | +100 |
| Operating temperature (°C) | −120 | +75 |
| Temperature ramping (°C/min) | - | 5 |

**Note:** Operation or storage in humid conditions may give rise to moisture on the sensor surface on cooling, causing irreversible damage.



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## TYPICAL PERFORMANCE SPECIFICATIONS

Except where otherwise specified, the following are measured for operation at a pixel rate of 15 MHz, with typical operating voltages. Parameters are given at 223 K unless specified otherwise. Where parameters are different in the normal and high gain mode, both are given.

| PARAMETER | UNIT | MIN | TYPICAL | MAX |
|---|---|---|---|---|
| Output amplifier responsivity, HR amplifier (normal mode) (see note 1) | $\mu V/e^-$ | - | 5.3 | - |
| Output amplifier responsivity, LS amplifier (normal mode) (see note 1) | $\mu V/e^-$ | - | 1.4 | - |
| Multiplication register gain, LS amplifier (high gain mode) (see notes 2, 3 and 4) | | 1 | - | 1000 |
| Peak signal - 2-phase IMO | $e^-$/pixel | 50k | 80k | - |
| Charge handling capacity of multiplication register (see note 5) | $e^-$/pixel | - | 730k | - |
| Charge handling capacity of HR amplifier (see note 6) | $e^-$ | - | 280k | - |
| Charge handling capacity of LS amplifier (see note 6) | $e^-$ | - | 1M | - |
| Readout noise at 50 kHz with CDS, HR amplifier (normal mode) (see note 6) | $e^-$ rms | - | 3.1 | - |
| Readout noise at 1 MHz with CDS, HR amplifier (normal mode) (see note 6) | $e^-$ rms | - | 6.0 | - |
| Amplifier reset noise (without CDS), HR amplifier (normal mode) (see note 6) | $e^-$ rms | - | 50 | - |
| Readout noise at 15 MHz with CDS, LS amplifier (normal mode) (see note 6) | $e^-$ rms | - | 43 | - |
| Amplifier reset noise (without CDS), LS amplifier (normal mode) (see note 6) | $e^-$ rms | - | 100 | - |
| Readout noise at 1 MHz (high gain mode) (see note 6) | $e^-$ rms | - | $<1$ | - |
| Maximum frequency (settling to 1%), HR amplifier (see notes 6 and 7) | MHz | - | - | 3 |
| Maximum frequency (settling to 5%), HR amplifier (see notes 6 and 7) | MHz | - | - | 4.5 |
| Maximum frequency (settling to 1%), LS amplifier (see note 6 and 7) | MHz | - | - | 13 |
| Maximum frequency (settling to 5%), LS amplifier (see note 6 and 7) | MHz | - | - | 20 |
| Maximum parallel transfer frequency (see note 1) | MHz | - | 0.9 | - |
| Dark signal at 293 K (see note 8) | $e^-$/pixel/s | - | 260 | 530 |
| Dark signal non-uniformity (DSNU) at 293 K (see note 9) | $e^-$/pixel/s | - | 90 | - |
| Excess noise factor (see note 10) | | - | $\sqrt{2}$ | - |



## NOTES

1. Measured at a pixel rate of 1 MHz.
2. The typical variation of gain with R∅2HV is shown in Fig. 1.
3. The variation of gain with R∅2HV at different temperatures is shown in Fig. 1.
4. Some increase of R∅2HV may be required throughout life to maintain gain performance. Adjustment of R∅2HV should be limited to the maximum specified under Operating Conditions.
5. When multiplication gain is used and clock timings optimised, a linear response of output signal with input signal of better than 3% is achieved for output signals up to 400 $ke^-$ typically.
6. These values are inferred by design and not measured.
7. The quoted maximum frequencies assume a 20 pF load and that correlated double sampling is being implemented.
8. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a component generated during readout through the register. Operating at a temperature of 293 K and 10 Hz frame rate, the readout component contributes 5.8 $e^-$/pixel/frame typically, at a gain of 1000 and referenced to the image area, and has a temperature dependence consistent with non-inverted mode operation.

   There exists a further weakly temperature dependent component, the clock induced charge, which is independent of the integration time. The clock induced charge is dependent on the operating biases and timings employed and is typically 0.2 $e^-$/pixel/frame at $T = -55\ ^\circ C$.

   For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".
9. DSNU is defined as the $1\sigma$ variation of the dark signal.
10. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

## DEVICE COSMETIC PERFORMANCE

Grade 1 devices are supplied to the blemish specification shown below.

Note that incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

### Test Conditions

| | |
|---|---|
| Operating mode | Devices run in 2-phase inverted mode, with an integration time of 100 ms and a readout rate of 15 MHz. |
| Sensor temperature | 18 $\pm$ 3 °C. |
| Multiplication gain | Set to approximately 1000. |
| Illumination | Set to give a signal level of approximately 60 $e^-$/pixel/frame. |

## BLEMISH SPECIFICATION

**Black Columns** Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A black column contains at least 9 contiguous black defects.

**White Columns** White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum specified dark signal level. A white column contains at least 9 contiguous white defects.

**Pin-Head Columns** Pin-head columns are manifest as a partial dark column with a bright pixel showing photoresponse at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 contiguous black defects.

## SPECIFICATION

| PARAMETER | GRADE 1 SPECIFICATION | GRADE 2 SPECIFICATION |
|---|---|---|
| White Columns | 0 | 0 |
| Black /Pin-head Columns | 1 | 6 |

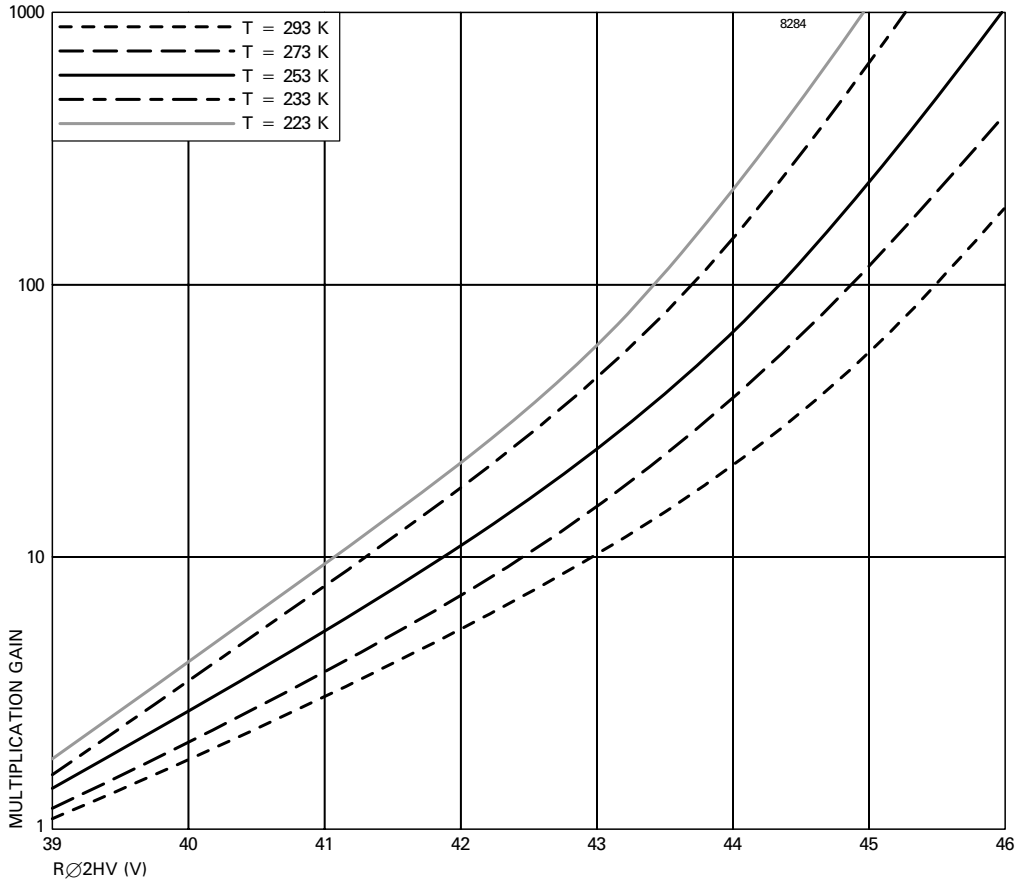
## ORDERING INFORMATION

| PART NUMBER | OPERATING MODE | COATING | WINDOW |
|---|---|---|---|
| CCD201-20-*- 122 | 2-phase | Midband | Temporary |



* denotes grade of device.

## Figure 1: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH R∅2HV AT DIFFERENT TEMPERATURES




## Figure 2: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

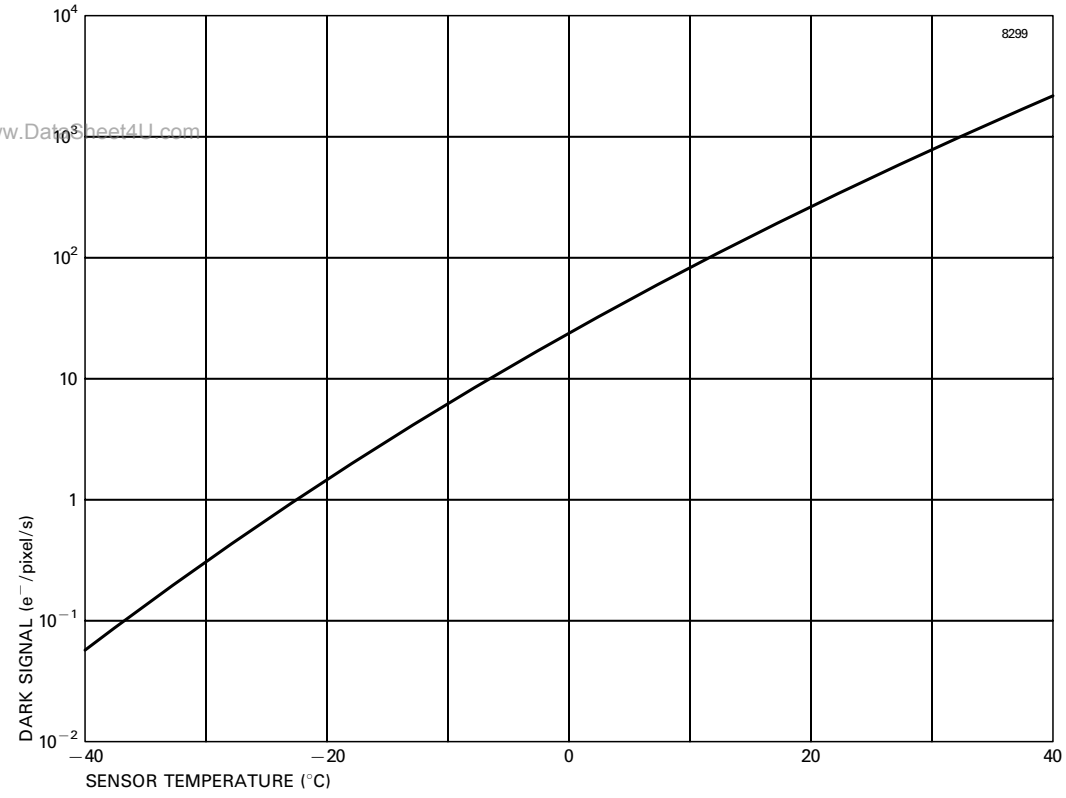
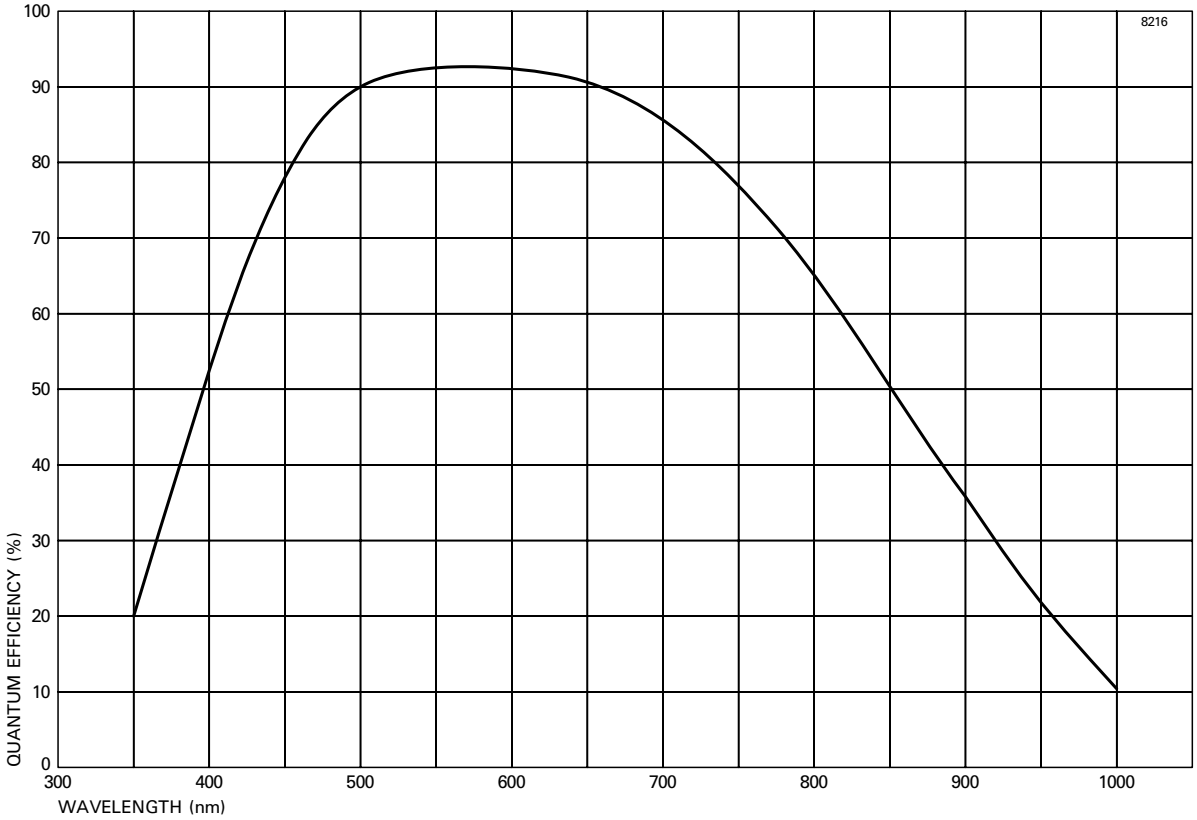


**Figure 3: TYPICAL SPECTRAL RESPONSE (At −20 °C, no window, midband coating)**






## ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

## EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

## ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to SS.

| PIN | CONNECTION | DESCRIPTION | MIN (V) | MAX (V) |
|---|---|---|---|---|
| 1 | ABD | Anti-blooming Drain (see note 11) | −0.3 | +25 |
| 2 | SS | Substrate | 0 | |
| 3 | IØ4 | Image Clock 4 | −20 | +20 |
| 4 | IØ3 | Image Clock 3 | −20 | +20 |
| 5 | SØ4 | Store Clock 4 | −20 | +20 |
| 6 | SØ2 | Store Clock 2 | −20 | +20 |
| 7 | SS | Substrate | 0 | |
| 8 | SS | Substrate | 0 | |
| 9 | DG | Dump Gate | −20 | +20 |
| 10 | OG | Output Gate | −20 | +20 |
| 11 | ODH | Output Drain (HR Amplifier) | −0.3 | +32 |
| 12 | RD | Reset Drain | −0.3 | +25 |
| 13 | ODL | Output Drain (LS Amplifier) | −0.3 | +32 |
| 14 | SS | Substrate | 0 | |
| 15 | OSH | Output Source (HR Amplifier) (see note 12) | −0.3 | +25 |
| 16 | OSL | Output Source (LS Amplifier) (see note 12) | −0.3 | +25 |
| 17 | ØR | Reset Pulse | −20 | +20 |
| 18 | RØDC | Multiplication Register DC Bias | −20 | +20 |
| 19 | RØ2HV | Multiplication Register Clock | −20 | +50 |
| 20 | DG | Dump Gate | −20 | +20 |
| 21 | n.c. | Not Connected | | |
| 22 | n.c. | Not Connected | | |
| 23 | SS | Substrate | 0 | |
| 24 | n.c. | Not Connected | | |
| 25 | n.c. | Not Connected | | |
| 26 | DD | Dump Drain | −0.3 | +25 |
| 27 | RØ3 | Register Clock 3 | −20 | +20 |
| 28 | RØ1 | Register Clock 1 | −20 | +20 |
| 29 | RØ2 | Register Clock 2 | −20 | +20 |
| 30 | SS | Substrate | 0 | |
| 31 | SØ3 | Store Clock 3 | −20 | +20 |
| 32 | SØ1 | Store Clock 1 | −20 | +20 |
| 33 | IØ1 | Image Clock 1 | −20 | +20 |
| 34 | IØ2 | Image Clock 2 | −20 | +20 |
| 35 | SS | Substrate | 0 | |
| 36 | IG | Isolation Gate | −20 | +20 |



## NOTES

11. Anti-blooming is not available on this device type. However, ABD is used for connection purposes and must be biased as specified.
12. Permanent damage may result if, in operation, OSL or OSH experience short-circuit conditions.

### Maximum voltages between pairs of pins:

| PIN | CONNECTION | PIN | CONNECTION | MIN (V) | MAX (V) |
|---|---|---|---|---|---|
| 15 | OSH | 11 | ODH | −15 | +15 |
| 16 | OSL | 13 | ODL | −15 | +15 |
| 19 | RØ2HV | 18 | RØDC | −20 | +50 |
| 19 | RØ2HV | 27 | RØ3 | −20 | +50 |
| Output transistor current (mA) | | | | | 20 |

## OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

| CONNECTION | PULSE AMPLITUDE OR DC LEVEL (V) | | |
|---|---|---|---|
| | Min | Typical | Max |
| IØ1,2,3,4 high | +5 (see note 13) | +7 | +9 (see note 13) |
| IØ1,2,3,4 low | −6 | −5 | −4 |
| SØ1,2,3,4 high | +5 (see note 13) | +7 | +9 (see note 13) |
| SØ1,2,3,4 low | −6 | −5 | −4 |
| RØ1,2,3 high | +8 | +12 | +13 |
| RØ1,2,3 low | - | 0 | - |
| RØ2HV high | +20 | +40 | +50 (see note 4) |
| RØ2HV low | 0 | +4 | +5 |
| ØR high | see note 14 | +10 | see note 14 |
| ØR low | - | 0 | - |
| RØDC | +2 | +3 | +5 |
| OG | +1 | +3 | +5 |
| IG | - | −5 | - |
| SS | 0 | +4.5 | +7 |
| ODL, ODH | +25 | +28 | +32 |
| RD | +15 | +17 | +20 |
| ABD | +10 | +18 | +20 |
| DG low | - | 0 | - |
| DG high | +10 | +12 | +13 |
| DD | +20 | +24 | +25 |



## NOTES

13. IØ and SØ adjustment may be common.
14. ØR high level may be adjusted in common with RØ1,2,3.
15. Between the two amplifiers, common connections are made to the reset gates (ØR), reset drains (RD) and output gates (OG).
16. An external load is required for each output amplifier. For the HR amplifier, this can be a resistor of about 5 kΩ (non-critical) or a constant current type of about 5 mA. For the LS amplifier, the load should be either 3.3 kΩ or 7.5 mA. The on-chip amplifier power dissipation is approximately 30 mW for the HR amplifier and 50 mW for the LS amplifier.

## DRIVE PULSE WAVEFORM SPECIFICATION

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases ∅1 and ∅2, and phases ∅3 and ∅4 of the image and store sections. Suggested timing diagrams are shown in Figs. 4 - 11. The following are suggested pulse rise and fall times.

| CLOCK PULSE | TYPICAL RISE TIME τ (ns) | TYPICAL FALL TIME τ (ns) | TYPICAL PULSE OVERLAP |
|---|---|---|---|
| I∅ | 140 < τ < 200 | 140 < τ < 200 | @90% points |
| S∅ | 140 < τ < 200 | 140 < τ < 200 | @90% points |
| R∅1 | 10 | 10 | @70% points |
| R∅2 | 10 | 10 | @70% points |
| R∅3 | 10 | 10 | @70% points |
| R∅2HV | 25 | 25 | see note 18 |
| R∅2HV | Sine | Sine | Sinusoid- high on falling edge of R∅1 |

## NOTES

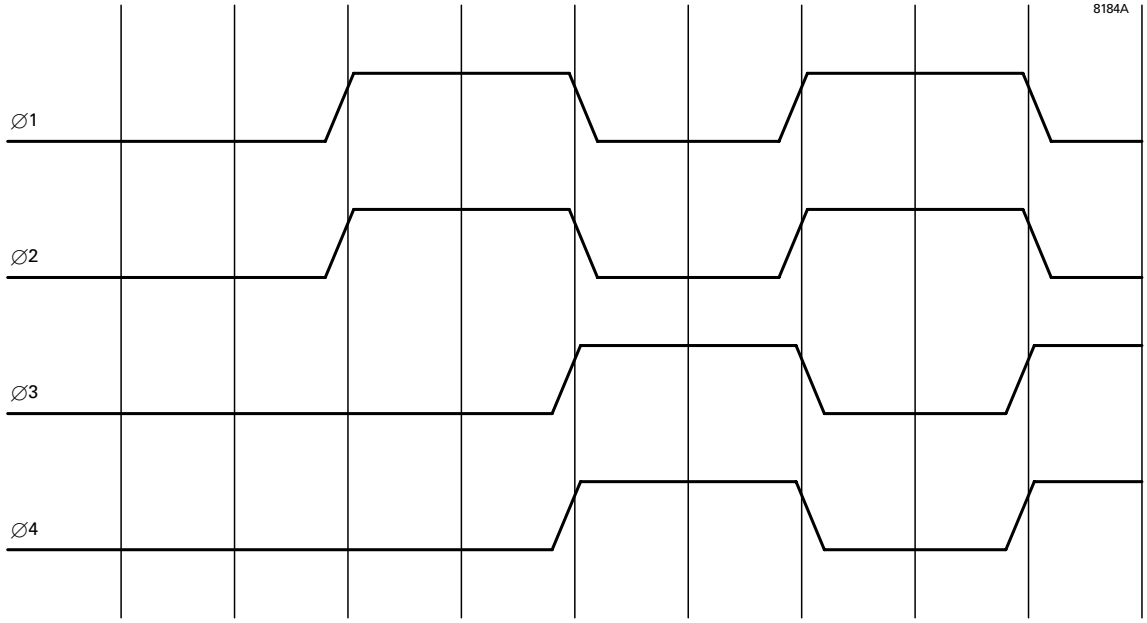
17. Register clock pulses are as shown in Figs. 5 and 6.
18. An example clocking scheme is shown in Fig. 5. R∅2HV can also be operated with a normal clock pulse, as shown in Fig. 6. The requirement for successful clocking is that R∅2HV reaches its maximum amplitude before R∅1 goes low.

## ELECTRICAL INTERFACE CHARACTERISTICS

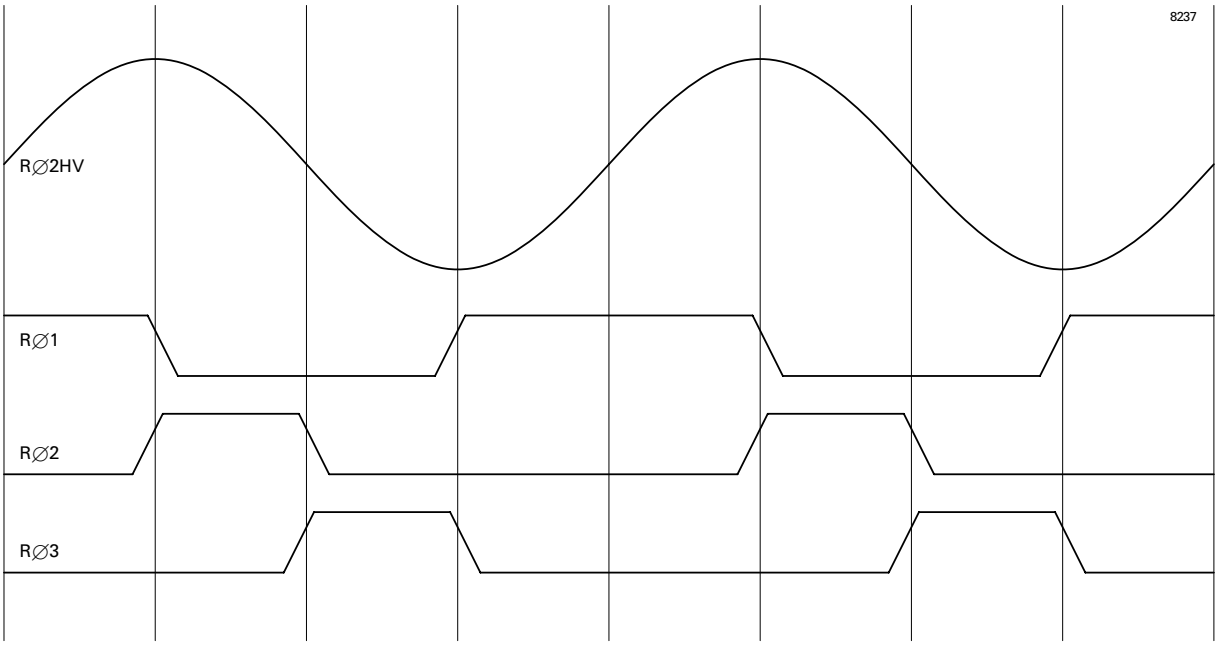
| ELECTRODE CAPACITANCES AT MID CLOCK LEVELS | | | | |
|---|---|---|---|---|
| **Connection** | **Capacitance to SS** | **Inter-phase Capacitances** | **Total Capacitance** | **Units** |
| I∅1 | 2.4 | 2.4 | 7.2 | nF |
| I∅2 | 5.4 | 2.4 | 10.2 | nF |
| I∅3 | 2.4 | 2.4 | 7.2 | nF |
| I∅4 | 5.4 | 2.4 | 10.2 | nF |
| S∅1 | 2.4 | 2.4 | 7.2 | nF |
| S∅2 | 5.4 | 2.4 | 10.2 | nF |
| S∅3 | 2.4 | 2.4 | 7.2 | nF |
| S∅4 | 5.4 | 2.4 | 10.2 | nF |
| R∅1 | 68 | 98 | 166 | pF |
| R∅2 | 56 | 68 | 124 | pF |
| R∅3 | 89 | 74 | 163 | pF |
| R∅2HV | 15 | 18 | 33 | pF |
| **SERIES RESISTANCES** | | | | |
| **Connection** | **Approximate Total Series Resistance** | | | |
| I∅1 | 16 | | | Ω |
| I∅2 | 14 | | | Ω |
| I∅3 | 16 | | | Ω |
| I∅4 | 14 | | | Ω |
| S∅1 | 16 | | | Ω |
| S∅2 | 14 | | | Ω |
| S∅3 | 16 | | | Ω |
| S∅4 | 14 | | | Ω |
| R∅1 | 6 | | | Ω |
| R∅2 | 6 | | | Ω |
| R∅3 | 6 | | | Ω |
| R∅2HV | 8 | | | Ω |
| **APPROXIMATE OUTPUT IMPEDANCE** | | | | |
| Large Signal Amplifier | 350 | | | Ω |
| High Responsivity Amplifier | 400 | | | Ω |

## PULSE TIMINGS AND OVERLAPS

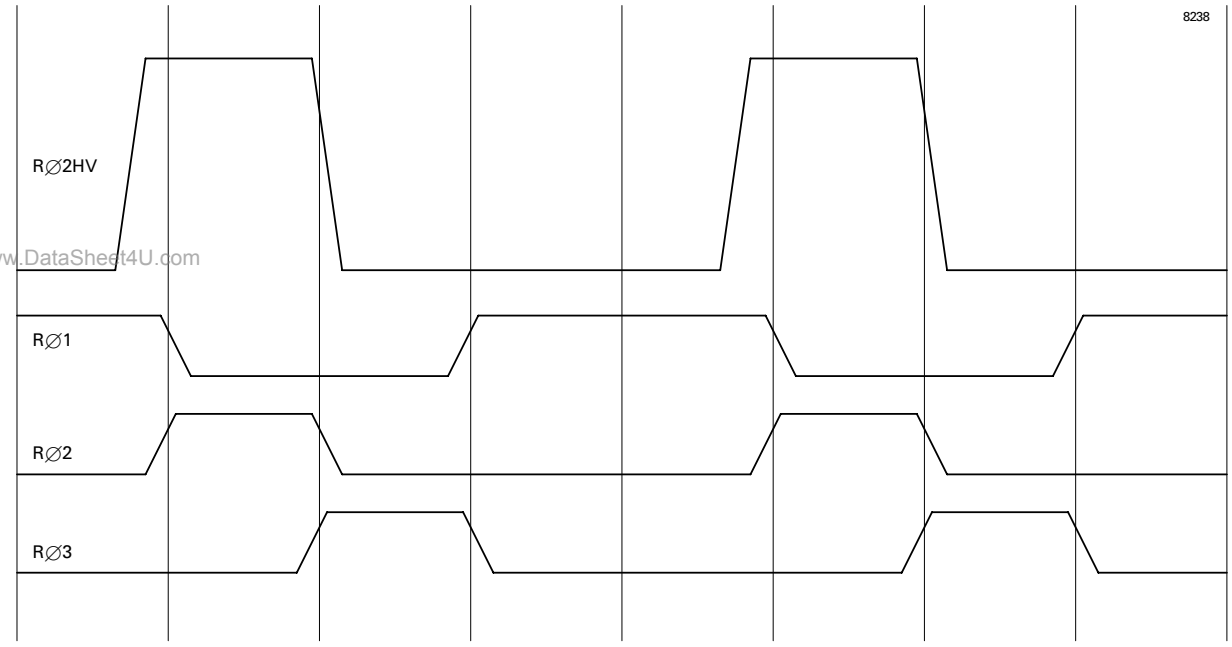
### Figure 4: CLOCKING SCHEME FOR 2-PHASE INVERTED MODE OPERATION



## Figure 5: CLOCKING SCHEME FOR MULTIPLICATION GAIN
**(Sine wave clocking scheme) (see note 19)**




## Figure 6: CLOCKING SCHEME FOR MULTIPLICATION GAIN
**(Conventional clocking scheme) (see note 19)**

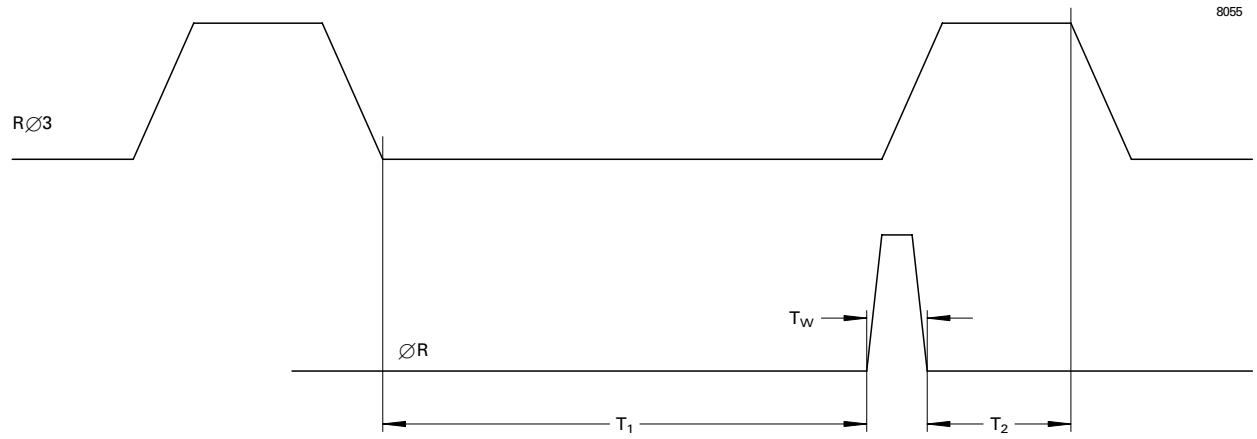





## NOTE

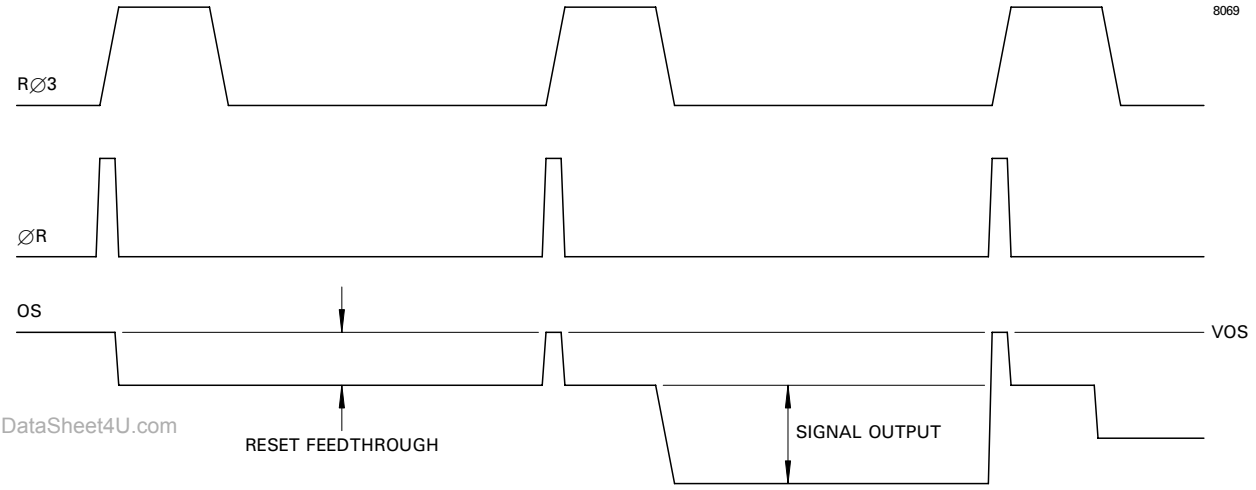
19. To operate through the OSH output amplifier, the RØ1 and RØ2 waveforms should be interchanged.

## Figure 7: RESET PULSE

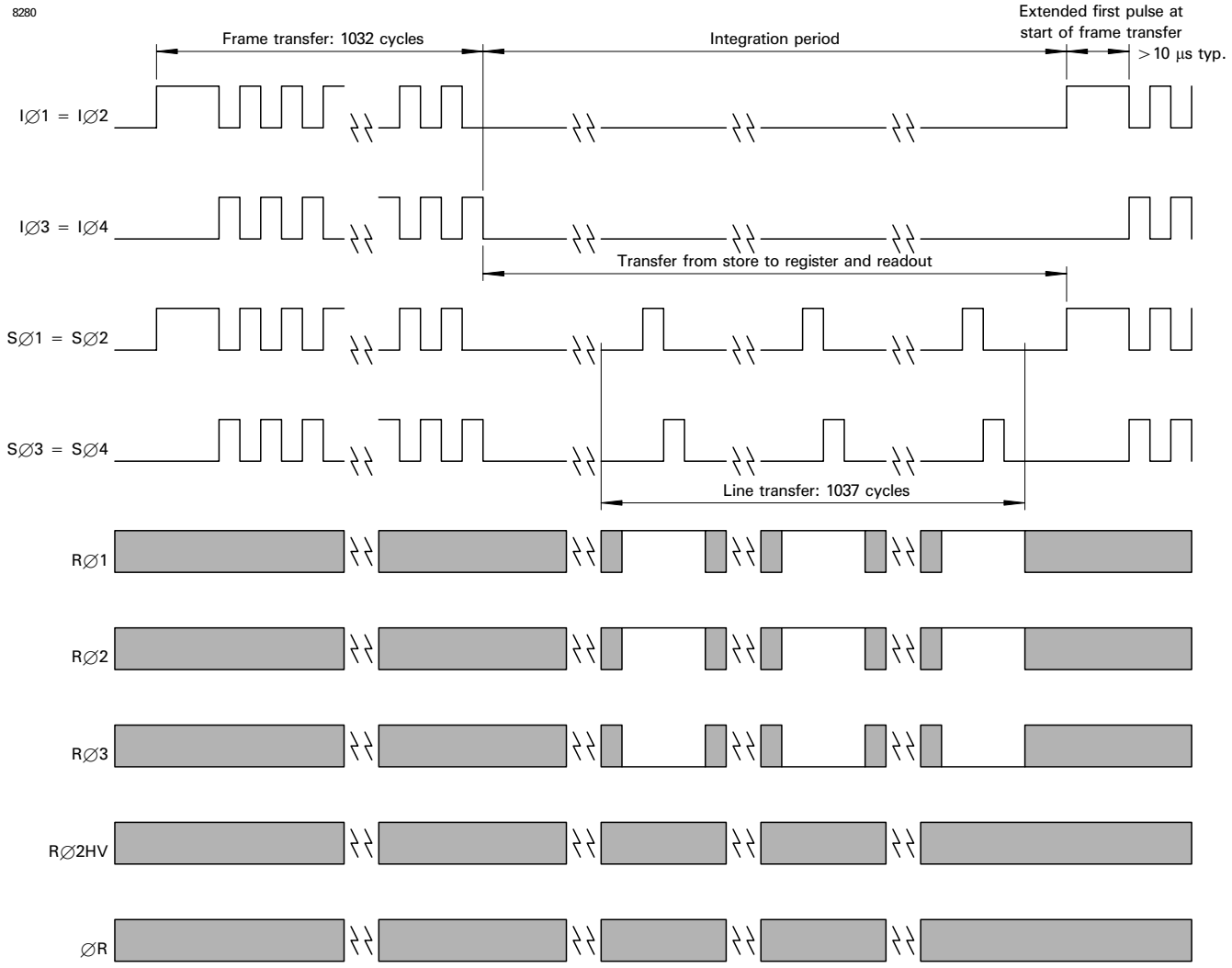



$T_W$ = 10 ns typical
$T_1$ = output valid
$T_2$ > 0 ns

## Figure 8: PULSE AND OUTPUT TIMING

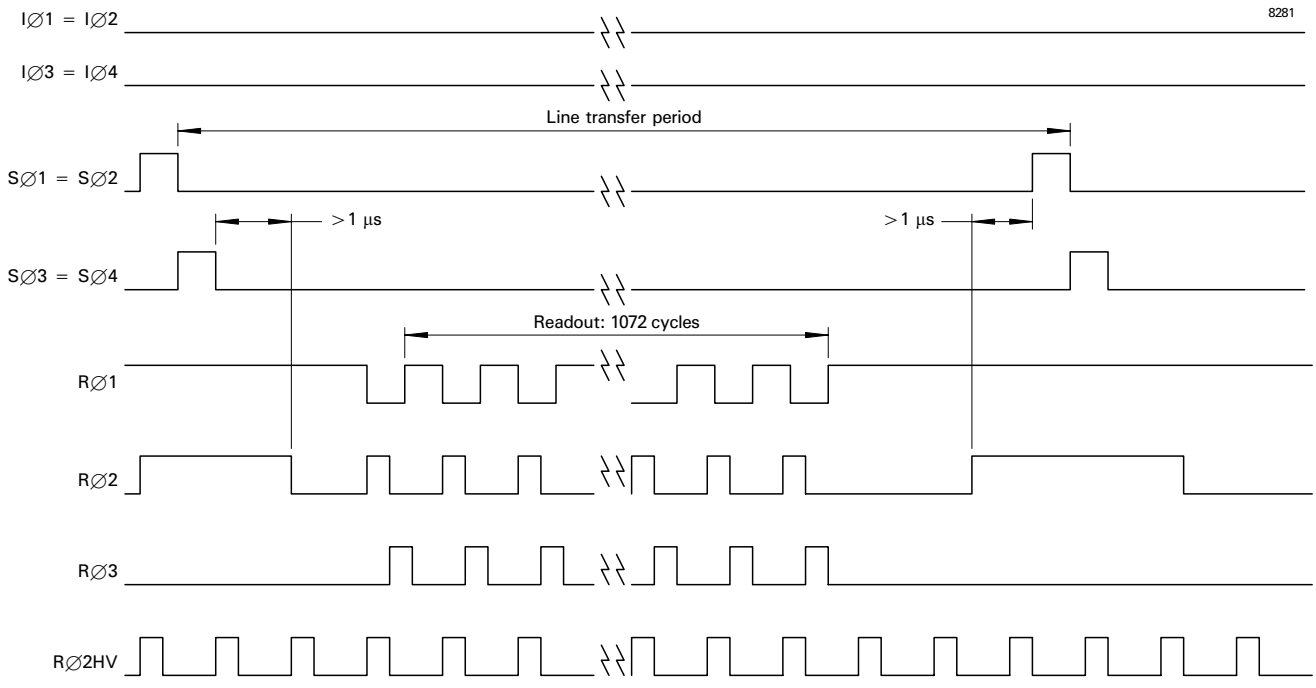


## Figure 9: EXAMPLE FRAME TIMING DIAGRAM

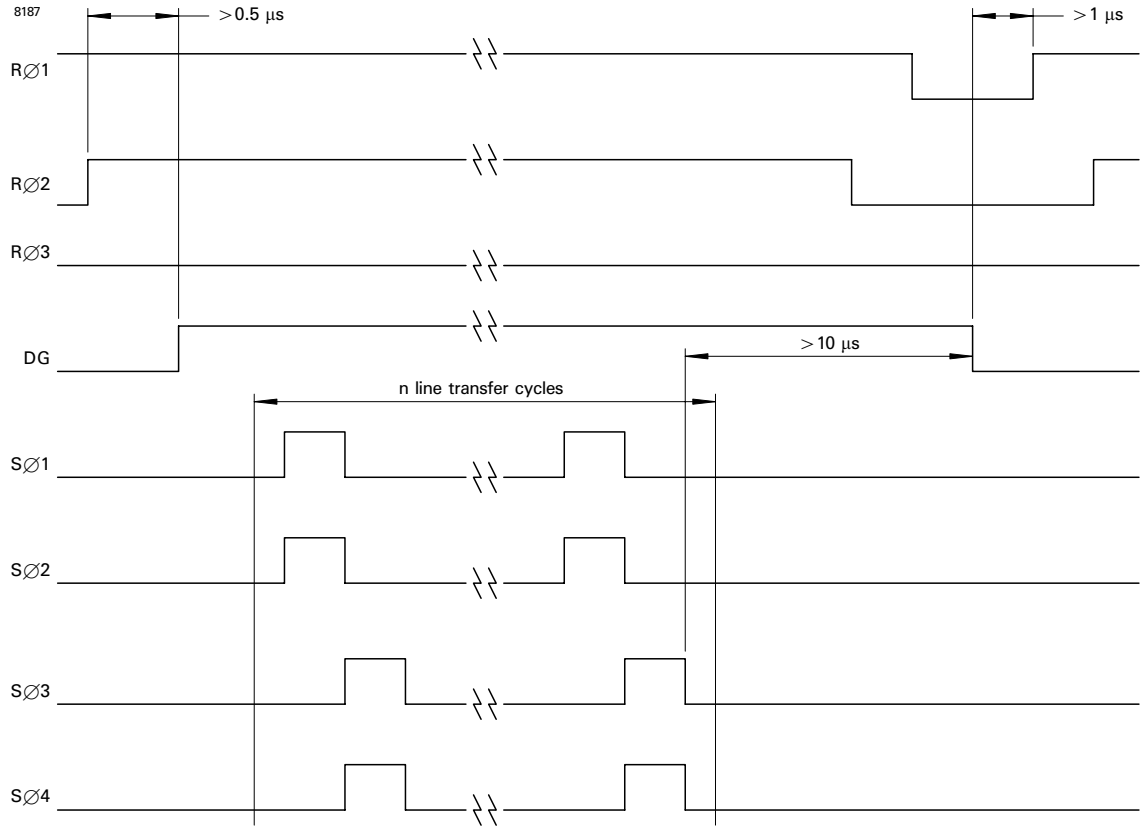



## Figure 10: EXAMPLE LINE TIMING DIAGRAM (Operation through OSL, see notes 19 and 22)





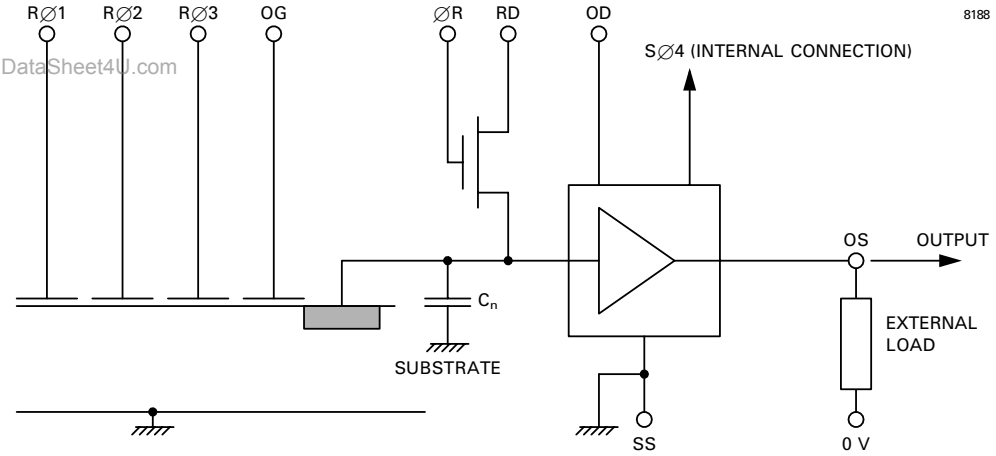
## Figure 11: OPERATION OF THE DUMP GATE TO DUMP n LINES OF UNWANTED DATA FROM THE STANDARD REGISTER




### NOTE

20. Wanted lines of data must be completely read out before dumping unwanted data.

## Figure 12: OUTPUT CIRCUIT SCHEMATIC (OSL and OSH Amplifiers)

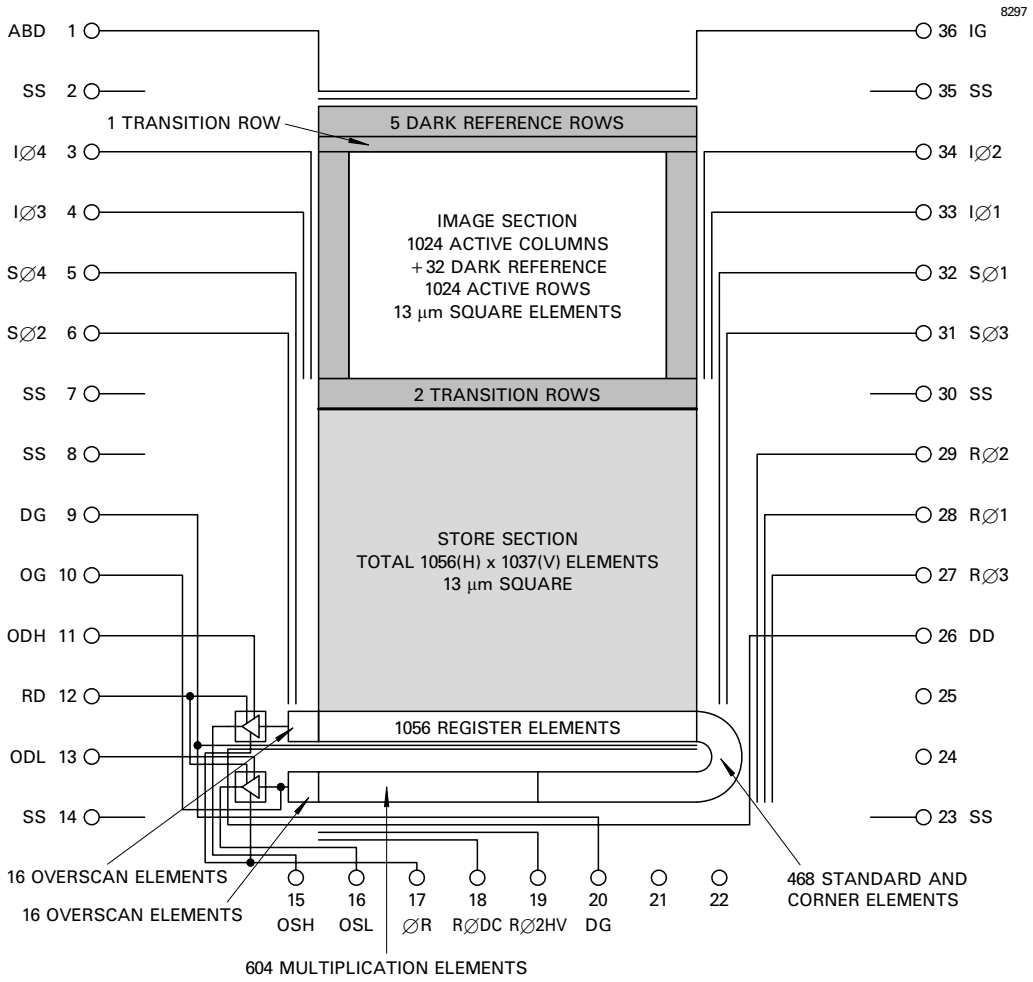





### NOTE

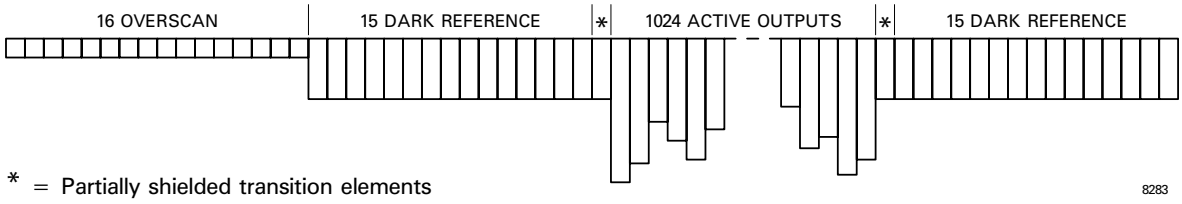
21. The amplifiers have a DC restoration circuit that is internally activated whenever SØ4 is high.

## Figure 13: SCHEMATIC CHIP DIAGRAM





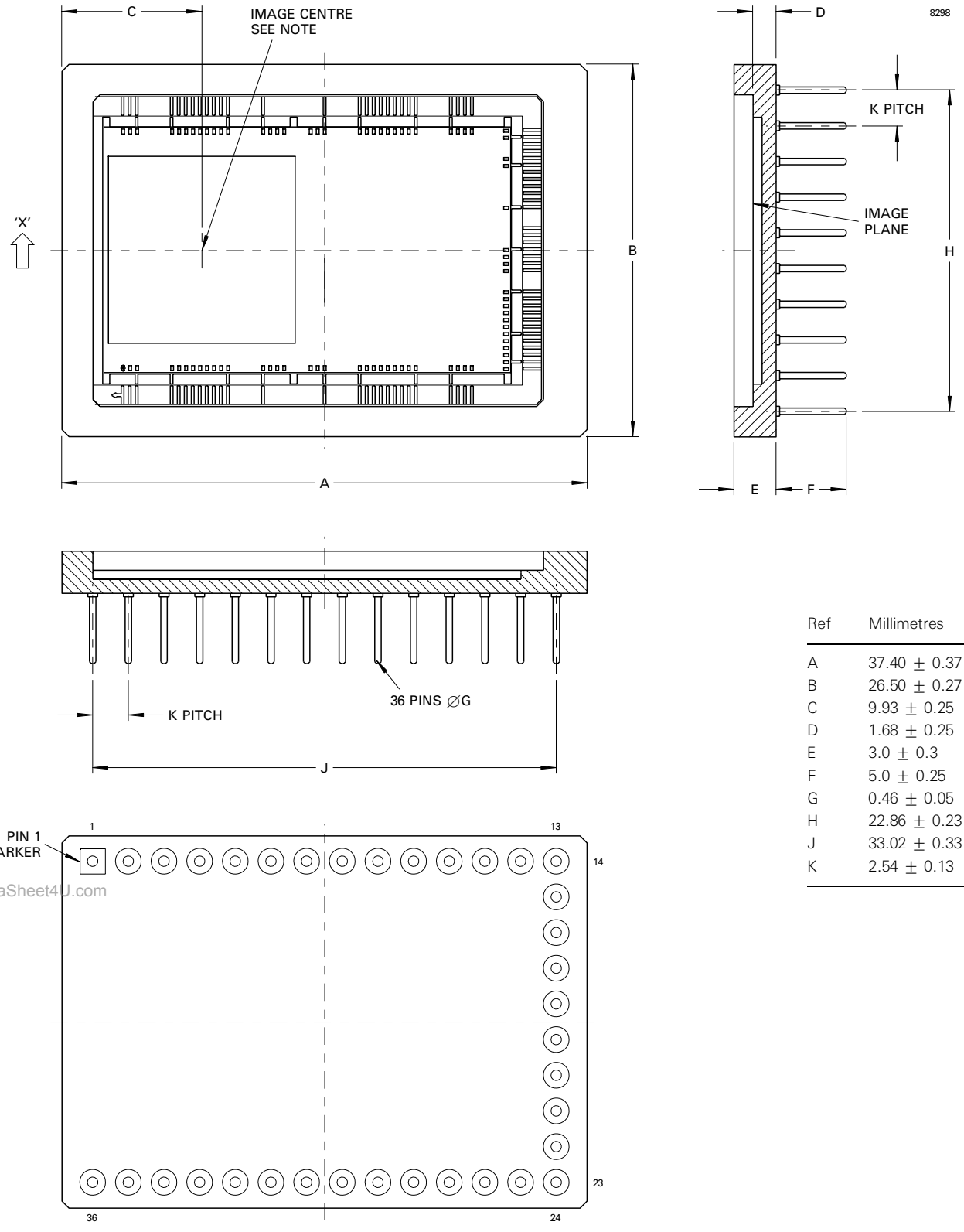

## Figure 14: LINE OUTPUT FORMAT (for Example Line Timing Figure 10)




### NOTE

22. There is a 1-line propagation delay between transferring a line from the store section to the standard register and reading it out through the OSL output amplifier.

## Figure 15: PACKAGE OUTLINE




| Ref | Millimetres |
|---|---|
| A | 37.40 ± 0.37 |
| B | 26.50 ± 0.27 |
| C | 9.93 ± 0.25 |
| D | 1.68 ± 0.25 |
| E | 3.0 ± 0.3 |
| F | 5.0 ± 0.25 |
| G | 0.46 ± 0.05 |
| H | 22.86 ± 0.23 |
| J | 33.02 ± 0.33 |
| K | 2.54 ± 0.13 |



### Outline Note

The image centre is aligned centrally in the package in direction 'X', to within a tolerance of ±0.2 mm.