AN9008-1

10Base ISA Plug & Play Controller
PC Board Layout Design Considerations
Application Note

This application note is designed to inform the designer using the DM9008 about PC board layout considerations. The DM9008's pinout was arranged so that it's pin configuration corresponds closely to the pinout of the ISA bus edge connector. At the same time, the PC board layout accommodates for a lager ground trace when using a two sided PC board configuration.

Digital Trace Routing

Placement of digital components and the routing of digital traces should follow standard "common-sense" digital layout techniques, such as minimizing trace lengths, daisy-chaining bus signals, etc.

Analog Trace Routing

The cardinal rule of analog trace routing is to keep the area enclosed by a circuit loop as small as possible to minimize the incidence of magnetic coupling. However this can conflict with the general rule of keeping trace lengths to a minimum. For example, if circuit components are position along the same sides of a square, the best return route is back along the same three sides of the square, **NOT** directly back along the fourth side. **This rule must be strictly be adhered to.** Furthermore, there should never be an unnecessary via feed-through inside the circuit loop. This also implies that the circuit loop should never encircle the power/ground planes (i.e., part of the circuit loop above and part of the circuit of the circuit loop below these planes). This concept is illustrated in Figure 1.

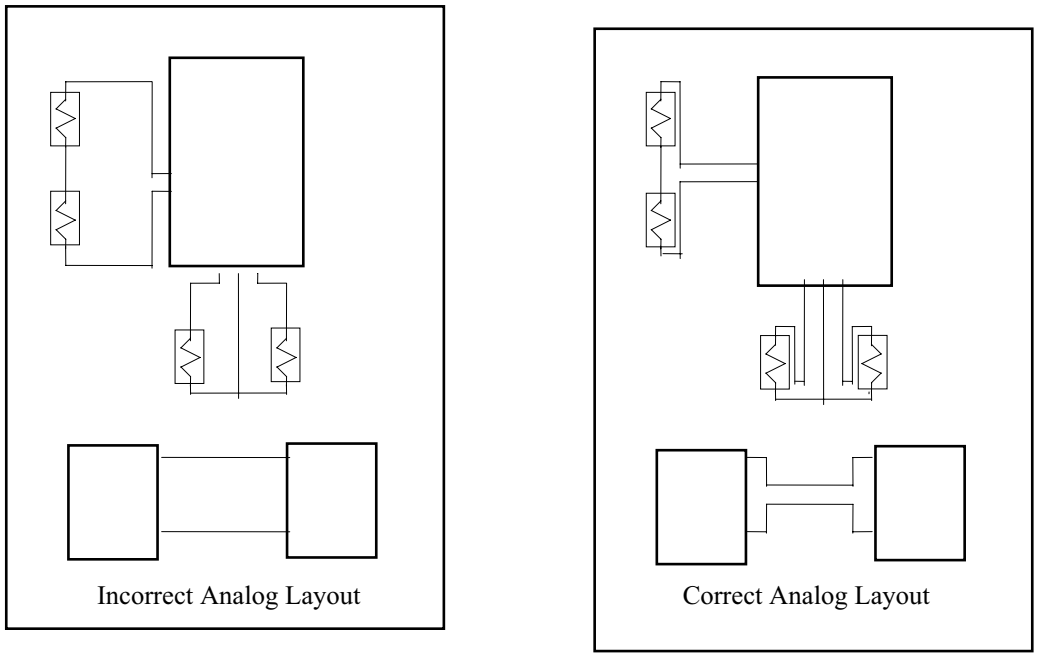

Figure 1.

A simple case of this guideline applies to differential signal pairs. The two traces of the pair should always be routed in adjacent channels. To reduce capacitive coupling, each circuit loop should be separated from

the others. Circuit loops can be separated either by physical space (if located on the same signal layer) or by placement on signal layers on the opposite side of the power/ground planes. The following signal groups should be isolated from each other.

To achieve optimum performance when using a 10Base-2 transceiver the designer must protect the transceiver from the environment. The only layout restriction for the transmitter circuit is that the longest path from the TXO pin (DM9092A, pin 15) to the coaxial cable's center conductor must be no longer than 4 inches. The layout of the receiver circuit RXI (DM9092A, pin 14) is critical to minimize parasitic capacitance that can degrade the received signal. The external receiver should be isolated from the power and ground planes, see figure 2.

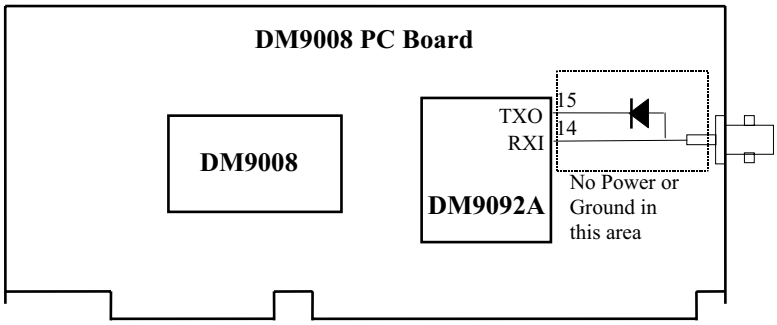

Figure 2.

Decoupling Power and Ground on the DM9008

Placement of the decoupling capacitors for digital VCC is straight forward. Try to locate the decoupling capacitors as physically close to the DM9008's VCC pins as possible. There are three .1μf capacitors required for the digital VCC power to the DM9008. The digital VCC pins are 1,53 and 72.

Decoupling of the analog power requires a more careful approach. The decoupling capacitors should be placed in pin pairs on pins 34 to 43, pins 47 to 44, and pins 48 to 51. The suggested trace routing is illustrated in figure 3. Figure 3 depicts the trace routing for pin pair 34 to 43, the other pin pairs are not shown, but should be routed in the same fashion.

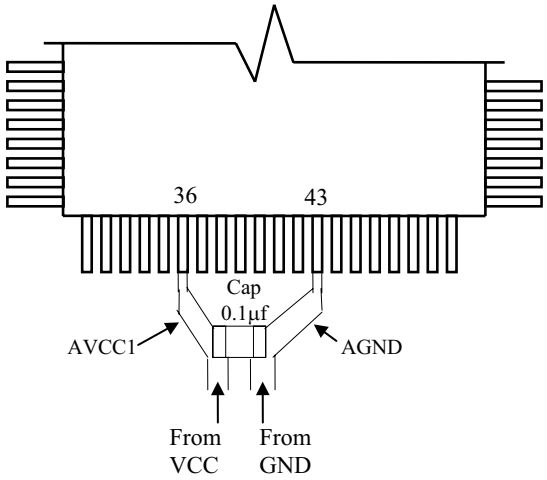

Figure 3

10Base-T Media Filter Placement and Termination

Placement of the termination components for TPTX+ and TPTX- should be located as physically close to the media filter as possible.

The media filter placement should also be placed as physically close to the RJ-45 connector as possible to minimize stray EMI transfer to the media.

Magnetics approved for use for 10Base-T application

Through-Hole PCB:

YCL part no. 20F001N
Fil-Mag. part no. 78Z034
Valor part no. FL1012/1066
Pulse Eng. part no. PE65424

Surface Mount PCB:

YCL part no. 20F001NS
Fil-Mag. part no. 78Z1122D-01
Valor part no. SF1012