19-0619; Rev 0; 8/06

EVALUATION KIT AVAILABLE

HDTV Anti-Aliasing Filters with Triple-Input Mux

General Description

The MAX7472/MAX7473 triple-channel anti-aliasing filters and buffers with triple-input mux are ideal for high-definition (HD) and standard-definition (SD) television (TV) applications. Compatible with 1080i, 720p, 480p, and 480i scanning system standards as well as computer format signals, the MAX7472/MAX7473 support component video (Y P_B P_R, GsBR, and RGBHV) as well as composite (CVBS) and S-video (Y/C).

The MAX7472/MAX7473 limit the input bandwidth for anti-aliasing and out-of-band noise reduction prior to digital conversion by an ADC or video decoder. The frequency response of the MAX7472/MAX7473 can be continuously varied in 256 linear steps from below SD response to beyond HD response through an I²C† interface. The adjustable cutoff frequency allows filter optimization for sampling rate and noise reduction. The MAX7472/MAX7473 also include 3:1 multiplexers for selection of three complete sets of video inputs through the I²C interface.

The MAX7472/MAX7473 drive a $2V_{P-P}$ video signal into a standard 150Ω load. The inputs are AC-coupled and the outputs can be either DC- or AC-coupled. The MAX7472 has a gain of 0dB and the MAX7473 has a gain of +6dB. Both devices are available in a 28-pin TQFN package and are fully specified over the upper-commercial (0°C to +85°C) temperature range.

Applications

HDTV (LCD, PDP, DLP, CRT)

Set-Top Boxes

Personal Video Recorders

Home Theaters

Typical Operating Circuit appears at end of data sheet.

†Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Features

- **Continuously Variable Anti-Aliasing Filter**
  5MHz to 34MHz in 256 Steps
- **3:1 Input Mux on Each Video Filter**
- **Supports All Standard Video and Computer Input Formats**
  480i, 480p, 720p, 1080i
  QVGA, VGA, SVGA, XGA, SXGA, UXGA
  Y P_B P_R, GsBR, RGBHV, Y/C, CVBS
- **Accepts Any Input Sync Format**
  Sync on Y, Sync on G, External Sync (Positive or Negative)
  Sync on All Channels
- **Buffered Outputs Drive Standard 150Ω Video Load**
  0dB (MAX7472)
  +6dB (MAX7473)
- **DC- or AC-Coupled Outputs**
- **Single +5V Analog and +3.3V Digital Supplies**
- **5mW Power-Down Mode**
- **Lead (Pb)-Free 28-Pin TQFN Package**

Ordering Information

PART	PIN-PACKAGE	PKG CODE	BUFFER GAIN (dB)
MAX7472UTI+	28 TQFN-EP*	T2855-8	0
MAX7473UTI+**	28 TQFN-EP*	T2855-8	+6

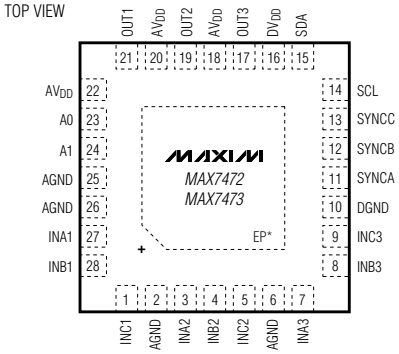
Note: *All devices are specified over the 0°C to +85°C operating temperature range.*

+Indicates lead-free packaging.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

Pin Configuration



TQFN
5mm x 5mm
***EXPOSED PAD.**

HDTV Anti-Aliasing Filters with Triple-Input Mux

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +4V
AGND to DGND.....-0.3V to +0.3V
INA_, INB_, INC_ to AGND.....
.....-0.3V to the lower of (AV_{DD} + 0.3V) and +6V
OUT_ to AGND…….-0.3V to the lower of (AV_{DD} + 0.3V) and +6V
SYNC_, A_ to AGND.....
.....-0.3V to the lower of (AV_{DD} + 0.3V) and +6V
SCL, SDA to DGND.....-0.3V to + 6V

Maximum Current into Any Pin
(except AV_{DD}, DV_{DD}, and OUT) .....±50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range..... 0°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +5V ±5%, DV_{DD} = 2.7V to 3.6V, R_{LOAD} = 150Ω to AGND, C_{IN} = 0.1µF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Filter Passband Response	A_{PB}	HD: f = 100kHz to 30MHz, relative to 100kHz (Note 1)	-3	-0.6	+1	dB
		SD: f = 100kHz to 5.75MHz, relative to 100kHz (Note 2)		±0.1	±1.0	
Filter Stopband Attenuation	A_{SB}	HD: f = 74MHz (Note 1)		57		dB
		SD: f = 27MHz (Note 2)		63		
Group-Delay Deviation	Δt_G	HD: 100kHz to 30MHz, relative to 100kHz (Note 1)		20		ns
		SD: 100kHz to 5.75MHz, relative to 100kHz (Note 2)		15		
Group-Delay Matching	$t_{G(MATCH)}$	HD: channel to channel, 100kHz to 2MHz (Note 1)		5		ns
		SD: channel to channel, 100kHz to 500kHz (Note 2)		1.5		
Bypass Frequency Response		-3dB, bypass mode, independent of filter setting		100		MHz
SD Differential Gain	dG	5-step modulated staircase (Note 2)		0.25		%
SD Differential Phase	dϕ	5-step modulated staircase (Note 2)		0.25		Degrees
Signal-to-Noise Ratio	SNR	Output signal ($2V_{P-P}$) to RMS noise (100kHz to 30MHz) (Note 1)		69		dB
SD Line-Time Distortion	H_{DIST}	Deviations in a line with an 18µs, 100 IRE bar, 1 line = 63.5µs (Note 2)			0.3	%
SD Field-Time Distortion	V_{DIST}	Deviations in 130 lines with 18µs, 100 IRE bars (Note 2)			0.3	%

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = +5V ±5%, DV_{DD} = 2.7V to 3.6V, R_{LOAD} = 150Ω to AGND, C_{IN} = 0.1µF, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clamp Settling Time		To 1% with 100 IRE step (Note 3)	Positive		350		H
			Negative		650		
Minimum Functional Input Sync Amplitude				125			mV
Low-Frequency Gain		T_A = +25°C, MAX7472 (Note 1)		-0.5	0	+0.5	dB
		T_A = +25°C, MAX7473 (Note 1)		5.5	6	6.5	
Low-Frequency Gain Matching		100kHz			0.05		dB
Maximum Input Voltage Amplitude		MAX7472			2.4		V_{P-P}
		MAX7473			1.2		
Maximum Output Voltage Amplitude		DC to 30MHz			2.4		V_{P-P}
Output Clamping Level Variation		(Notes 1, 4)				±120	mV
Mux Crosstalk					-80		dB
Channel-to-Channel Isolation					62		dB
Power-Supply Rejection Ratio	PSRR				50		dB
DIGITAL INPUTS (A1, A0, SYNC_)							
Input Logic High Voltage	V_{IH}			2.0			V
Input Logic Low Voltage	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0 to DV_{DD}			±1	±10	µA
Input Capacitance	C_{IN}				6		pF
DIGITAL INPUTS (SDA, SCL)							
Input Logic High Voltage	V_{IH}			0.7 x DV_{DD}			V
Input Logic Low Voltage	V_{IL}					0.3 x DV_{DD}	V
Input Hysteresis	V_{HYST}			0.05 x DV_{DD}			V
Input Leakage Current	I_{IN}	V_{IN} = 0 to DV_{DD}			±0.1	±10	µA
Input Capacitance	C_{IN}				6		pF
DIGITAL OUTPUT (SDA)							
Output Logic Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Tri-State Leakage Current	I_L	V_{IN} = 0 to DV_{DD}			±0.1	±10	µA
Tri-State Output Capacitance	C_{OUT}				6		pF
POWER REQUIREMENTS							
Analog Supply Voltage Range	AV_{DD}			4.75	5	5.25	V
Digital Supply Voltage Range	DV_{DD}			2.7	3.3	3.6	V
Analog Supply Current	I_{AVDD}	Normal operation, no load			180	200	mA
		Power-down mode, no load			1	1.5	
Digital Supply Current	I_{DVDD}				25		µA

TIMING CHARACTERISTICS

(AV_{DD} = +5V ±5%, DV_{DD} = 2.7V to 3.6V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP (P) and START (S) Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START (Sr) Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START (Sr) Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$	(Note 5)	0		0.9	µs
Data Setup Time	$t_{SU;DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_r		0		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_f		0		300	ns
Fall Time of SDA Signal, Transmitting	t_f	(Note 6)	$20 + 0.1C_b$		300	ns
Setup Time for STOP (P) Condition	$t_{SU;STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	(Note 7)	0		50	ns

Note 1: The filter passband edge is set to code 255.
Note 2: The filter passband edge is set to code 40.
Note 3: 1H is the total line period, depending on the video standard. For NTSC, this is 63.5µs, for HDTV, the line period is 29.64µs.
Note 4: The clamp level is at the sync tip for signals with sync pulses, and is at the blanking level otherwise.
Note 5: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 6: C_b = total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.
Note 7: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

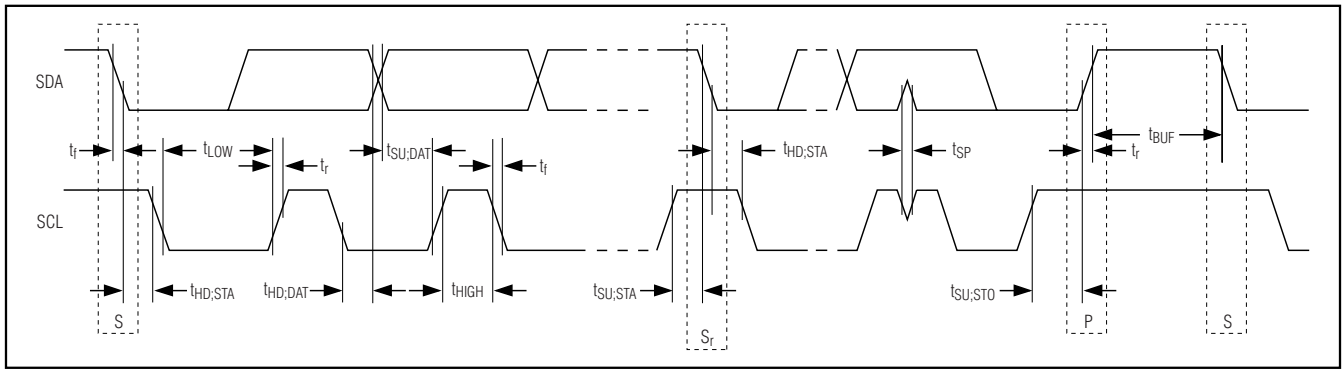
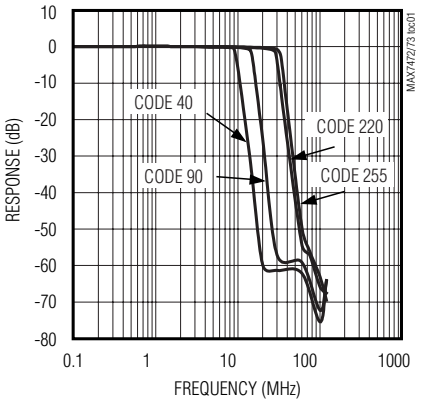


Figure 1. 2-Wire Serial-Interface Timing Diagram

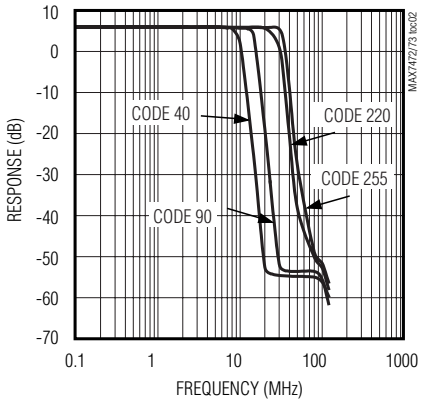
Typical Operating Characteristics

(AV_{DD} = +5V, DV_{DD} = 3.3V, R_{LOAD} = 150Ω to GND, C_{IN} = 0.1µF, T_A = +25°C.)

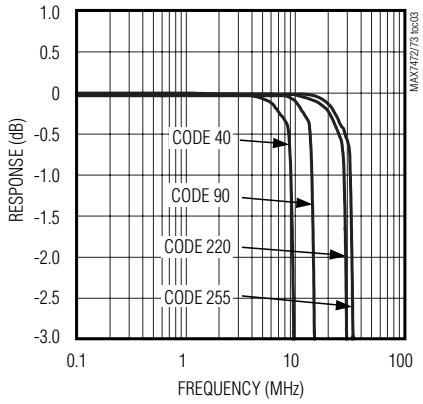
FREQUENCY RESPONSE (MAX7472)



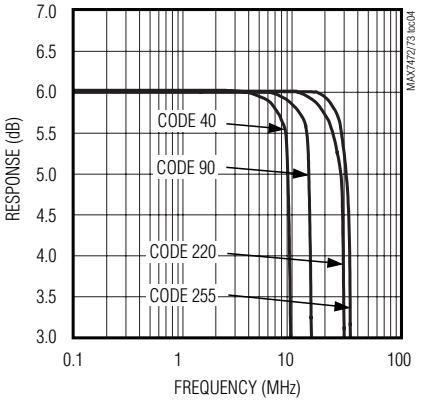
FREQUENCY RESPONSE (MAX7473)



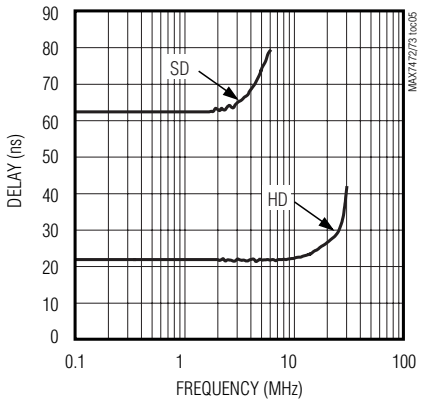
PASSBAND FLATNESS (MAX7472)



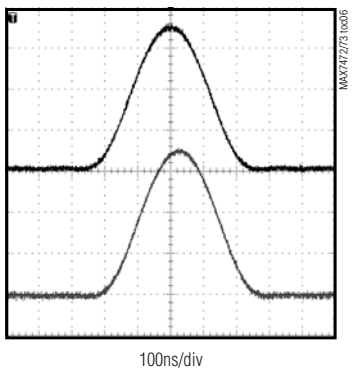
PASSBAND FLATNESS (MAX7473)



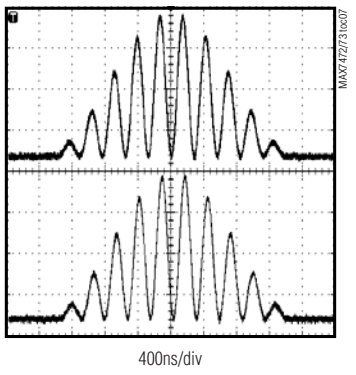
GROUP DELAY



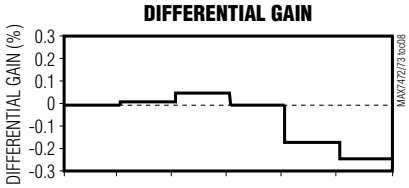
2T RESPONSE (1 IRE = 7.14mV)



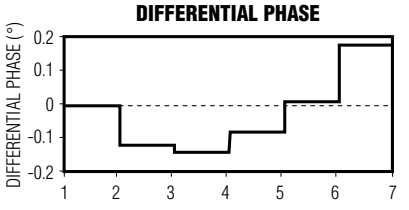
MODULATED 12.5T RESPONSE



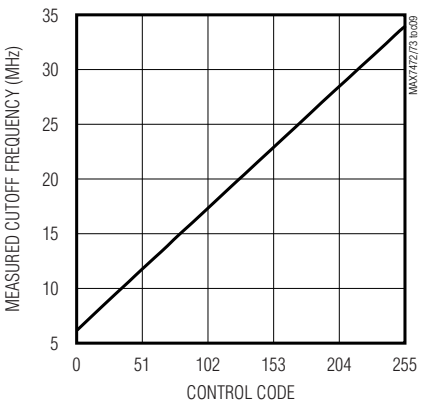
DIFFERENTIAL GAIN



DIFFERENTIAL PHASE



-3dB FREQUENCY vs. CONTROL CODE

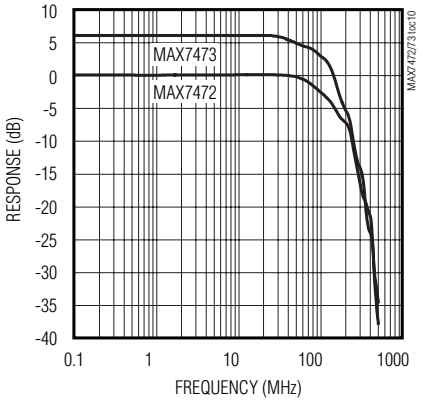


HDTV Anti-Aliasing Filters with Triple-Input Mux

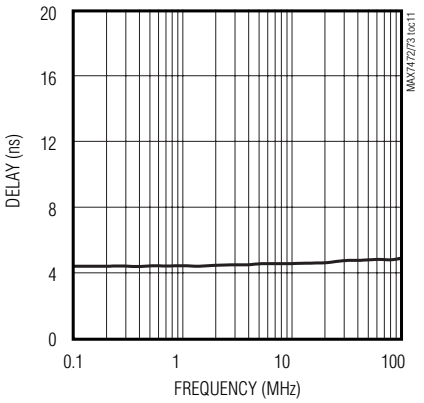
Typical Operating Characteristics (continued)

(AV_{DD} = +5V, DV_{DD} = 3.3V, R_{LOAD} = 150Ω to GND, C_{IN} = 0.1µF, T_A = +25°C.)

BYPASS-MODE FREQUENCY RESPONSE



BYPASS-MODE GROUP DELAY



Pin Description

PIN	NAME	FUNCTION
1	INC1	Channel C Input 1. AC-couple INC1 with a series 0.1µF capacitor.
2, 6, 25, 26	AGND	Analog Ground. Connect all AGND pins to the ground plane. See the *Power-Supply Bypassing and Layout Considerations* section.
3	INA2	Channel A Input 2. AC-couple INA2 with a series 0.1µF capacitor.
4	INB2	Channel B Input 2. AC-couple INB2 with a series 0.1µF capacitor.
5	INC2	Channel C Input 2. AC-couple INC2 with a series 0.1µF capacitor.
7	INA3	Channel A Input 3. AC-couple INA3 with a series 0.1µF capacitor.
8	INB3	Channel B Input 3. AC-couple INB3 with a series 0.1µF capacitor.
9	INC3	Channel C Input 3. AC-couple INC3 with a series 0.1µF capacitor.
10	DGND	Digital Ground. See the *Power-Supply Bypassing and Layout Considerations* section.
11	SYNCA	Channel A External Sync Input. Connect to ground if not used.
12	SYNCB	Channel B External Sync Input. Connect to ground if not used.
13	SYNCC	Channel C External Sync Input. Connect to ground if not used.
14	SCL	I²C-Compatible Serial Clock Input
15	SDA	I²C-Compatible Serial Data Input/Output
16	DV_{DD}	Digital Power Supply. Bypass to DGND with a 0.1µF capacitor. See the *Power-Supply Bypassing and Layout Considerations* section.
17	OUT3	Video Output 3. OUT3 can be either AC- or DC-coupled.
18, 20, 22	AV_{DD}	Analog Power Supply. Bypass each AV_{DD} input to AGND using a 0.1µF capacitor. See the *Power-Supply Bypassing and Layout Considerations* section.

Pin Description (continued)

PIN	NAME	FUNCTION
19	OUT2	Video Output 2. OUT2 can be either AC- or DC-coupled.
21	OUT1	Video Output 1. OUT1 can be either AC- or DC-coupled.
23	A0	Address Bit 0
24	A1	Address Bit 1
27	INA1	Channel A Input 1. AC-couple INA1 with a series 0.1µF capacitor.
28	INB1	Channel B Input 1. AC-couple INB1 with a series 0.1µF capacitor.
—	EP	Exposed Pad. The exposed pad is located on the package bottom and is internally connected to AGND. Connect EP to the analog ground plane. Do not route any PC board traces under the package. See the *Power-Supply Bypassing and Layout Considerations* section.

Detailed Description

The MAX7472/MAX7473 are complete video anti-aliasing solutions ideal for fixed-pixel HDTV display technologies such as plasma and LCD, which digitize the input video signal and then scale the resolution to match the native pixel format of the display. With a software-selectable corner frequency ranging from 5MHz to 34MHz, the MAX7472/MAX7473 support both SD and HD video signals including 1080i, 720p, 720i, 480p, and 480i. Higher bandwidth computer resolution signals are also supported.

Integrated lowpass filters limit the analog video input bandwidth for anti-aliasing and out-of-band noise reduction prior to sampling by an ADC or video decoder. By allowing the corner frequency to be adjusted from below SD resolution to beyond HD resolutions in 256 steps, the filter's corner frequency can be optimized dynamically for a specific input video signal and the sampling frequency of the ADC or video decoder. The MAX7472/MAX7473 provide a filter-bypass mode to support applications requiring a passband greater than 34MHz.

An I^2C interface allows a microcontroller to configure the MAX7472/MAX7473s' performance and functionality including the mux, the clamp voltage, the filter's corner frequency, the sync source (internal/external), and filter bypassing.

The *Typical Operating Circuit* shows the block diagram and typical external connections of the MAX7472/MAX7473.

Sync Detector and Clamp Levels

The MAX7472/MAX7473 use a video clamp circuit to establish a DC offset for the incoming video signal after the AC-coupling capacitor. This video clamp sets the DC bias level of the circuit at the optimum operating point.

The MAX7472/MAX7473 support both internal and external sync detection. Selection of internal vs. external detection is achieved by programming the command byte (see Table 3). After extracting the sync information from channel 1 or an external sync (SYNCA, SYNCB, or SYNCC), the MAX7472/MAX7473 clamp the video signal during the sync tip portion of the video. Select one of two possible clamp levels according to the input signal format. Use the low level when the input signal contains sync information such as Y (luma) or CVBS signals. Use the high level for bipolar signals such as C (chroma) or P_B/P_R. See Table 1.

Table 1. Clamp Levels

INPUT SIGNAL FORMAT	CLAMP LEVEL		
	CHANNEL 1	CHANNEL 2	CHANNEL 3
Y P_B P_R	Low	High	High
GsBR	Low	High	High
CVBS Y C	Low	Low	High
Y P_B P_R (sync on all signals)	Low	Low	Low
R G B H V	High	High	High

HDTV Anti-Aliasing Filters with Triple-Input Mux

Component/Composite Selection

The MAX7472/MAX7473 accept component or composite inputs. The sync detection path provides an additional selectable color burst filter to improve sync detection.

External Sync Detection

When filtering a video signal without embedded sync information, such as computer formats (RGBHV) with separate sync signals, use the external sync mode (see Table 3) and apply the horizontal sync source to the SYNCA, SYNCB, or SYNCC pin. The sync detector determines when the clamp circuit is turned on.

The MAX7472/MAX7473 can detect positive or negative polarity external syncs with TTL logic levels. Use the I²C interface to program the polarity of the external sync signal.

Filter

The internal video filter delivers an optimized response with a steep transition band to achieve a wide passband along with excellent stopband rejection. In addition, the filter is optimized to provide an excellent time-domain response with low overshoot.

Setting the Filter Frequency

The frequency response (-3dB cutoff frequency) of the filter in the MAX7472/MAX7473 can be varied from less than the SD passband to beyond the HD passband in 256 linear steps through the I²C interface. Use the command byte to write to the Frequency register followed by the 8-bit data word that corresponds to the desired frequency. See Table 6.

The Frequency register sets the -3dB point. Set this frequency accordingly to achieve the desired flat passband response.

Optimizing the Frequency Response

Select the frequency according to the resolution of the video-signal format. High-definition signals require higher bandwidth and standard-definition signals require less bandwidth. The actual bandwidth contained in the video signal is a function of the visual resolution of the signal. This bandwidth is typically less than what is indicated by the format resolution (1080i, 720p, 480p, and 480i). For more information on this topic, see Application Note 750: *Bandwidth vs. Video Resolution* on the Maxim website (www.maxim-ic.com). See Table 6.

The frequency response can be optimized to improve the overall performance. There are a number of considerations, one of the most important being the sampling rate of the subsequent ADC or video decoder in the system. In oversampled systems, the sampling rate is significantly more than the desired passband response. The extra frequency span between the passband and the sampling rate contains noise that can be eliminated by setting the corner frequency of the filter to just pass the desired bandwidth. This results in a higher signal-to-noise ratio of the overall system.

Filter Bypass

The MAX7472/MAX7473 offer selectable filter bypassing that allows the input video signals to bypass the internal filters reaching the output buffers unfiltered. The filter-bypass mode is enabled/disabled through the command byte (see Table 3).

Output Buffer

Each output buffer can drive a $2V_{P-P}$ signal into a 150Ω video load. The MAX7472/MAX7473 can drive a DC- or AC-coupled load. The output DC level is controlled to limit the DC voltage on the cable so that the blanking level of the video signal is always less than 1V, meeting the digital TV specification. As a result, output AC-coupling capacitors can be eliminated when driving a cable, thus eliminating the normal adverse effects caused by these capacitors such as line- and field-time distortion, otherwise known as droop. See the *Output Considerations* section for more information.

Gain Options

The MAX7472 features an overall gain of 0dB, while the MAX7473 features an overall gain of +6dB. Use the +6dB option (MAX7473) when driving a back-matched cable. Use the 0dB option (MAX7472) when driving an ADC or video decoder with an input range the same as the input to the MAX7472. To add flexibility, the MAX7472 accepts input signals up to $2V_{P-P}$, twice the standard video-signal range.

Output Clamp Level

The MAX7472/MAX7473 output can be DC- or AC-coupled. The nominal output clamp level in the DC-coupled case depends on the clamp voltage setting and can be determined according to Table 2.

Table 2. Output Clamp Level

CLAMP SETTING	OUTPUT CLAMP LEVEL (mV) (typ)
Low	±100
High	±100

As shown in the *Sync Detector and Clamp Levels* section, the low clamp level is used for signals with sync information and determines the voltage level of the sync tip, while the high clamp level is used for signals without sync information and sets the blanking level.

The absolute voltage level of the output signal is relative to the output clamp level. A video signal containing sync information (i.e., CVBS or Y) is unipolar above the clamp level and conversely, a video signal without sync (i.e., P_B, P_R, or C) is bipolar around the clamp level.

Multiplexers

The MAX7472/MAX7473 provide four 3:1 multiplexers programmable through the I²C interface to select which of three separate channels (channels A, B, C) is to be connected to each video input. The fourth multiplexer is used in conjunction with external sync detection and determines which channel's external sync is to be connected to the external sync input.

See Table 3 and the *Serial Interface* section for more information on how to select a particular channel. After selecting a channel with a command byte, bits CS7 and CS6 of the Channel Selection register reflect the channel setting (Table 7).

Power-Down Mode

The MAX7472/MAX7473 include a power-down mode that reduces the supply current from 180mA (typ) to 1mA (typ) by powering down the analog circuitry. The I²C interface remains active allowing the device to return to full-power operation. The clamp settling time (see the *Electrical Characteristics* table) limits the wake-up time of the MAX7472/MAX7473. After exiting the power-down mode, the MAX7472/MAX7473 resume normal operation using the settings stored prior to power-down. The command byte controls the power-down and wake-up modes (see Table 3). A software reset sets the Control/Status register to its default conditions. The Frequency register and the Channel Selection register are not affected.

Power-On Reset (POR)

The MAX7472/MAX7473 include a power-on reset (POR) circuit that resets the internal registers and I²C interface to their default condition (see Tables 4–7).

Serial Interface

The MAX7472/MAX7473 feature an I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX7472/MAX7473 and the master at rates up to 400kHz.

Once a command byte is written to the MAX7472/MAX7473, the command interpreter changes the Control/Status register and the Channel Selection register accordingly. See the *Control/Status Register* and *Channel-Selection Register* sections for more information. The command interpreter also controls access to the Frequency register (see the *Command Byte (Write Cycle)* section).

The MAX7472/MAX7473 are transmit/receive slave-only devices, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL.

A master device communicates to the MAX7472/MAX7473 by transmitting the proper address (see the *Slave Address* section) followed by a command and/or data words. Each transmit sequence is framed with a START (S) or REPEATED START (Sr) condition and a STOP (P) condition.

The SDA driver is an open-drain output, requiring a pullup resistor (2.4kΩ or greater) to generate a logic-high voltage. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals.

Bit Transfer

Each SCL rising edge transfers 1 data bit. Nine clock cycles are required to transfer the data into or out of the MAX7472/MAX7473. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). When the serial interface is inactive, SDA and SCL idle high.

START and STOP Conditions

A master device initiates communication by issuing a START condition (S), a high-to-low transition on SDA with SCL high (Figure 2). The master terminates transmission by a STOP condition (P) (see the *Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)* section). A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). The STOP condition frees the bus. If a repeated START condition (S_r) is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect address is detected, the MAX7472/MAX7473 then ignore all communication on the I²C bus until the next START or REPEATED START condition, minimizing digital noise and feedthrough.

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Early STOP Conditions

The MAX7472/MAX7473 recognize a STOP condition at any point during transmission except when a STOP condition occurs in the same high pulse as a START condition (Figure 3). This condition is not a legal I²C format; at least one clock pulse must separate any START and STOP conditions. The MAX7472/MAX7473 discard any data received during a data transfer aborted by an early STOP condition.

REPEATED START (S_r) Conditions

An S_r condition is used to indicate a change in direction of data flow (see the *Read Cycle* section). S_r can also be used when the bus master is writing to several I²C devices and does not want to relinquish control of the bus. The MAX7472/MAX7473 serial interface supports continuous write operations with (or without) an S_r condition separating them.

Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)

Successful data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX7472/MAX7473 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 4). To generate a not acknowledge, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse (ninth pulse) and leaves it high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

The MAX7472/MAX7473 generate an acknowledge bit when receiving an address or data by pulling SDA low during the ninth clock pulse. When transmitting data during a read, the MAX7472/MAX7473 do not drive SDA during the ninth clock pulse (i.e., the external pullups define the bus as a logic high) so that the receiver of the data can pull SDA low to acknowledge receipt of data.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address (Figure 5). When idle, the MAX7472/MAX7473 wait for a START condition followed by its slave address. The serial interface compares each address bit by bit, allowing the interface to power down and disconnect from SCL immediately if an incorrect address is detected. After recognizing a START condition followed by the correct address, the MAX7472/MAX7473 are ready to accept or send data. The least significant bit (LSB) of the address byte (R/$\overline{W}$) determines whether the master is writing to or reading from the MAX7472/MAX7473 (R/$\overline{W}$ = 0 selects a write condition, R/$\overline{W}$ = 1 selects a read condi-

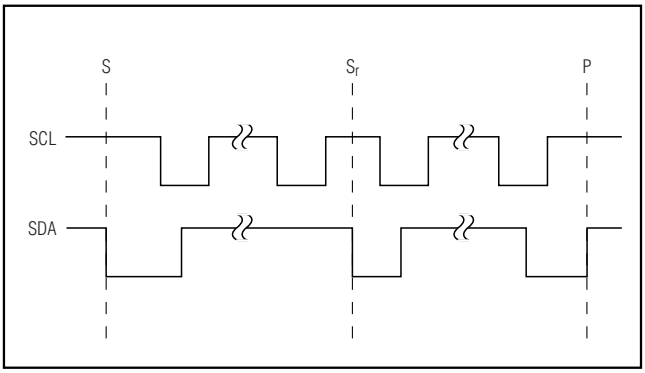

Figure 2. START/STOP Conditions

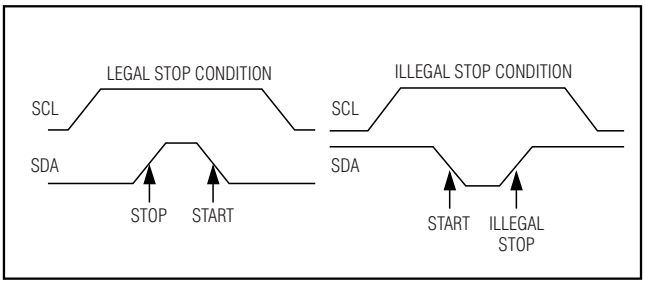

Figure 3. Early STOP Conditions

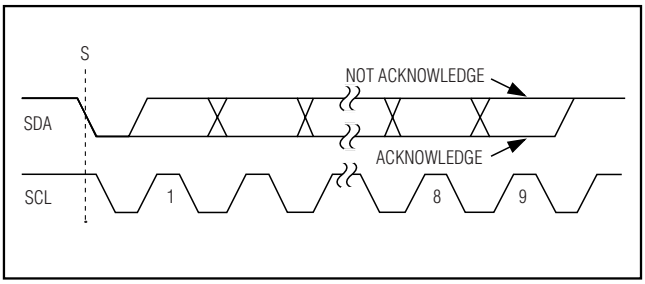

Figure 4. Acknowledge and Not-Acknowledge Bits

tion). After receiving the proper address, the MAX7472/MAX7473 (slave) issue an ACK by pulling SDA low for one clock cycle.

The MAX7472/MAX7473 slave address consists of 5 fixed bits A6–A2 (set to 10010) followed by 2 pin-programmable bits A1 and A0. The most significant address bit (A6) is transmitted first, followed by the remaining bits. Addresses A1 and A0 can also be driven dynamically if required, but the values must be stable when they are expected in the address sequence.

Command Byte (Write Cycle)

A write cycle begins with the bus master issuing a START condition followed by 7 address bits (Figure 5) and a write bit (R/$\overline{W}$ = 0). After successfully receiving its address, the MAX7472/MAX7473 (slave) issue an ACK. The MAX7472/MAX7473 recognize the next byte after a successfully received address as the command byte (Table 3).

Use the command byte to configure the MAX7472/MAX7473. While most of the commands listed in Table 3 modify the functionality of the MAX7472/MAX7473, some commands prepare the device for further data transfers (see the *Control/Status Register*, *Frequency Register*, and *Channel-Selection Register* sections.) When the write cycle is prematurely aborted, the register is not updated. Figures 6 and 7 show examples of write sequences.

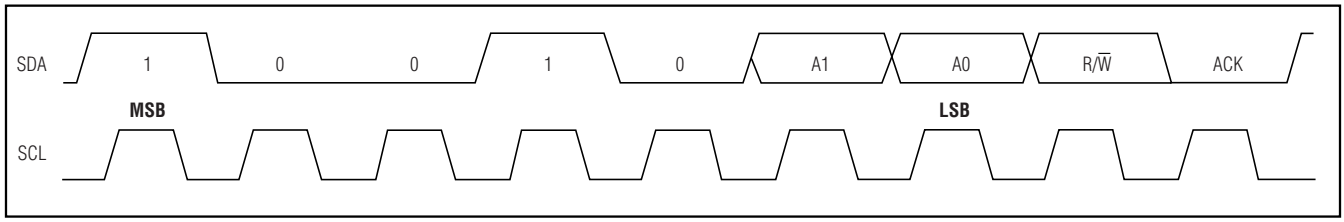

Figure 5. Slave-Address Byte Definition

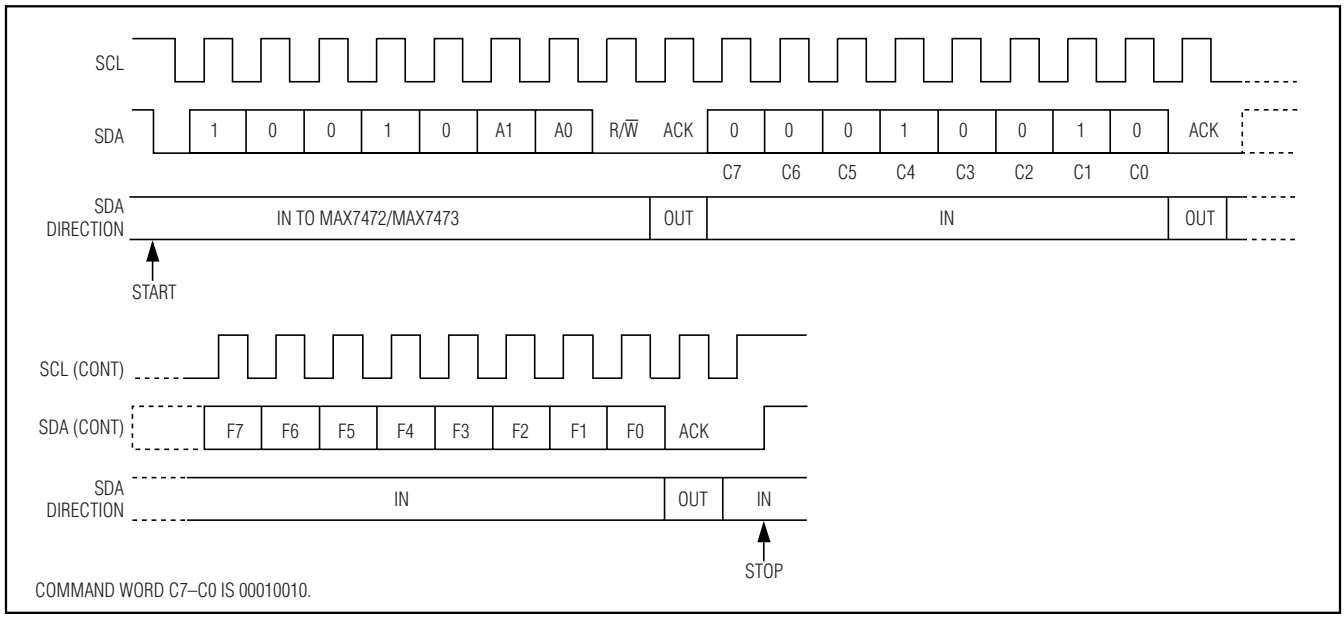

Figure 6. Write Sequence to Update the Frequency Register

Table 3. Command Byte Definition

COMMAND BYTE: INDIVIDUAL BIT DEFINITIONS								DESCRIPTION
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	0	0	0	0	0	Power-down.
0	0	0	0	0	0	0	1	Wake-up; resume normal operation using the frequency/status previously stored (unless power has been cycled).
0	0	0	0	0	0	1	0	Set clamp voltage level for IN1 to low.
0	0	0	0	0	0	1	1	Set clamp voltage level for IN1 to high.
0	0	0	0	0	1	0	0	Set clamp voltage level for IN2 to low.
0	0	0	0	0	1	0	1	Set clamp voltage level for IN2 to high.
0	0	0	0	0	1	1	0	Set clamp voltage level for IN3 to low.
0	0	0	0	0	1	1	1	Set clamp voltage level for IN3 to high.
0	0	0	0	1	0	0	0	Select component input, color-burst filter disabled.
0	0	0	0	1	0	0	1	Select composite input, color-burst filter enabled.
0	0	0	0	1	0	1	0	Select internal sync.
0	0	0	0	1	0	1	1	Select external sync.
0	0	0	0	1	1	0	0	Select positive polarity for the external sync.
0	0	0	0	1	1	0	1	Select negative polarity for the external sync.
0	0	0	0	1	1	1	0	Enable filters.
0	0	0	0	1	1	1	1	Disable filters. Enter bypass mode.
0	0	0	1	0	0	0	0	Reset status to the default status as outlined in the Control/Status register table. This command does not affect the Frequency register and the Channel Selection register.
0	0	0	1	0	0	0	1	Request reading the Control/Status register. The interface expects an S_r condition to follow with address and read/write set to read so that data can be driven onto the bus.
0	0	0	1	0	0	1	0	Load the Frequency register with the data byte following the command word.
0	0	0	1	0	0	1	1	Request reading the Frequency register. The interface expects an S_r condition to follow with address and read/write set to read so that data can be driven onto the bus.
0	0	0	1	0	1	0	0	Select Input A.
0	0	0	1	0	1	0	1	Select Input B.
0	0	0	1	0	1	1	0	Select Input C.
0	0	0	1	0	1	1	1	Request reading the Channel Selection register. The interface expects an S_r condition to follow with address and read/write set to read so that data can be driven onto the bus.

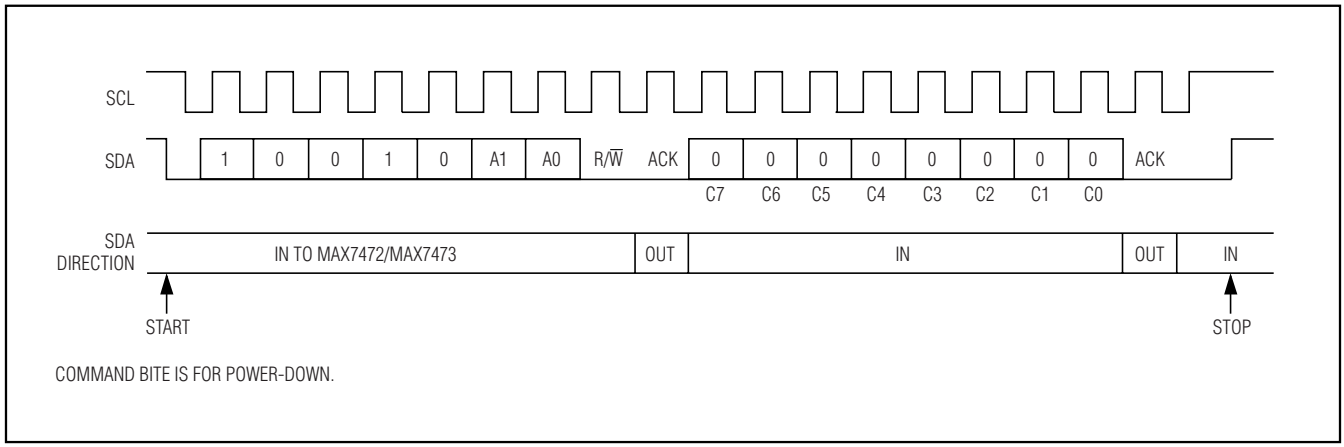

Figure 7. Write Sequence for a Command Bite

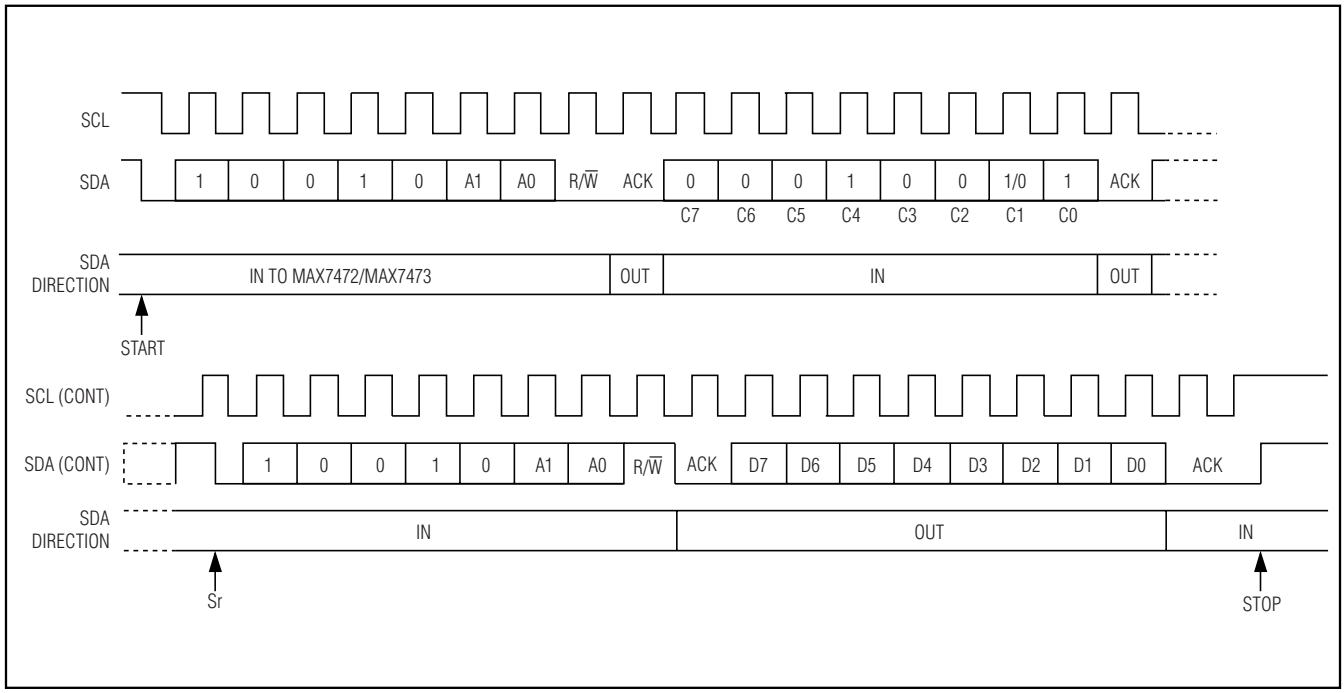

Figure 8. Basic Read Sequence

Read Cycle

In read mode (R/$\overline{W}$ = 1), the MAX7472/MAX7473 write the contents of the Status, Channel Selection, or Frequency register to the bus. When the command byte indicates a read operation of either the Status or the Frequency register, the serial interface expects an Sr condition to follow the command byte. After sending an Sr, the master sends the MAX7472/MAX7473 slave address byte followed by the R/$\overline{W}$ bit (set to 1 to indicate a read). The slave device (MAX7472/MAX7473) generates an ACK for the second address word and immediately after the ACK clock pulse, the direction of data flow reverses. The slave (MAX7472/MAX7473) then transmits 1 byte of data containing the value of the register that was selected in the command byte. Figure 8 shows a basic read sequence.

Note: To read the contents of the Status, Channel Selection, or Frequency register, the master must first write a command byte, requesting to read the Status, Channel Selection, or Frequency register.

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Control/Status Register

The MAX7472/MAX7473 store their status in an 8-bit register that can be read back by the master. The individual bits of the Control/Status register are summarized in Tables 4 and 5. The power-on default value of this register is 03h.

Frequency Register

The frequency response (-3dB passband edge) of the MAX7472/MAX7473 can be continuously varied in 256 linear steps by changing the codes in the Frequency register (Table 6). See the *Command Byte* (*Write Cycle)* section for a write sequence to update the Frequency register.

Table 4. Control/Status Register

CONTROL/STATUS REGISTER							
S7	S6	S5	S4	S3	S2	S1	S0

Table 5. Control/Status Register Bit Description

BIT	DESCRIPTION
S7	0 = component input signal selected (default). 1 = composite input signal selected.
S6	0 = internal sync enabled (default). 1 = external sync enabled.
S5	0 = external sync: positive polarity (default). 1 = external sync: negative polarity.
S4	0 = normal operation mode (default). 1 = power-down mode.
S3	0 = filters enabled (default). 1 = bypass mode—no filtering.
S2	0 = clamp voltage for IN1 set to low (default). 1 = clamp voltage for IN1 set to high.
S1	0 = clamp voltage for IN2 set to low. 1 = clamp voltage for IN2 set to high (default).
S0	0 = clamp voltage for IN3 set to low. 1 = clamp voltage for IN3 set to high (default).

Table 6. Suggested Frequency Register Setting for Various Video-Signal Formats

VIDEO-SIGNAL FORMAT	F7	F6	F5	F4	F3	F2	F1	F0	CODE NUMBER	APPROXIMATE FREQUENCY (-3dB) (MHz)
Standard-Definition Interlaced	0	0	1	0	1	0	0	0	40	10
Standard-Definition Progressive	0	1	0	1	1	0	1	0	90	15
High-Definition Low Bandwidth	1	1	0	1	1	1	0	0	220	30
High-Definition High Bandwidth	1	1	1	1	1	1	1	1	255	34 (default)

Table 7. Channel-Selection Register

CHANNEL-SELECTION REGISTER								DESCRIPTION
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	
0	0	X	X	X	X	X	X	Channel A selected (default).
0	1	X	X	X	X	X	X	Channel B selected.
1	0	X	X	X	X	X	X	Channel C selected.

X = Don't care.

Channel-Selection Register

The MAX7472/MAX7473 store channel selection in an 8-bit register that can be read back by the master. The individual bits of the Channel Selection register are summarized in Table 7. The power-on default selects channel A.

I²C Compatibility

The MAX7472/MAX7473 are compatible with existing I²C systems supporting standard I²C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The devices' address is compatible with 7-bit I²C addressing protocol only. Ten-bit address formats are not supported.

Applications Information

Input Considerations

Use 0.1µF ceramic capacitors to AC-couple the inputs. The input cannot be DC-coupled. The internal clamp circuit stores a DC voltage across the input capacitors to obtain the appropriate output DC voltage level. Increasing the value of these capacitors to improve line-time distortion is not necessary due to the extremely low input leakage current yielding a very low line-time distortion performance.

The MAX7472/MAX7473 provide a high input impedance to allow a nonzero source impedance to be used such as when the input is connected directly to a back-matched video cable, ensuring the external resistance determines the termination impedance.

Output Considerations

The MAX7472/MAX7473 outputs can be DC- or AC-coupled. The MAX7473, with +6dB gain, is typically connected to a 75Ω series back-match resistor followed by the video cable. Because of the inherent divide-by-two of this configuration, the blanking level of the video signal is always less than 1V, which complies with digital TV requirements.

The MAX7472, with 0dB gain, is typically connected to an ADC or video decoder. This can be a DC or AC connection. If a DC connection is used, ensure that the DC input requirements of the ADC or video decoder are compatible.

When using an AC connection, choose an AC-coupling capacitor value that ensures that the lowest frequency content in the video signal is passed and the line-time distortion is kept within desired limits. The selection of this value is a function of the input impedance and more importantly, the input leakage of the circuit being driven. Use a video clamp to reestablish the DC level if not already included in the subsequent circuit.

The outputs of the MAX7472/MAX7473 are fully protected against short-circuit conditions either to ground or to the positive supply of the device.

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Power-Supply Bypassing and Layout Considerations

The MAX7472/MAX7473 operate from a single +5V analog supply and +3.3V digital supply. Bypass each AV_{DD} to AGND with a 0.1µF capacitor with an additional 1µF capacitor in parallel for low-frequency decoupling. Determine the proper power-supply bypassing necessary by taking into account the desired disturbance level tolerable on the output, the power-supply rejection of the MAX7472/MAX7473, and the amplitude and frequency of the disturbance signals present in the vicinity of the MAX7472/MAX7473. Use an extensive ground plane to ensure optimum performance. The three AV_{DD} inputs (pins 18, 20, and 22) that supply the individual channels can be connected together and bypassed as one provided the components are close to the pins. Bypass DV_{DD} to DGND with a 0.1µF capacitor. Connect all ground pins to a low-impedance ground plane as close to the device as possible.

Place the input termination resistors as close to the device as possible. Alternatively, the terminations can be placed further from the device if the PC board traces are designed to be a controlled impedance of 75Ω. Minimize parasitic capacitance as much as possible to avoid performance degradation in the upper frequency range possible with the MAX7472/MAX7473.

Refer to the MAX7472/MAX7473 evaluation kit for a proven PC board layout.

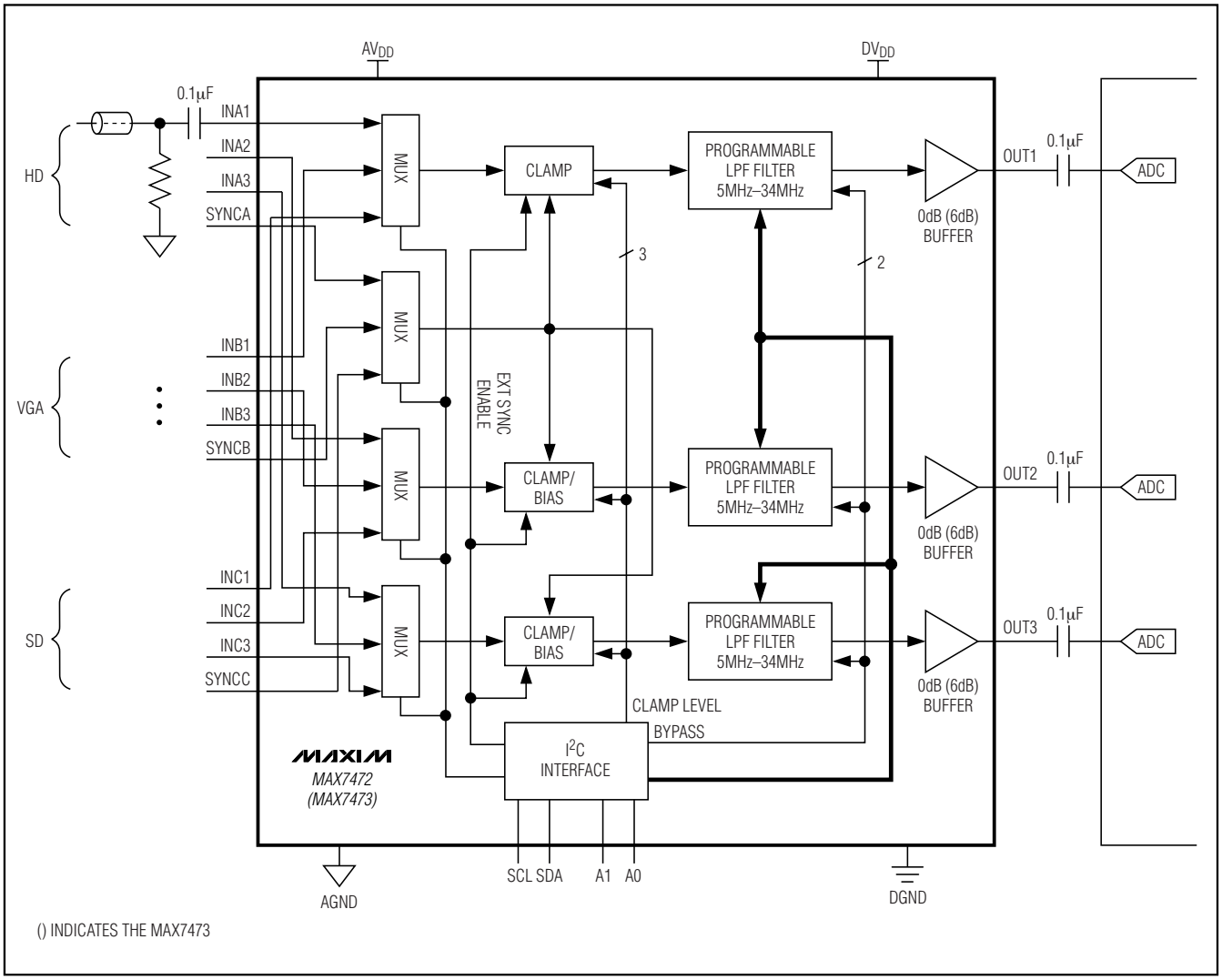
Exposed Pad and Heat Dissipation

The MAX7472/MAX7473 TQFN package provides an exposed pad on the bottom side of the package. This pad is electrically connected to AGND and must be soldered to the ground plane for proper thermal conductivity. Do not route any PC board traces under the package.

The MAX7472/MAX7473 typically dissipate 900mW of power; therefore, pay attention to heat dispersion. Use at least a two-layer board with a good ground plane. To maximize heat dispersion, place copper directly under the MAX7472/MAX7473 package to match the outline of the plastic encapsulated area. Repeat the same with the bottom ground plane layer and place as many vias as possible connecting the top and layers to thermally connect to the ground plane.

Maxim has evaluated a four-layer board using FR-4 material and 1oz copper with equal areas of metal on the top and bottom side coincident with the plastic encapsulated areas of the package. The two middle layers are used as power and ground planes. The board has 21, 15-mil, plated-through via holes between top, bottom, and ground plane layers. Thermocouple measurements confirm device temperatures to be safely within maximum limits.

Typical Operating Circuit



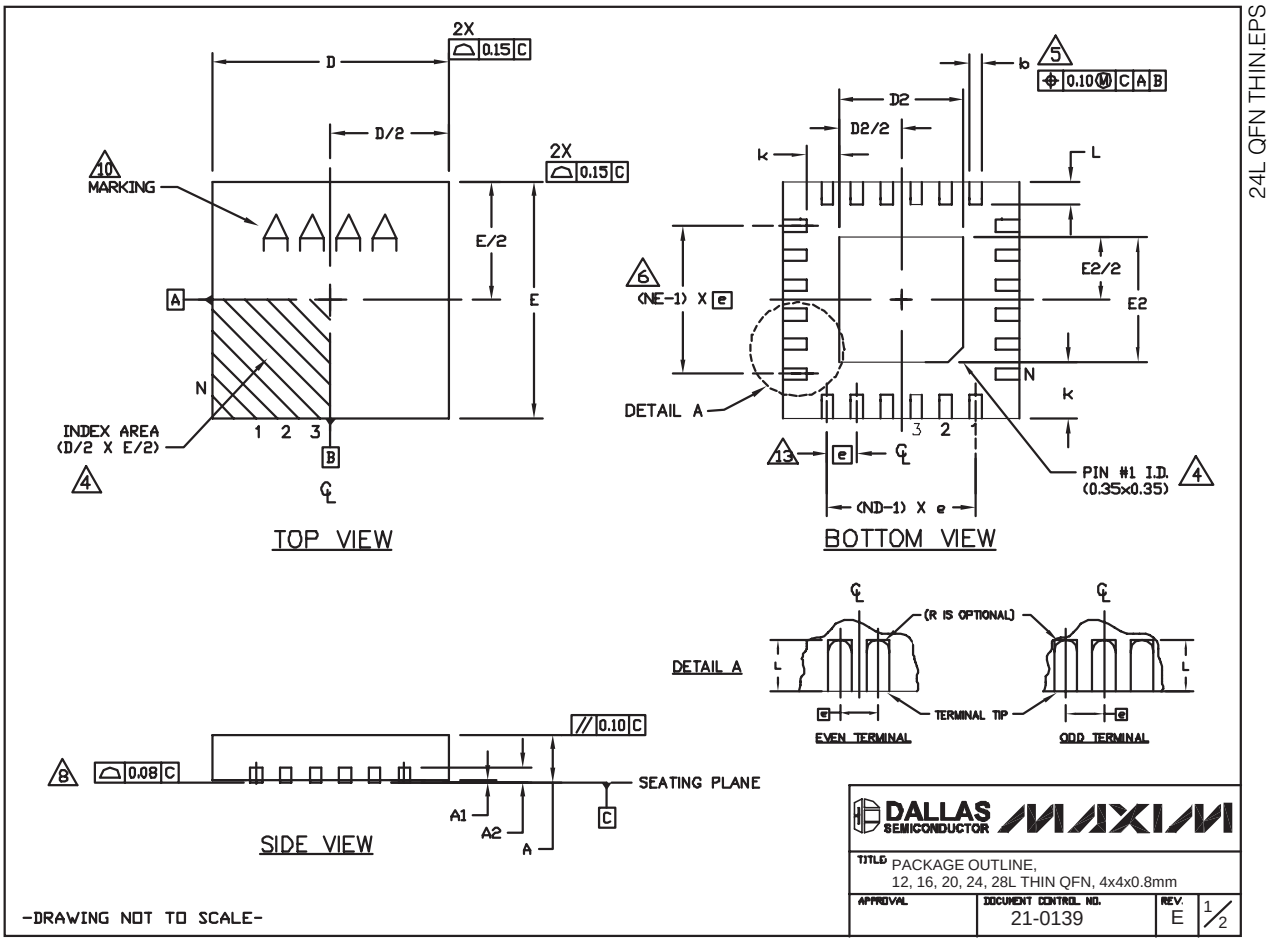
Chip Information

PROCESS: BiCMOS

HDTV Anti-Aliasing Filters with Triple-Input Mux

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2