MC10E411

5V ECL 1:9 Differential PECL/NECL RAMBus Clock Buffer

The MC10E411 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC10E411's function and performance are similar to the popular MC10E111, with the added feature of 1.2 V output swings.

The output voltage swing of the E411 is larger than a standard ECL swing. The 1.2 V output swings provide a signal which can be AC coupled into RAMBus compatible input loads. The larger output swings are produced by lowering the V_{OL} of the device. With the exception of the lower V_{OL}, the E411 is identical to the MC10E111. Note that the larger output swings eliminate the possibility of temperature compensated outputs, thus the E411 is only available in the 10E style of ECL. In addition, because the V_{OL} is lower than standard ECL, the outputs cannot be terminated to –2.0 V. This data sheet provides a few termination alternatives.

The E411 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate–to–gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot–to–lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated, even if only one side is being used. In most applications, all nine differential pairs will be used, and therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC10E411, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the E411 to be used for high performance clock distribution in +5.0 V systems. Designers can take advantage of the E411's performance to distribute low–skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to ON Semiconductor Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

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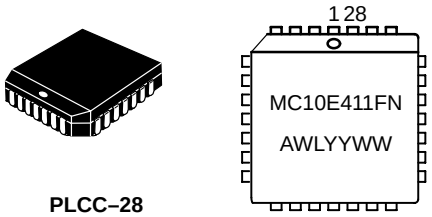
MARKING DIAGRAM



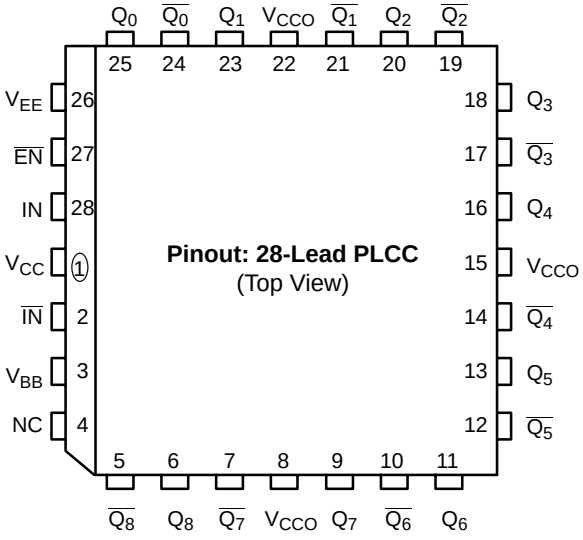
PLCC–28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E411FN	PLCC–28	37 Units/Rail
MC10E411FNR2	PLCC–28	500 Tape & Reel

- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage Compensated Outputs
- V_{EE} Range of –4.5 to –5.5 V
- PECL Mode Operating Range:
  V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 kV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, refer to Application Note AND8003/D
- Flammability Rating:
  UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 180 devices



All V_{CC} and V_{CCO} pins are tied together on the die
Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagram and Pinout Assignment

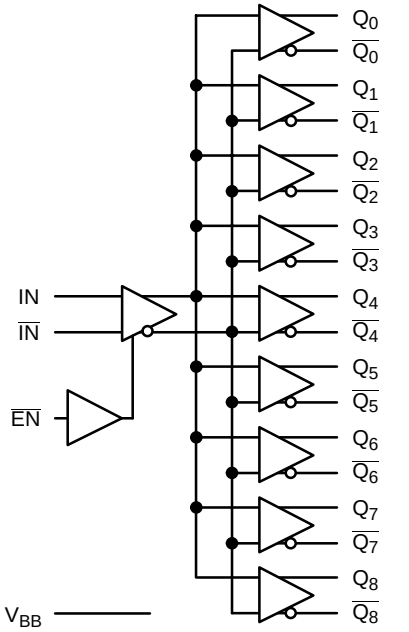


Figure 2. Logic Symbol

PIN DESCRIPTION

PIN	FUNCTION
IN, $\overline{IN}$	ECL Differential Input Pair
$\overline{EN}$	ECL Enable
Q0, $\overline{Q0}$–Q8, $\overline{Q8}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

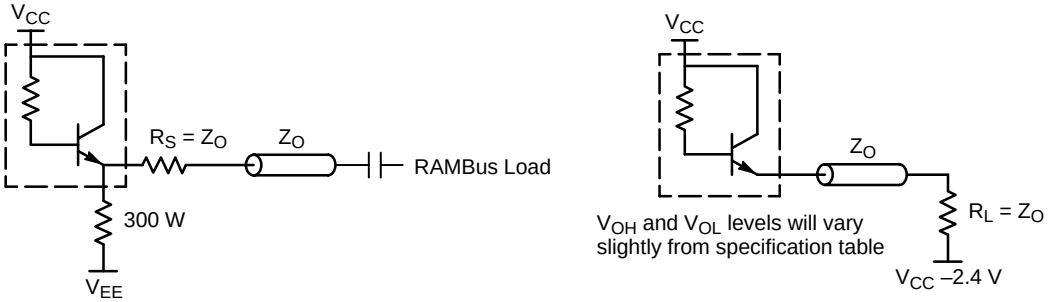


Figure 3. Termination Alternatives

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 2)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	65		55	65		55	65	mA
V_{OH}	Output HIGH Voltage (Note 3)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	2580	2750	2920	2620	2785	2950	2690	2865	3040	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	3.4		4.6	3.4		4.6	3.4		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.5 V / –0.5 V.
3. Outputs are terminated through a 300 ohm resistor to V_{EE}.
4. V_{IHCMR} min and max vary 1:1 with V_{CC}.

NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = –5.0 V (Note 5)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	65		55	65		55	65	mA
V_{OH}	Output HIGH Voltage (Note 6)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 6)	–2420	–2250	–2080	–2380	–2215	–2050	–2310	–2135	–1960	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	–1.6		–2.4	–1.6		–0.4	–1.6		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.5 V / –0.5 V.
6. Outputs are terminated through a 300 ohm resistor to V_{EE}.
7. V_{IHCMR} min and max vary 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 8)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 9) IN (single-ended) (Note 10) $\overline{EN}$ to Q	 400 350 450		 600 650 850	 430 380 450		 630 680 850	 500 450 450		 700 750 850	ps
t_S	Setup Time (Note 11) $\overline{EN}$ to IN	200	0		200	0		200	0		ps
t_H	Hold Time (Note 12) IN to $\overline{EN}$	0	–200		0	–200		0	–200		ps
t_R	Release Time (Note 13) $\overline{EN}$ to IN	300	100		300	100		300	100		ps
t_{skew}	Within-Device Skew (Note 14) Part-to-Part Skew (Diff)			50 200			50 200			50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing (Note 15)	250		1000	250		1000	250		1000	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	275		600	275		600	275		600	ps

8. V_{EE} can vary +0.5 V / –0.5 V.
9. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
10. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
11. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
12. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
13. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times.
14. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
15. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E411 as a differential input as low as 50 mV will still produce full ECL levels at the output.

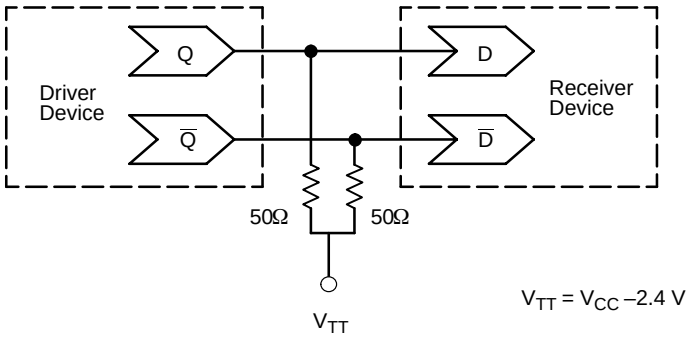


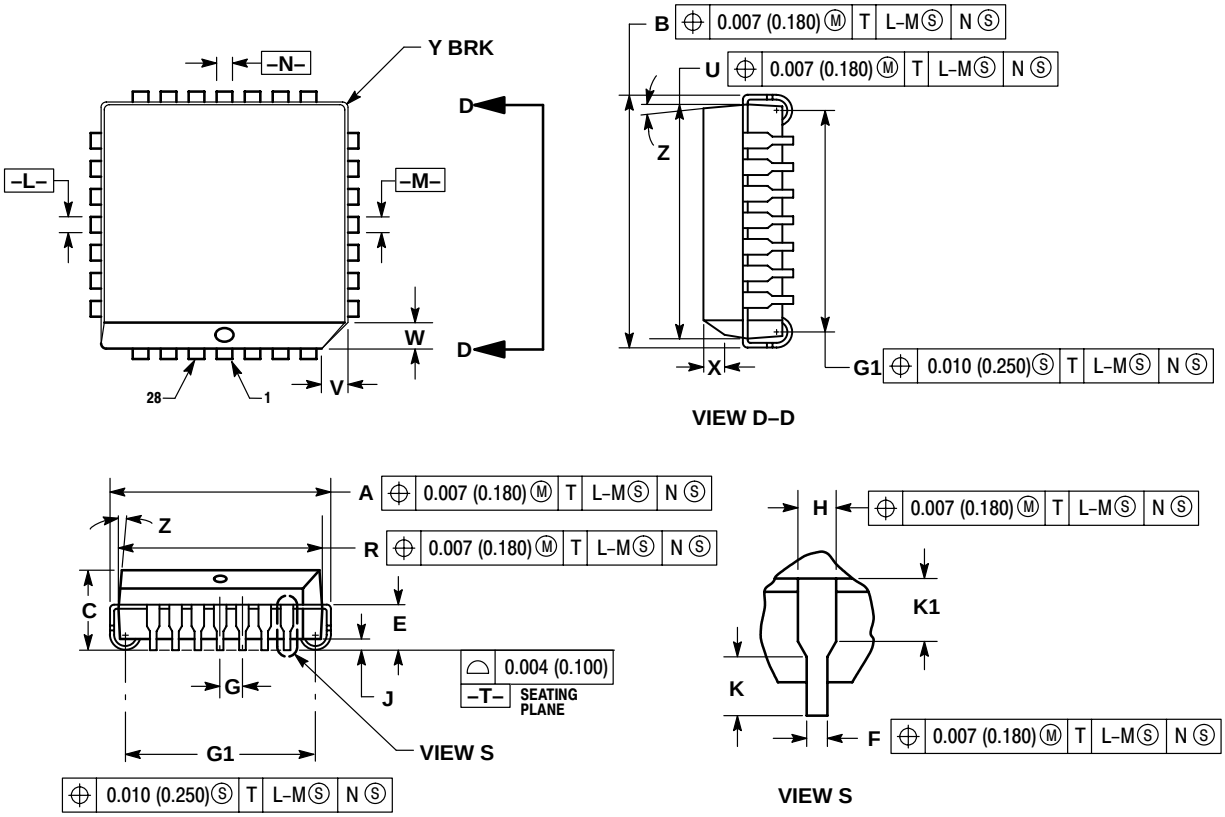
Figure 4. Termination for Output Driver and Device Evaluation of This Device (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing With PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

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