12-BIT BINARY A/D CONVERTER

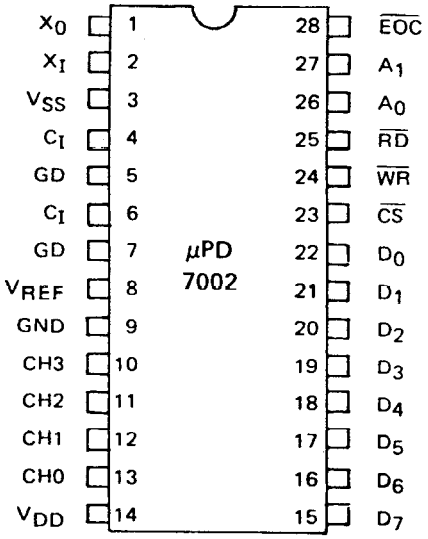
DESCRIPTION

The μPD7002 is a high performance, low power, monolithic CMOS A/D converter designed for microprocessor applications. The analog input voltage is applied to one of the four analog inputs. By loading the input register with the multiplexer channel and the desired resolution (8 or 12 bits) the integrating A/D conversion sequence is started. At the end of conversion $\overline{EOC}$ signal goes low and if connected to the interrupt line of microprocessor it will cause an interrupt. At this point the digital data can be read in two bytes from the output registers. The μPD7002 also features a status register that can be read at any time.

FEATURES

- Single Chip CMOS LSI
- Resolution: 8 or 12 Bits
- 4 Channel Analog Multiplexer
- Auto-Zeroscale and Auto-Fullscale Corrections without any External Components
- High Input Impedance: 1000MΩ
- Readout of Internal Status Register Through Data Bus
- Single +5V Power Supply
- Interfaces to Most 8-Bit Microprocessors
- Conversion Speed: 5 ms
- Power Consumption: 20 mW
- Available in a 28 Pin Plastic Package

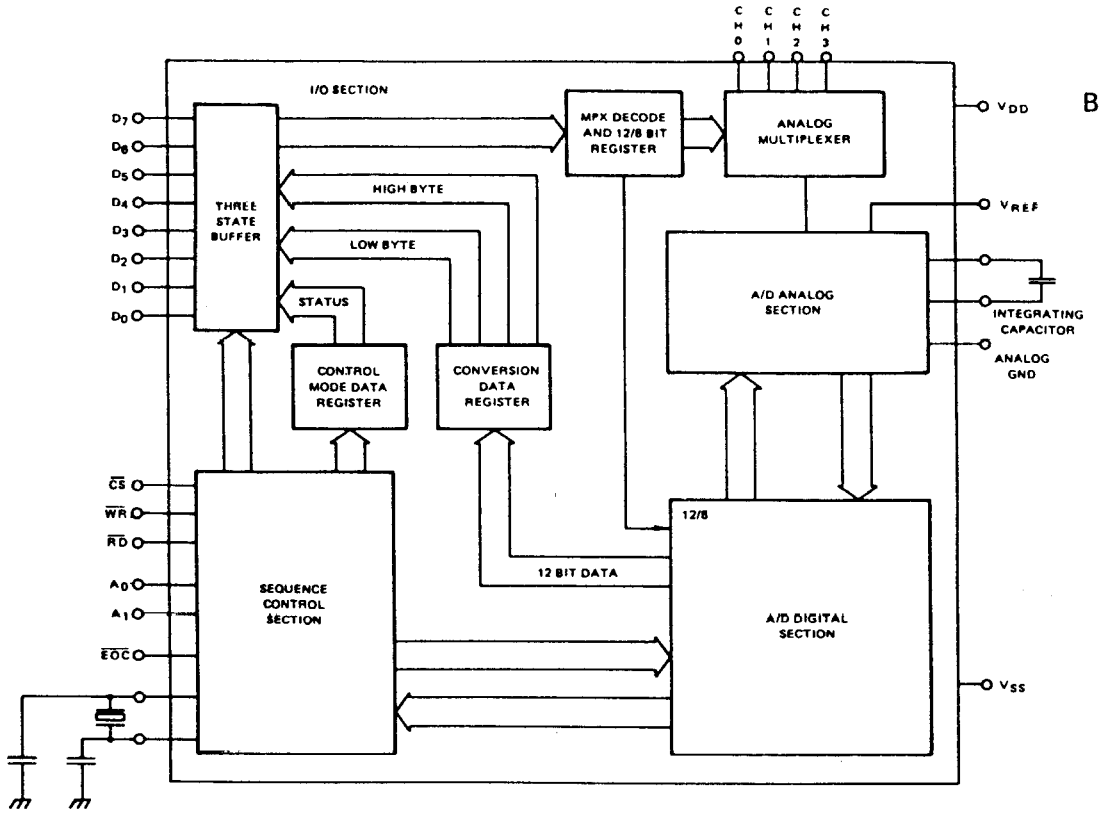
PIN CONFIGURATION



PIN NAMES

X_0,X_I	External Clock Input
V_{SS}	TTL Ground
C_I	Integrating Capacitor
GD	Guard
V_{REF}	Reference Voltage Input
GND	Analog Ground
CH3	Analog Channel 3
CH2	Analog Channel 2
CH1	Analog Channel 1
CH0	Analog Channel 0
V_{DD}	TTL Voltage (+5V)
D_0-D_7	Data Bus
$\overline{CS}$	Chip Select
$\overline{WR}$, $\overline{RD}$	Control Bus
A_0,A_1	Address Bus
$\overline{EOC}$	End of Conversion Interrupt

BLOCK DIAGRAM



DC CHARACTERISTICS

T_a = 25 ± 2°C; V_{DD} = +5 ± 0.25V, V_{REF} = +2.50V, f_{CK} = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution			12		Bits	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Non Linearity			0.05	0.08	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V,
Fullscale Error			0.05	0.08	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Zeroscale Error			0.05	0.08	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Fullscale Temperature Coefficient			10		PPM/°C	V_{DD} = 5V
Zeroscale Temperature Coefficient			10		PPM/°C	V_{DD} = 5V
Analog Input Voltage Range	V_{IA}	0		V_{REF}	V	
Analog Input Resistance	R_{IA}		1000		MΩ	V_{IA} = V_{SS} to V_{DD}
Total Unadjusted Error 1	T.U.E. 1		0.05	0.08	%FSR	V_{REF} = 2.25 to 2.75V, V_{DD} = 5V
Total Unadjusted Error 2	T.U.E. 2		0.05	0.08	%FSR	V_{REF} = 2.5V, V_{DD} = 4.75 to 5.25V
Clock Input Current	I_{XI}		5	50	μA	
Clock Input High Level	V_{XIH}	V_{DD}−1.4			V	
Clock Input Low Level	V_{XIL}			V_{SS}+1.4	V	
High Level Input Voltage	V_{IH}	2.2			V	T_a = −20°C to +70°C
Low Level Input Voltage	V_{IL}			0.8	V	T_a = −20°C to +70°C
High Level Output Voltage	V_{OH}	3.5			V	I_O = −1.6 mA T_a = −20°C to +70°C
Low Level Output Voltage	V_{OL}			0.4	V	I_O = +16 mA T_a = −20°C to +70°C
Digital Input Leakage Current	I_I		1	10	μA	V_I = V_{SS} to V_{DD}
High-Z Output Leakage Current	I_{Leak}		1	10	μA	V_O = V_{SS} to V_{DD}
Power Dissipation	Pd		15	25	mW	f_{CK} < 1 MHz

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-20°C to +70°C
Storage Temperature	-65°C to +125°C
All Input Voltages	-0.3 to V_{DD} + 0.3 Volts
Power Supply	-0.3 to +7 Volts
Power Dissipation	300 mW
Analog GND Voltage	V_{SS} ± 0.3 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

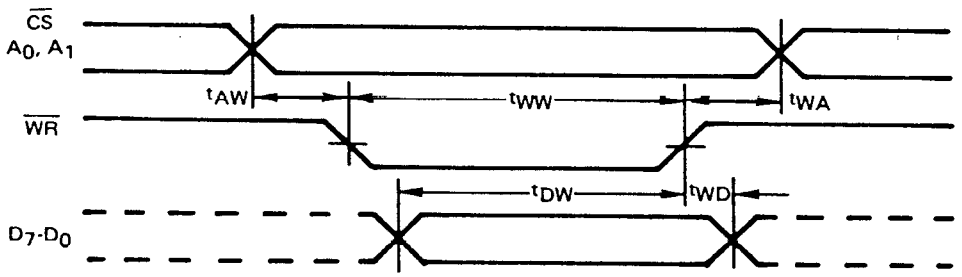
AC CHARACTERISTICS

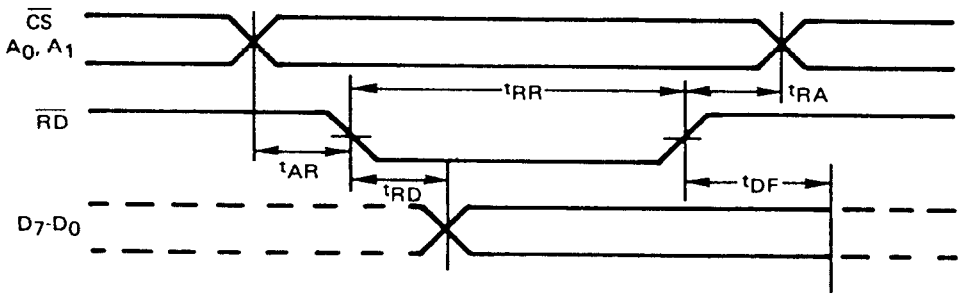
T_a = 25° ± 2°C; V_{DD} = +5 ± 0.25V; V_{REF} = 2.5V; f_{CK} = 1 MHz; C_{INT} = 0.033 μF

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Conversion Speed (12 bit)	t_{CONV}	8.5	10	15	ms	f_{CK} = 1 MHz
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	f_{CK} = 1 MHz
Clock Frequency Range	f_{CK}	0.1	1	3	MHz	
Integrating Capacitor Value	C_{INT}*	0.029			μF	V_{REF} = 2.50V, f_{CK} = 1 MHz
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to CS, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to CS, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	1TTL + 100 pF
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

* $C_{INT}(\mu F)(Min) = 0.029/f_{CK}(MHz)$

TIMING WAVEFORMS





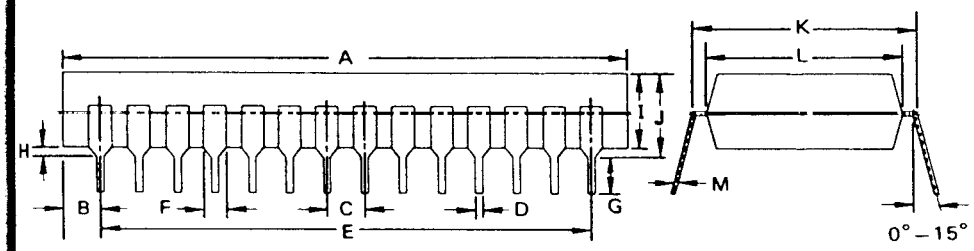
CONTROL TERMINAL FUNCTIONS

CONTROL TERMINALS					MODE	INTERNAL FUNCTION	DATA INPUT-OUTPUT TERMINALS
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0			
H	x	x	x	x	Not selected		High impedance
L	H	H	x	x	Not selected	–	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D_1, D_0 = MPX address D_3 = 8 bit/12 bit conversion designation. ① D_2 = Flag Input
L	H	L	L	H	Not selected	–	High Impedance
L	H	L	H	L	Not selected	–	
L	H	L	H	H	Test mode	Test status	Input status ②
L	L	H	L	L	Read mode	Internal status	D_7 = $\overline{EOC}$, D_6 = $\overline{BUSY}$, D_5 = MSB, D_4 = 2nd MSB, D_3 = 8/12, D_2 = Flag Output D_1 = MPX, D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7-D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7-D_4 = 9th – 12th bit, D_3-D_0 = L
L	L	H	H	H	Read mode	Low data byte	

Notes: ① Designation of number of conversion bits: 8 bit = L; 12 bit = H

② Test Mode: Used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.

PACKAGE OUTLINE μPD7002C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$